DUAL DIGITAL ISOLATOR

Check for Samples: ISO7221C-HT

FEATURES

- **1-, 5- and 25-Mbps Signaling Rate Options**
  - **Low Channel-to-Channel Output Skew; 1 ns max**
  - **Low Pulse-Width Distortion (PWD); 1 ns max**
  - **Low Jitter Content; 1 ns Typ at 150 Mbps**
- **4000-V_{peak} Isolation, 560 V_{peak} V_{IORM}**
  - **UL 1577 Approved**
  - **50-kV/μs Typical Transient Immunity**
- **Operates with 3.3-V or 5-V Supplies**
- **4-kV ESD Protection**
- **High Electromagnetic Immunity**

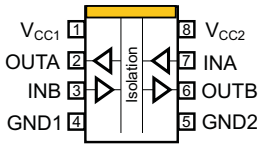
APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C to 175°C) Temperature Range** (1) (2)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

ISO7221C



(1) Custom temperature ranges available.
(2) Device is qualified to ensure reliable operation for 1000 hours at maximum rated temperature. This includes, but is not limited to temperature bake, temperature cycle, electro migration, bond inter metallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION

The ISO7221 is a dual-channel digital isolator. To facilitate PCB layout, the channels are oriented in the opposite directions. This device has a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, this device blocks high voltage, isolates grounds, and prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received every 4 μs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

The small capacitance and resulting time constant provide fast operation with signaling rates available from 0 Mbps (dc) to 150 Mbps. (3) The A-, B- and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device. The M-option devices have CMOS V_{CC}/2 input thresholds and do not have the input noise-filter and the additional propagation delay.

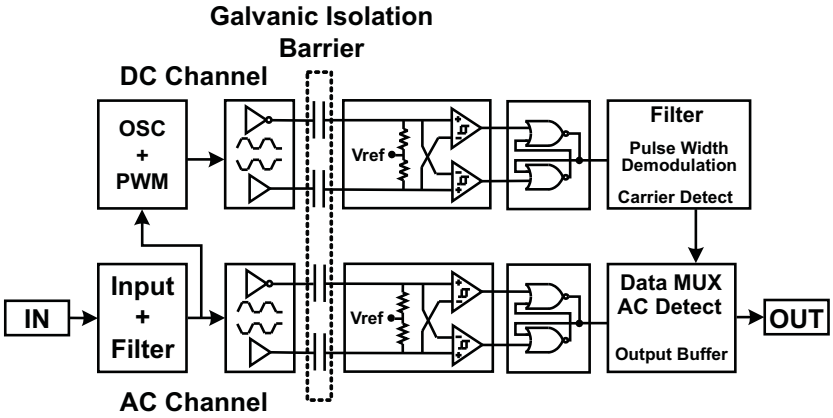
(3) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

This device requires two supply voltages of 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS.

The ISO7221 is characterized for operation over the ambient temperature range of –55°C to 175°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SINGLE-CHANNEL FUNCTION DIAGRAM



AVAILABLE OPTIONS[1]

PRODUCT	MAX SIGNALING RATE	PACKAGE[2]	INPUT THRESHOLD	MARKED AS	ORDERING NUMBER
ISO7221C	25 Mbps	SOIC-8	≠ 1.5 V (TTL) (CMOS compatible)	I7221H	ISO7221CHD

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

REGULATORY INFORMATION

UL
Recognized under 1577 Component Recognition Program[1]
File Number: E181974

(1) Production tested ≥3000 VRMS for 1 second in accordance with UL 1577.

ABSOLUTE MAXIMUM RATINGS[1]

					VALUE	UNIT
V_{CC}	Supply voltage[2], V_{CC1}, V_{CC2}				–0.5 to 6	V
V_I	Voltage at IN, OUT				–0.5 to 6	V
I_O	Output current				±15	mA
ESD	Electrostatic discharge	Human Body Model	Electrostatic discharge JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				180	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	3		5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			mA
t_{ui}	Input pulse width(2)	40	33		ns
$1/t_{ui}$	Signaling rate(2)	0	30	25	Mbps
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
T_A	Operating temperature	–55		175	°C

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.
(2) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC1}	25 Mbps	V_I = V_{CC} or 0 V, no load		12	22	mA
I_{CC2}	25 Mbps	V_I = V_{CC} or 0 V, no load		12	22	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}			11	µA
I_{IL}	Low-level input current	IN from 0 V to V_{CC}	–11			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 3	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	See Figure 1	21	32	43	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$(1)	See Figure 1		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	5	ns
t_r	Output signal rise time	See Figure 1		1		ns
t_f	Output signal fall time	See Figure 1		1		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	25 Mbps		V_I = V_{CC} or 0 V, no load		12	22	mA
I_{CC2}	25 Mbps		V_I = V_{CC} or 0 V, no load		6	12	mA
V_{OH}	High-level output voltage	(5-V side)	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			11	µA
I_{IL}	Low-level input current		IN from 0 V to V_{CC}	–11			µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay		24	36	49	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)			1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	10	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time	See Figure 1		2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	25 Mbps		V_I = V_{CC} or 0 V, no load		6	12	mA
I_{CC2}	25 Mbps		V_I = V_{CC} or 0 V, no load		12	22	mA
V_{OH}	High-level output voltage	(3.3-V side)	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		IOL = 4 mA, See Figure 1			0.4	
			IOL = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			11	µA
I_{IL}	Low-level input current		IN from 0 V or V_{CC}	–11			µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERTAION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay		24	36	49	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)			1	3	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	10	ns
t_r	Output signal rise time	See Figure 1		1		
t_f	Output signal fall time			1		
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC1}	25 Mbps	V_I = V_{CC} or 0 V, no load		6	12	mA
I_{CC2}	25 Mbps	V_I = V_{CC} or 0 V, no load		6	12	mA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4	3		V
		I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			11	µA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–11			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

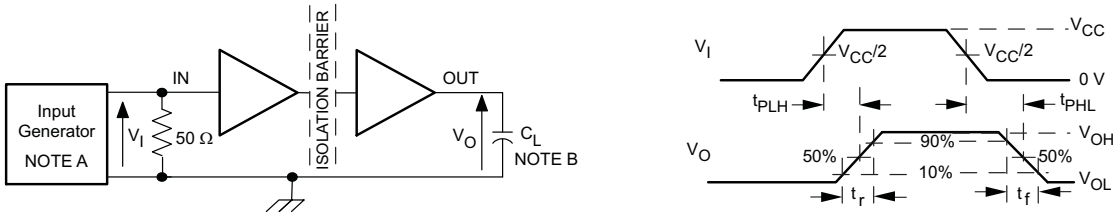
SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay		25	40	53	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)			1	3	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time	See Figure 1		2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

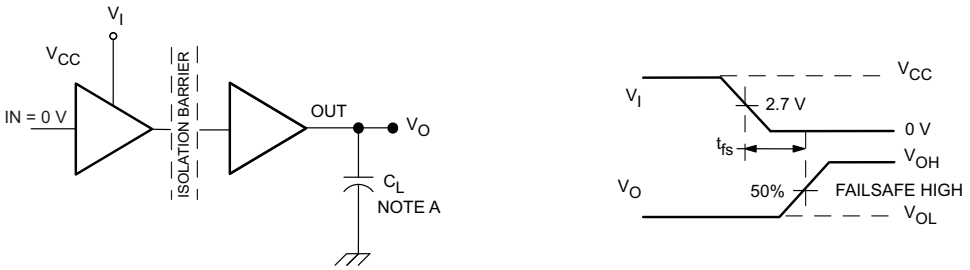
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

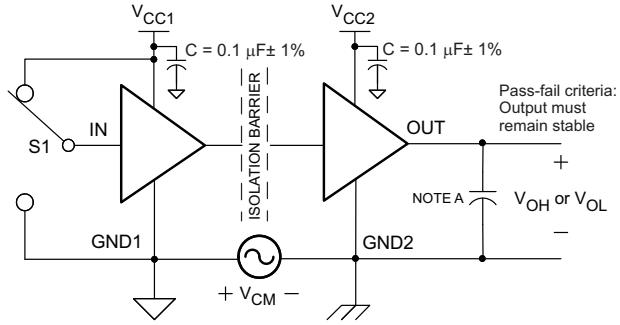
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



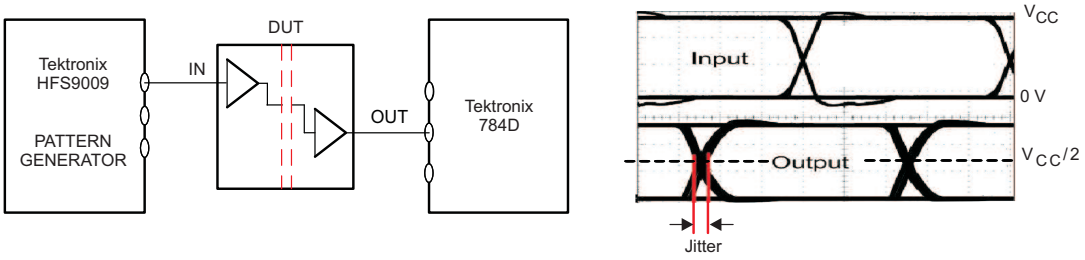
A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

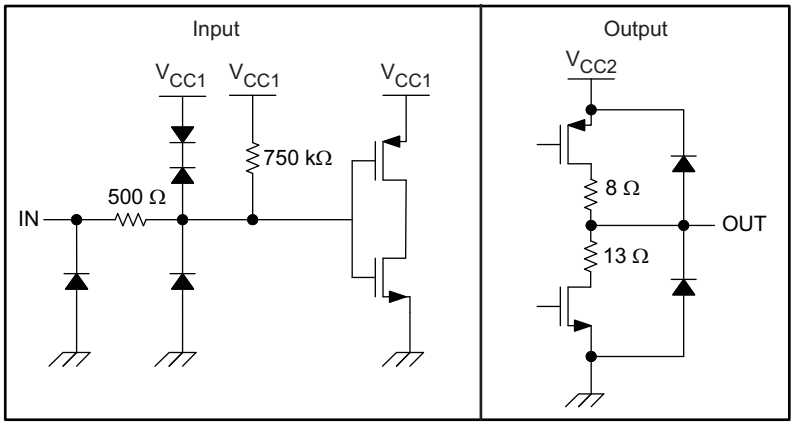


NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps.

Figure 4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

DEVICE I/O SCHEMATICS



SOIC-8 PACKAGE THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		212		°C/W
		High-K Thermal Resistance		122		
θ_{JB}	Junction-to-Board Thermal Resistance			37		
θ_{JC}	Junction-to-Case Thermal Resistance			69.1		

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

DEVICE FUNCTION TABLE

Table 1. Function Table(1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up(Vcc ≥ 3.0V); PD = Powered Down (Vcc ≤ 2.5V); X = Irrelevant; H = High Level; L = Low Level

TYPICAL CHARACTERISTIC CURVES

3.3-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

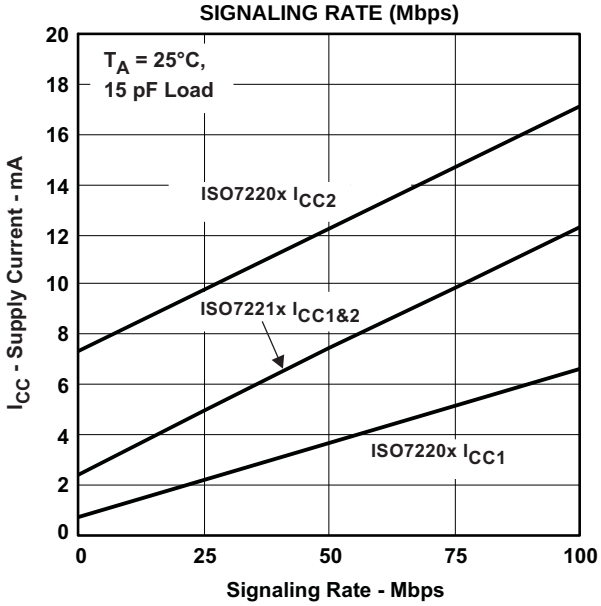


Figure 5.

5-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

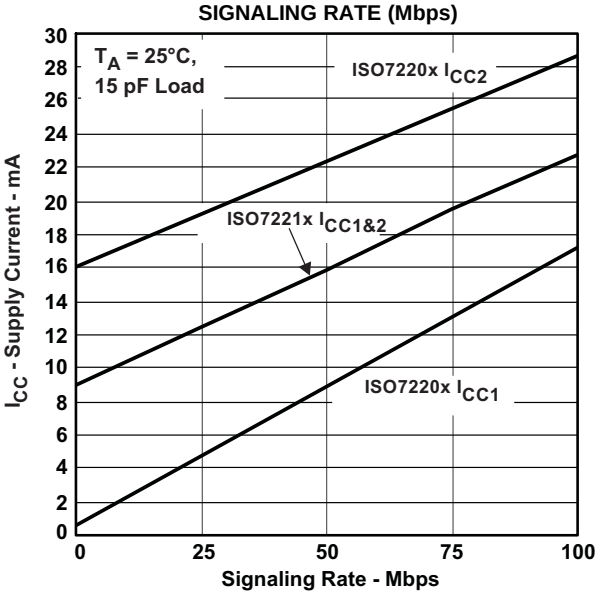


Figure 6.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE

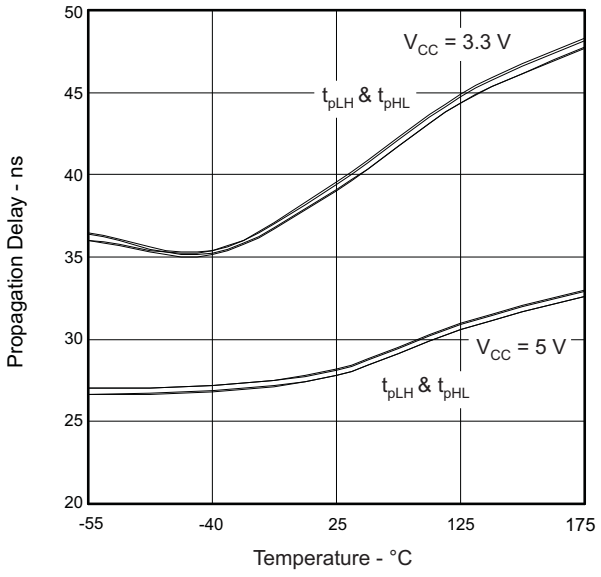


Figure 7.

INPUT VOLTAGE LOW-TO-HIGH SWITCHING THRESHOLD vs FREE-AIR TEMPERATURE

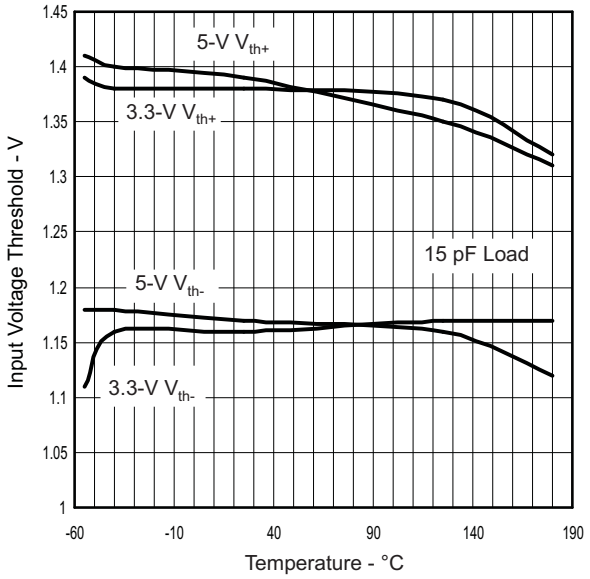


Figure 8.

TYPICAL CHARACTERISTIC CURVES (continued)

V_{CC} FAILSAFE THRESHOLD vs FREE-AIR TEMPERATURE

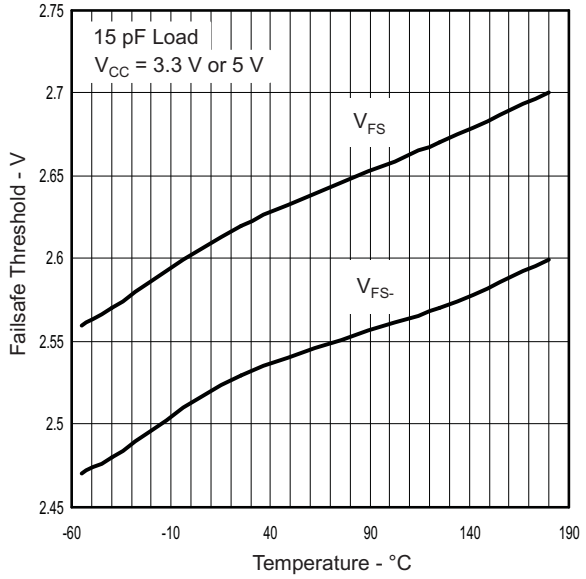


Figure 9.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

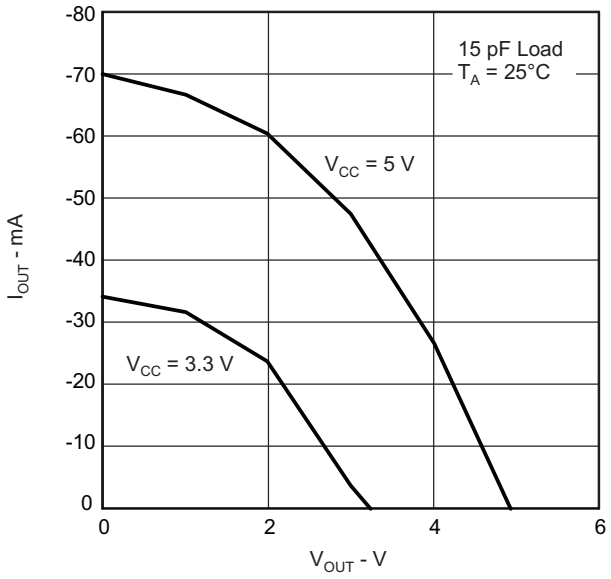


Figure 10.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

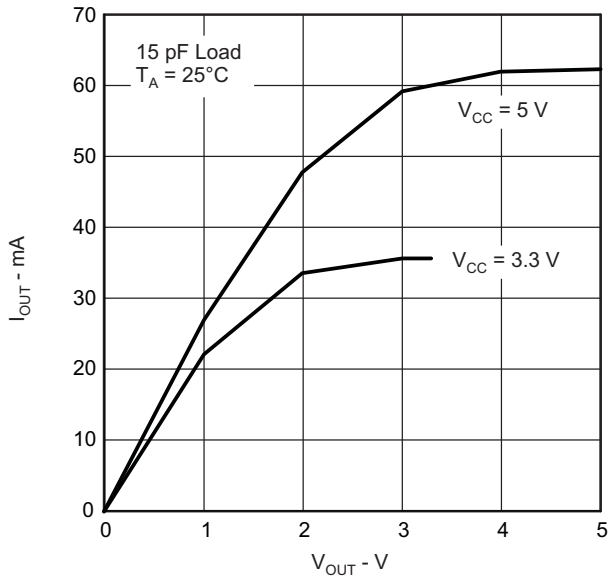


Figure 11.

APPLICATION INFORMATION

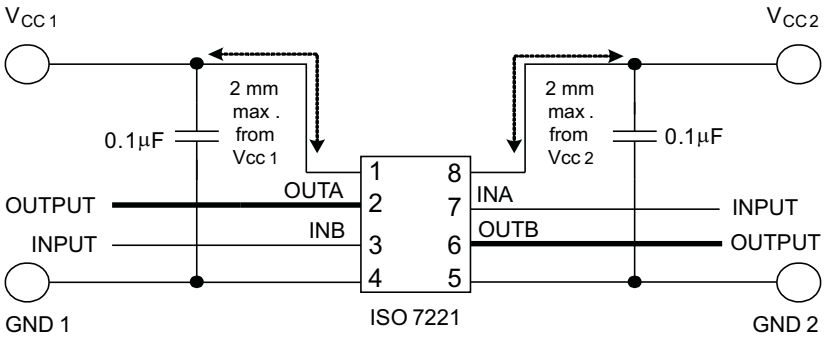
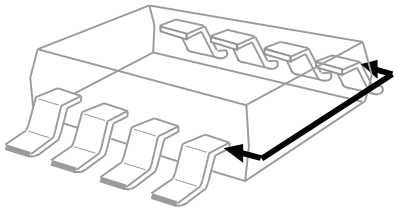


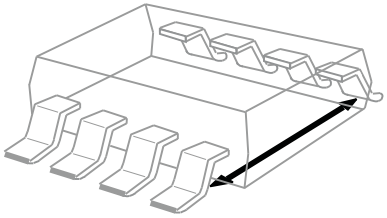
Figure 12. Typical ISO7221 Application Circuit

ISOLATION GLOSSARY

Creepage Distance — The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance — The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to Output Barrier Capacitance — The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to Output Barrier Resistance — The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit — An internal circuit directly connected to an external supply mains or other equivalent source which supplies the primary circuit electric power.

Secondary Circuit — A circuit with no direct connection to primary power, and derives its power from a separate isolated source.

Comparative Tracking Index (CTI) — CTI is an index used for electrical insulating materials which is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Insulation:

Operational insulation — Insulation needed for the correct operation of the equipment.

Basic insulation — Insulation to provide basic protection against electric shock.

Supplementary insulation — Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation — Insulation comprising both basic and supplementary insulation.

Reinforced insulation — A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1 — No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 — Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3 — Conductive pollution occurs or dry nonconductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 – Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category — This section is directed at insulation co-ordination by identifying the transient overvoltages which may occur, and by assigning 4 different levels as indicated in IEC 60664.

I: Signal Level — Special equipment or parts of equipment.

II: Local Level — Portable equipment etc.

III: Distribution Level — Fixed installation

IV: Primary Supply Level — Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7221CHD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 175	I7221H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

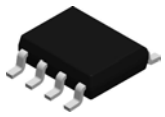
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7221C-HT :

- Catalog: ISO7221C
- Automotive: ISO7221C-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

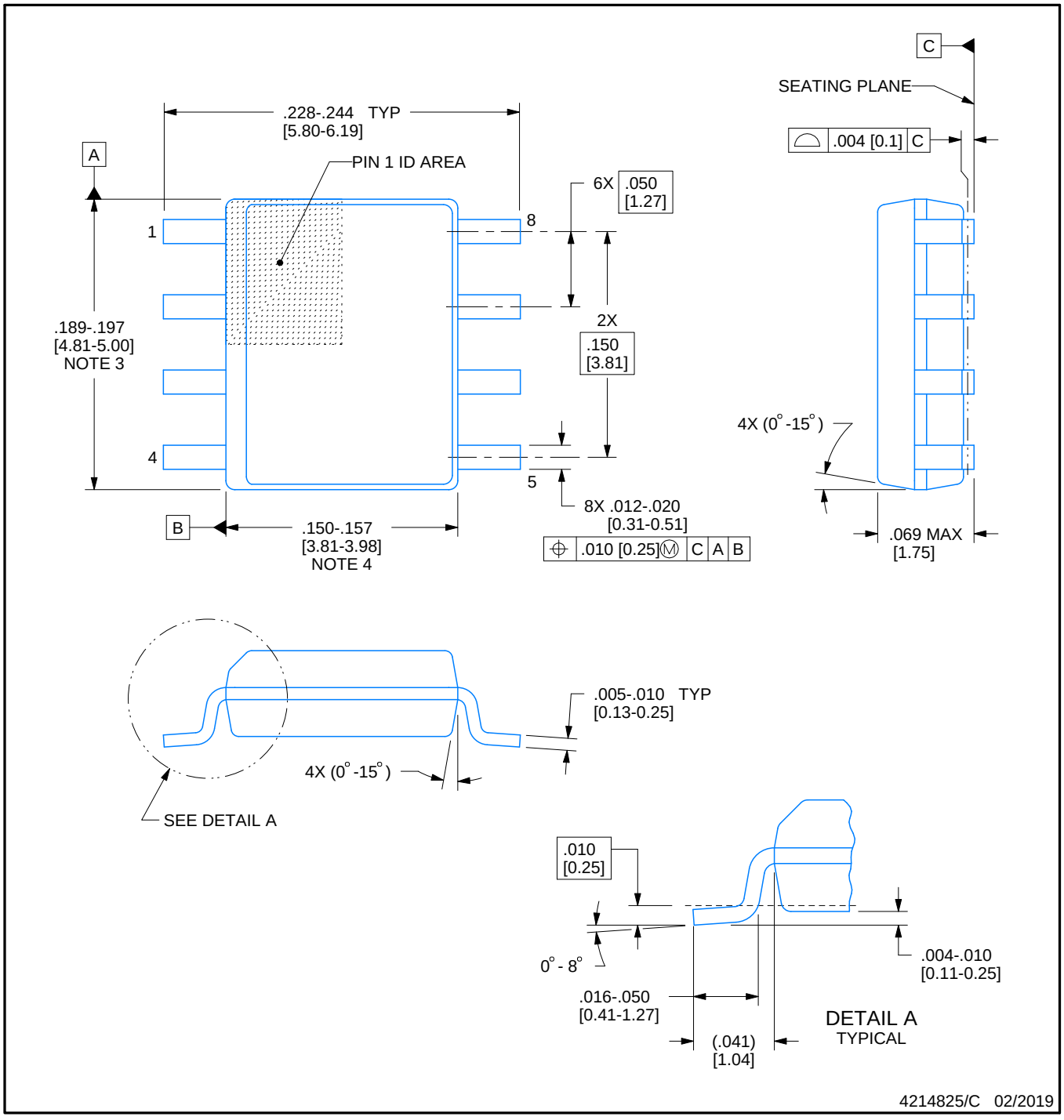


PACKAGE OUTLINE

D0008A

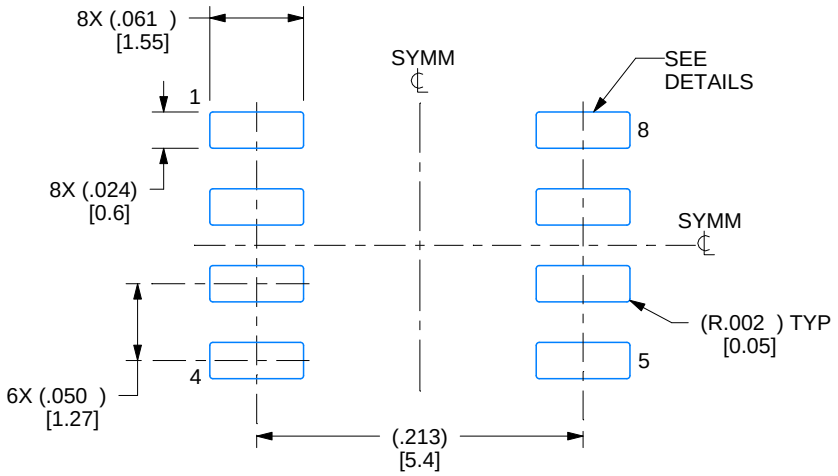
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

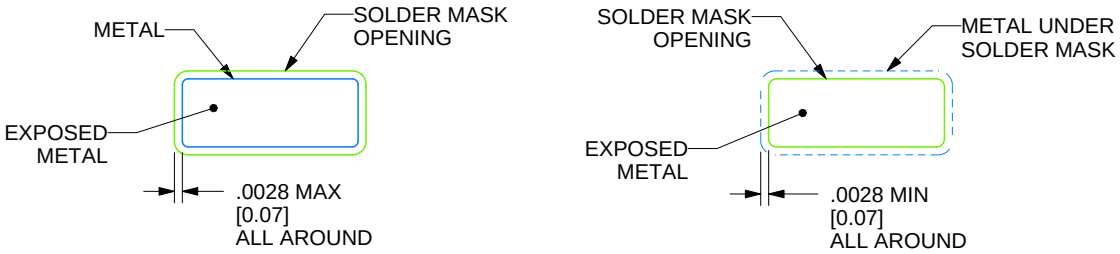


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

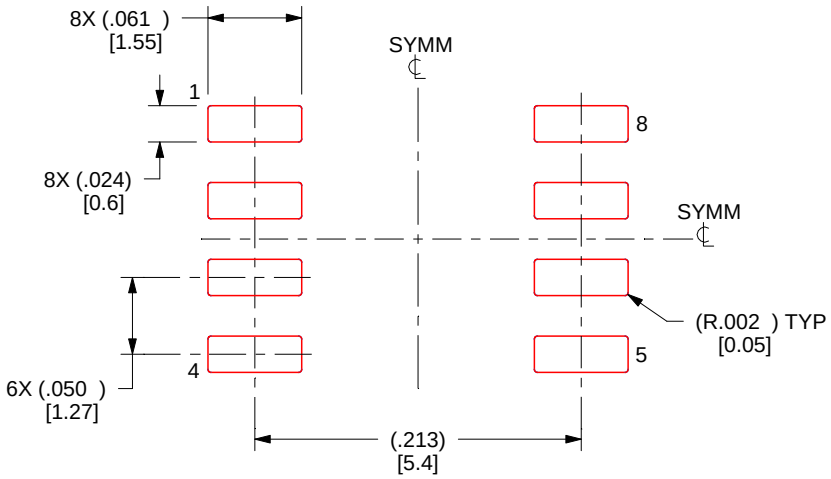
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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