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November 2013

# FQP4N80

# N-Channel QFET $^{\circledR}$ MOSFET 800 V, 3.9 A, 3.6 $\Omega$

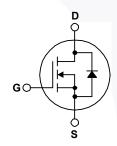
### **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

#### **Features**

- 3.9 A, 800 V,  $R_{DS(on)}$  = 3.6  $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_{D}$  = 1.95 A
- Low Gate Charge (Typ. 19 nC)
- · Low Crss (Typ. 8.6 pF)
- · 100% Avalanche Tested





# Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQP4N80	Unit	
V <sub>DSS</sub>	Drain-Source Voltage		800	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C	.)	3.9	А	
	- Continuous (T <sub>C</sub> = 100°	C)	2.47	А	
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	15.6	Α	
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	460	mJ	
I <sub>AR</sub>	Avalanche Current	(Note 1)	3.9	A	
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	13	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.0	V/ns	
$P_{D}$	Power Dissipation (T <sub>C</sub> = 25°C)		130	W	
	- Derate above 25°C		1.04	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C	

# **Thermal Characteristics**

Symbol	Parameter	FQP4N80	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.96	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP4N80	FQP4N80	TO-220	Tube	N/A	N/A	50 units

# **Electrical Characteristics**

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	800			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.95		V/°C
I <sub>DSS</sub>	5	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V			10	μΑ
Zero Gate Voltage Drain Current	V <sub>DS</sub> = 640 V, T <sub>C</sub> = 125°C			100	μΑ	
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	-		100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	aracteristics		ı	1		
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.95 A		2.8	3.6	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.95 A		3.8		S
C <sub>iss</sub>	ic Characteristics Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		680	880	pF
C <sub>oss</sub>	Output Capacitance			75	100	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			8.6	12	pF
Switchi	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 3.9 \text{ A},$		16	40	ns
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 25 \Omega$		45	100	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	116 - 20 32		35	80	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	/	35	80	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 640 V, I <sub>D</sub> = 3.9 A,		19	25	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V	/	4.2		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		9.1		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				3.9	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F				15.6	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.9 A			1.4	V
			1			

# $Q_{rr}$

 $t_{rr}$ 

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature. 2. L = 57 mH, I $_{AS}$  = 3.9 A, V $_{DD}$  = 50 V, R $_{G}$  = 25  $\Omega$ , starting T $_{J}$  = 25°C. 3. I $_{SD}$   $\leq$  3.9 A, di/dt  $\leq$  200 A/ $\mu$ s, V $_{DD}$   $\leq$  BV $_{DSS}$ , starting T $_{J}$  = 25°C . 4. Essentially independent of operating temperature.

Reverse Recovery Time

Reverse Recovery Charge

ns

μС

575

3.65

 $V_{GS} = 0 \text{ V}, I_{S} = 3.9 \text{ A},$ 

 $dI_F / dt = 100 A/\mu s$ 

# **Typical Characteristics**

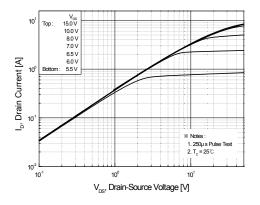


Figure 1. On-Region Characteristics

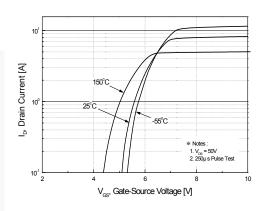


Figure 2. Transfer Characteristics

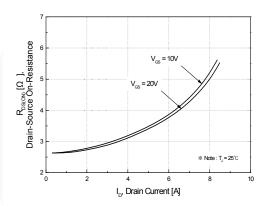


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

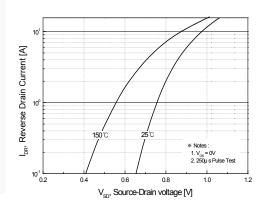


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

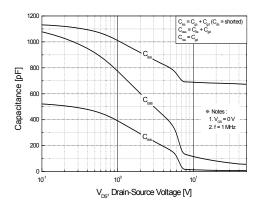


Figure 5. Capacitance Characteristics

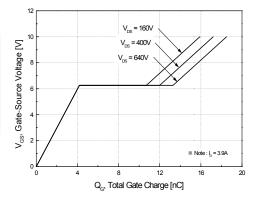
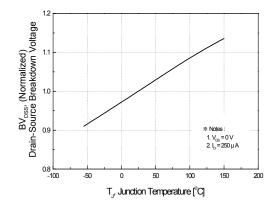


Figure 6. Gate Charge Characteristics

# Typical Characteristics (continued)



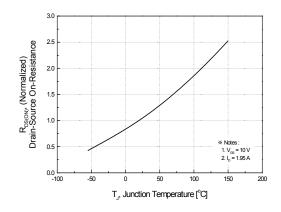
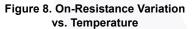
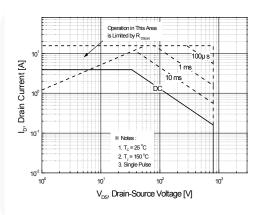


Figure 7. Breakdown Voltage Variation vs. Temperature





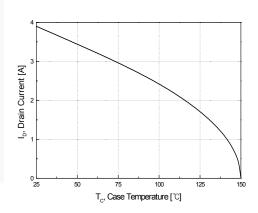


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

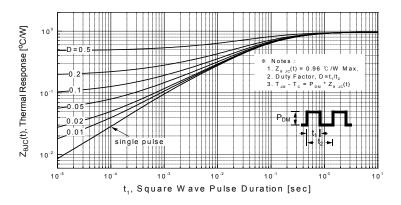


Figure 11. Transient Thermal Response Curve

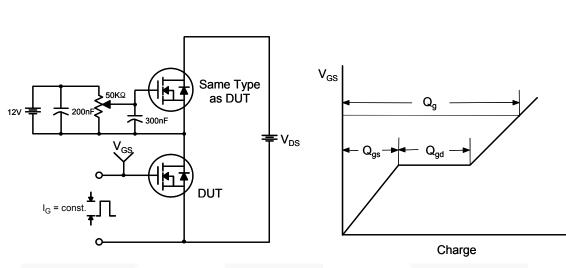


Figure 12. Gate Charge Test Circuit & Waveform

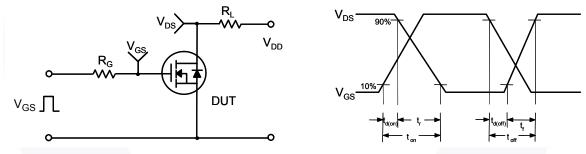


Figure 13. Resistive Switching Test Circuit & Waveforms

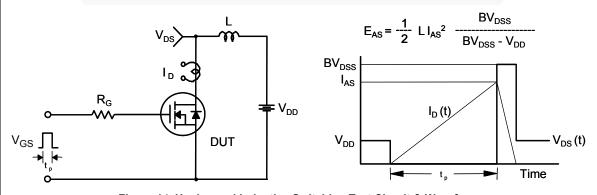
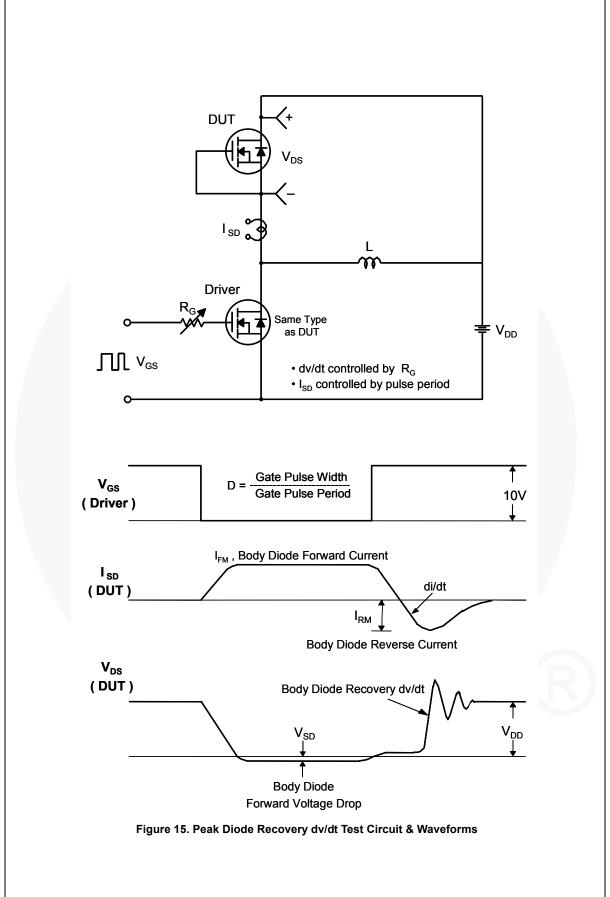


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



# **Mechanical Dimensions**

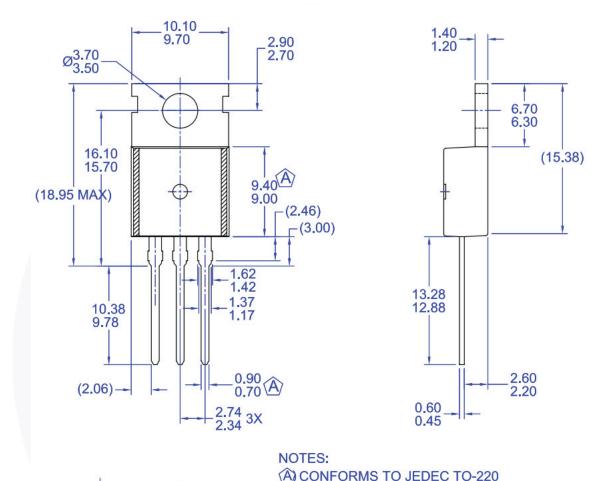


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

VARIATION AB EXCEPT WHERE NOTED

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

B) ALL DIMENSIONS ARE IN MILLIMETERS.

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10.20

9.80

4.70

4.30





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