LOCO™ PLL CLOCK MULTIPLIER

ICS503

Description

The ICS503 is a member of the LOCO™ family, the most cost effective way to generate a high-quality, high frequency clock output from a lower frequency crystal or clock input. The name LOCO stands for Low Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 160 MHz.

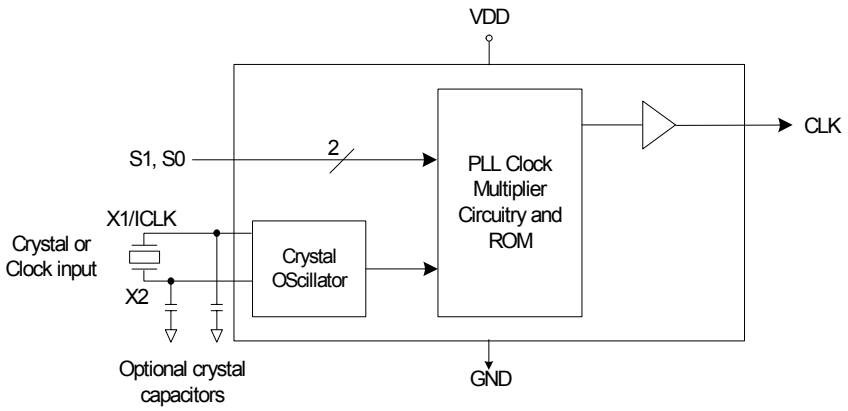
Stored in the chip's ROM is the ability to generate nine different multiplication factors, allowing one chip to output many common frequencies (see table on page 2).

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined or guaranteed. For applications which require defined input to output skew, use the ICS570B.

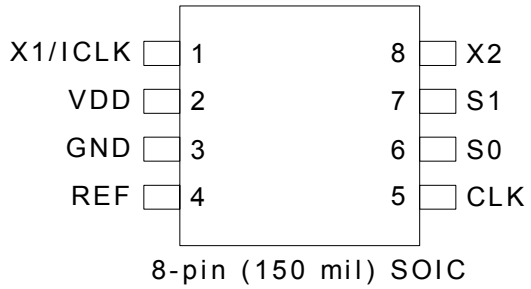
Features

- Packaged as 8-pin SOIC (Pb-free) or die
- IDT's lowest cost PLL clock
- Generates 16.9344 MHz for stereo codecs from the 14.31818 MHz motherboard clock.
- Can be cost effective in replacing a single surface-mount crystal
- Can be driven by other 5xx series
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 160 MHz
- Low jitter - 50 ps one sigma
- Duty cycle of 45/55 up to 160 MHz
- Operating voltages of 3.0 to 5.5V
- 25 mA drive capability at TTL levels
- Advanced, low power CMOS process

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC

Clock Decoding Table (MHz)

S1	S0	Multiplier	Typ. Input (MHz)	CLK (MHz)	Input Range (MHz) at 5.0 V	Input Range (MHz) at 3.3 V
0	0	10	10	100	2 ≤ Input ≤ 16	2 ≤ Input ≤ 16
0	M	16	10	160	2 ≤ Input ≤ 10	2 ≤ Input ≤ 6
0	1	1.1111	27	30	20 ≤ Input ≤ 50	20 ≤ Input ≤ 40
M	0	2.4444	14.31818	35	10 ≤ Input ≤ 50	10 ≤ Input ≤ 40
M	M	2.4164	14.31818	34.60	10 ≤ Input ≤ 50	10 ≤ Input ≤ 40
M	1	2.4	14.31818	34.36	10 ≤ Input ≤ 50	10 ≤ Input ≤ 40
1	0	5.5873	14.31818	80	14 ≤ Input ≤ 28	14 ≤ Input ≤ 18
1	M	1.1827	14.31818	16.934	14 ≤ Input ≤ 30	14 ≤ Input ≤ 30
1	1	4.1905	14.31818	60	5 ≤ Input ≤ 38	5 ≤ Input ≤ 24

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI/ICLK	Input	Crystal connection or clock input.
2	VDD	Power	Connect to +3.3 V or +5 V.
3	GND	Power	Connect to ground.
4	NC	—	No connect. Do not connect anything to this pin.
5	CLK	Output	Clock output per table above. Output frequency equals input freuency times multiplier.
6	S0	Tri-level Input	Select 0 for output clock. Connect to GND or VDD or float.
7	S1	Tri-level Input	Select 1 for output clock. Connect to GND or VDD or float.
8	X2	Output	Crystal connection. Leave unconnected for clock input.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS503 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and GND. It must be connected close to the ICS503 to minimize lead inductance. No external power supply filtering is required for the ICS503.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the CLK pin. The total on-chip capacitance is approximately 12 pF. A parallel resonant, fundamental mode crystal should be used.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -12 pF)*2. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF [(16-12) x 2] = 8.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS503. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+70	° C
Power Supply Voltage (measured in respect to GND)	+3		+5.5	V

DC Electrical Characteristics

VDD=5.0 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3		5.5	V
Input High Voltage, ICLK only	V_{IH}	ICLK (pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, ICLK only	V_{IL}	ICLK (pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage	V_{IH}	S0, S1	VDD-0.5			V
Input Mid Voltage	V_{IM}	S1, S0		VDD/2		V
Input Low Voltage	V_{IL}	S0, S1			0.5	V
Output High Voltage, CMOS high	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage, CMOS high	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
IDD Operating Supply Current, 14 MHz crystal		No load, 80 MHz		16		mA
Short Circuit Current		CLK output		±70		mA
Input Capacitance, S1, S0		Pins 6, 7		4		pF

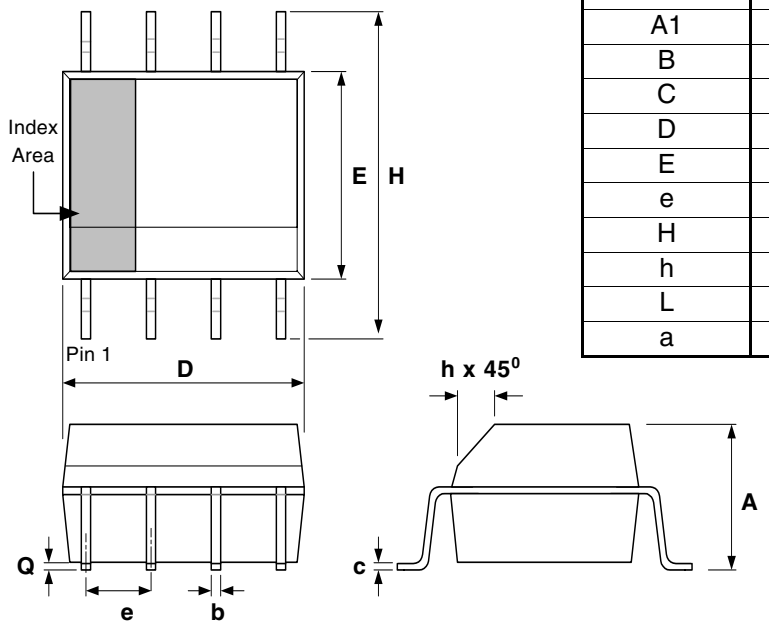
AC Electrical Characteristics

VDD = 5.0V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	F_{IN}		5		27	MHz
Input Frequency, clock input	F_{IN}		2		50	MHz
Output Frequency, VDD = 4.5 to 5.5V	F_{OUT}		14		160	MHz
Output Frequency, VDD = 3.0 to 3.6V			14		100	MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V		1		ns
Output Clock Fall Time	t_{OF}	2.0 to 8.0V		1		ns
Output Clock Duty Cycle	t_{OD}	at VDD/2	45	49-51	55	%
Absolute Clock Period Jitter	t_{ja}	Deviation from mean		±100		ps
One Sigma Clock Period Jitter	t_{js}			30		ps

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	1.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	0.1497	0.1574
e	1.27 Basic		0.050 Basic	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
a	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
503MLF	503MLF	Tubes	8 pin SOIC	0 to +70° C
503MLFT	503MLF	Tape and Reel	8 pin SOIC	0 to +70° C

“LF” denotes Pb-free packaging, RoHS compliant.

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