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FDP047N10 N-Channel PowerTrench[®] MOSFET 100 V, 164 A, 4.7 m Ω

Features

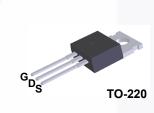
- $R_{DS(on)}$ = 3.9 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 75 A
- · Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$
- High Power and Current Handling Capability
- RoHS Compliant

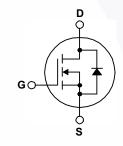
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDP047N10	Unit
V _{DSS}	Drain to Source Voltage			100	V
V _{GSS}	Gate to Source Voltage			±20	V
	Drain Current -	Continuous ($T_C = 25^{\circ}C$, Sili	con Limited)	164*	Α
ID	-	con Limited)	116*	А	
	-	ckage Limited)	120	Α	
I _{DM}	Drain Current	- Pulsed	(Note 1)	656*	Α
E _{AS}	Single Pulsed Avalanche Energy (Note		(Note 2)	1153	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		(Note 3)	6.0	V/ns
P _D	Devuer Dissinction	(T _C = 25 ^o C)		375	W
	Power Dissipation	- Derate Above 25°C	- Derate Above 25°C		W/ºC
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +175	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

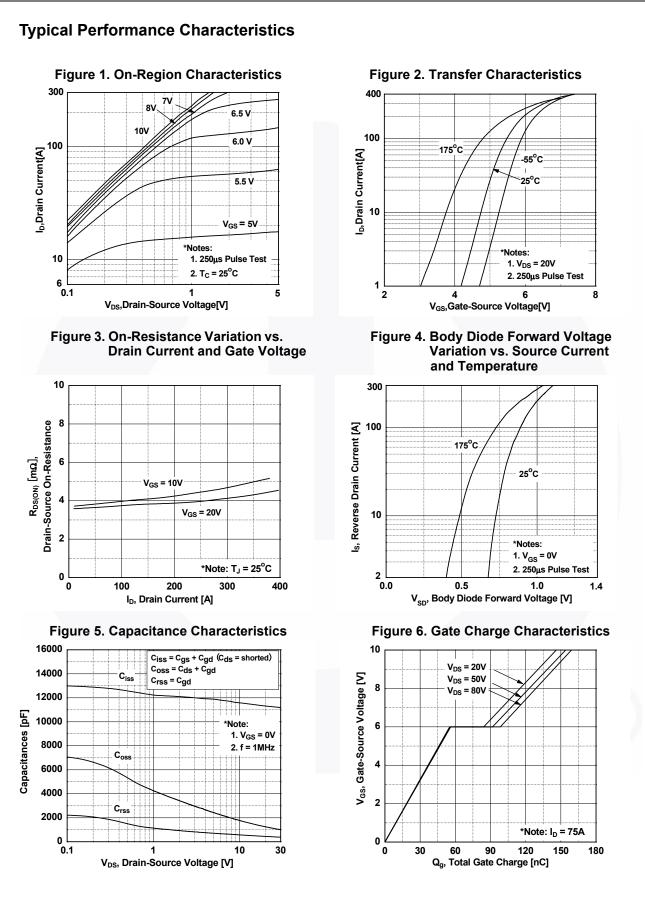
Symbol	Parameter	FDP047N10	Unit
$R_{ extsf{ heta}JC}$	_{eJC} Thermal Resistance, Junction to Case, Max.		°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	°C/vv

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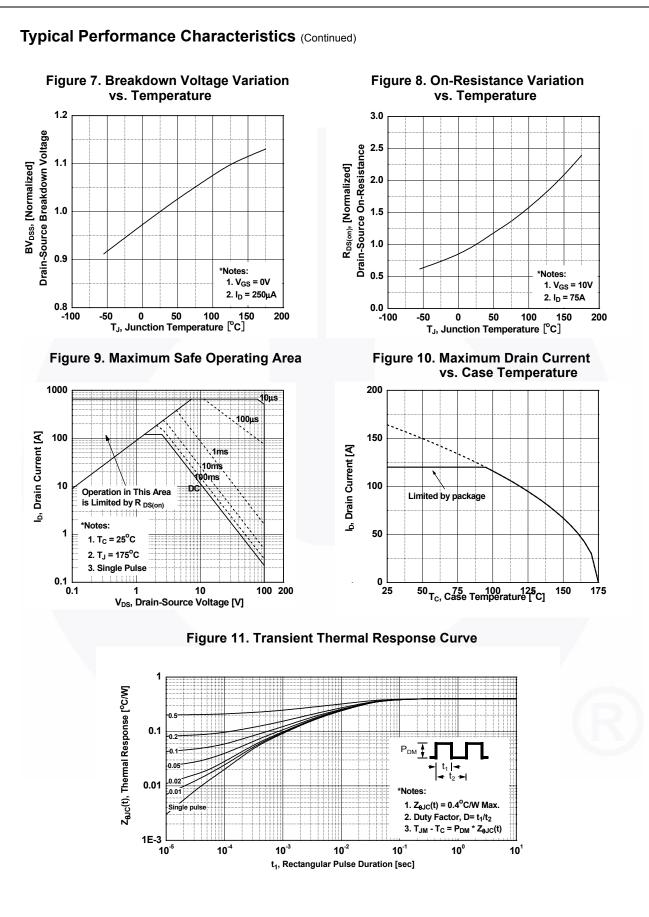
November 2013

		Package	Packing Method	Reel Size	Тар	e Width	Qua	ntity	
		TO-220	220 Tube N/A		N/A		50 units		
Electrical	Char	acteristics T _C = 25°0	C unless otl	nerwise noted.					
Symbol		Parameter		Test Conditio	ons	Min.	Тур.	Max.	Unit
Off Charact	eristic	s							
BV _{DSS}	1	Source Breakdown Voltag	e li	_D = 250 μA, V _{GS} = 0 V,	$T_1 = 25^{\circ}C_1$	100	-	-	V
∆BV _{DSS}		own Voltage Temperature				100			
$/\Delta T_J$	Coefficie		I.	$_{\rm D}$ = 250 μ A, Reference	d to 25°C	-	0.1	-	V/ºC
	Zoro Gr	Zana Cata Maltana Dusia Cumant		$\frac{V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}}{V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{C} = 150^{\circ}\text{C}}$		-	-	1	
DSS	Zero Gate Voltage Drain Current		V			-	-	500	μA
GSS	Gate to	Body Leakage Current	V	V _{GS} = ±20 V, V _{DS} = 0 V		-	-	±100	nA
On Charact	eristic	S							
V _{GS(th)}	Gate Th	nreshold Voltage	١	/ _{GS} = V _{DS} , I _D = 250 μA		2.5	3.5	4.5	V
R _{DS(on)}	Static D	rain to Source On Resistar		$I_{GS} = 10 \text{ V}, I_{D} = 75 \text{ A}$		-	3.9	4.7	mΩ
9FS	Forward	d Transconductance	١	V _{DS} = 10 V, I _D = 75 A		-	170	-	S
C _{iss} C _{oss} C _{rss}	Output (apacitance Capacitance e Transfer Capacitance		V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		-	11500 1120 455	15265 1500 680	pF pF pF
Switching (Charac	teristics	, i		·				
t _{d(on)}	1	Delay Time		V _{DD} = 50 V, I _D = 75 A, V _{GS} = 10 V, R _G = 25 Ω		-	174	358	ns
t _r	Turn-On	Rise Time	\ \			-	386	782	ns
t _{d(off)}	Turn-Off	f Delay Time	\ \			-	344	698	ns
t _f		f Fall Time			(Note 4)	-	244	499	ns
Q _{g(tot)}	Total Ga	te Charge at 10V	,			-	160	210	nC
Q _{gs}		Source Gate Charge		/ _{DS} = 80 V, I _D = 75 A, / _{GS} = 10 V	_	-	56	-	nC
Q _{gd}	Gate to	Drain "Miller" Charge		(Note 4)		-	36	-	nC
	ce Dioc	e Characteristics			I			1	
I _S	Maximum Continuous Drain to Source Diode Forward Current					-	-	164*	Α
I _{SM}	Maximum Pulsed Drain to Source Diode					-	-	656	Α
V _{SD}		Source Diode Forward Vol				-	-	1.25	V
t _{rr}		Recovery Time		$V_{GS} = 0 V, I_{SD} = 75 A,$ dI _F /dt = 100 A/µs		-	88	-	ns
	Reverse	Recovery Charge				-	245	/ -	nC
Q _{rr}							1		1

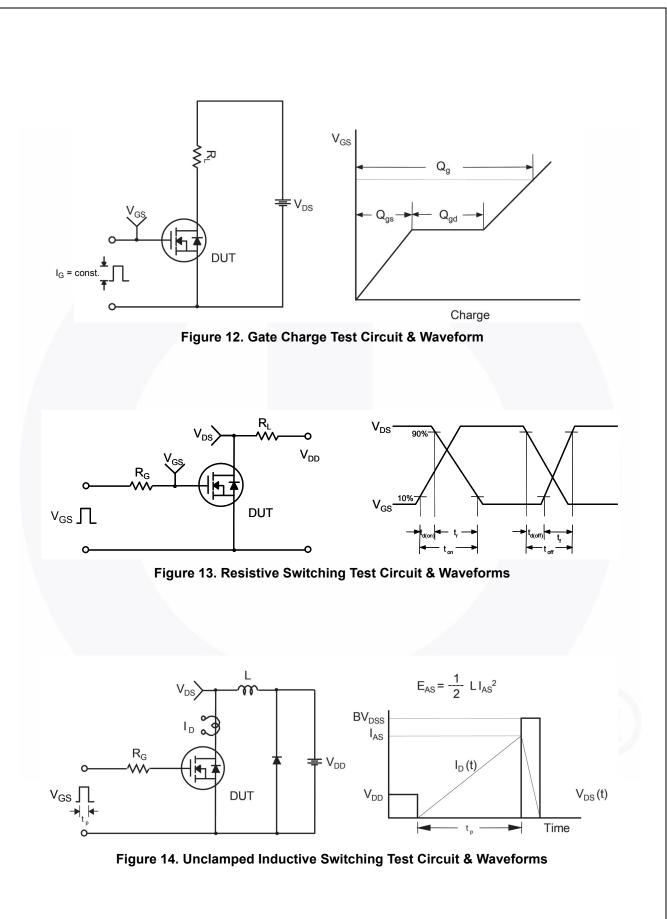
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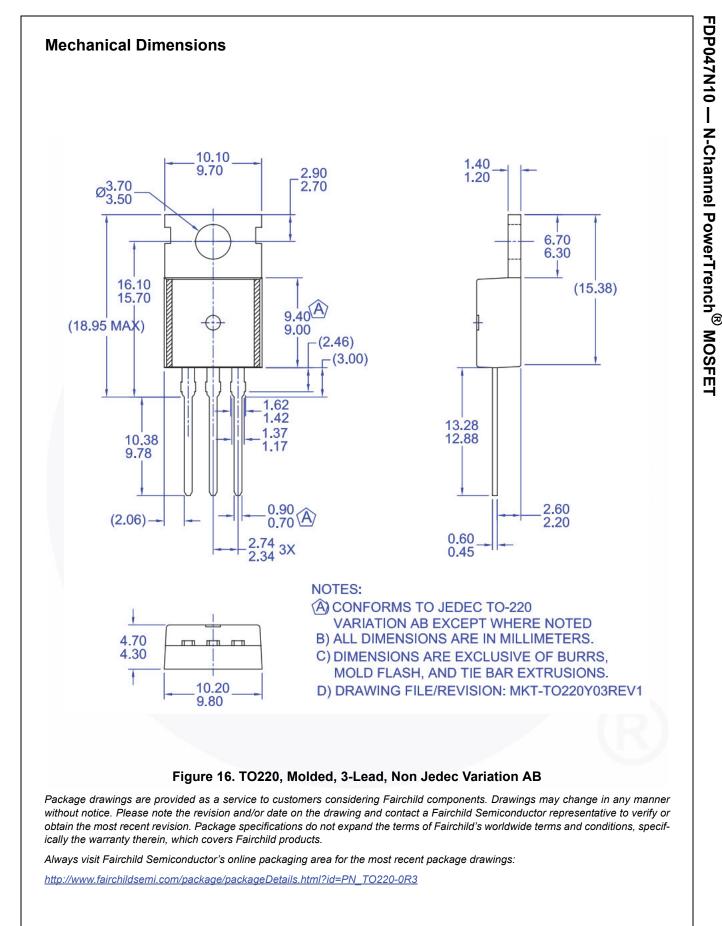
FDP047N10 — N-Channel PowerTrench[®] MOSFET



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DUT + v_{DS} a ۱_{SD} م L Driver R_G, Same Type as DUT L F ∨_{DD} $\prod V_{GS}$ • dv/dt controlled by R_{G} • I_{SD} controlled by pulse period Î Gate Pulse Width V_{GS} D = Gate Pulse Period 10V (Driver) I_{FM}, Body Diode Forward Current I _{SD} di/dt (DUT) I_{RM} Body Diode Reverse Current V_{DS} (DUT) Body Diode Recovery dv/dt V_{SD} V_{DD} Body Diode Forward Voltage Drop Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

FDP047N10 — N-Channel PowerTrench[®] MOSFET





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