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# FDP047N10 N-Channel PowerTrench<sup>®</sup> MOSFET 100 V, 164 A, 4.7 m $\Omega$

## Features

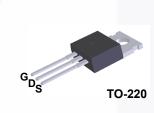
- $R_{DS(on)}$  = 3.9 m $\Omega$  (Typ.) @ V<sub>GS</sub> = 10 V, I<sub>D</sub> = 75 A
- · Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$
- High Power and Current Handling Capability
- RoHS Compliant

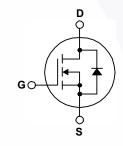
# Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

## Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter





### **MOSFET Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter		FDP047N10	Unit
V <sub>DSS</sub>	Drain to Source Voltage			100	V
V <sub>GSS</sub>	Gate to Source Voltage			±20	V
	Drain Current -	Continuous ( $T_C = 25^{\circ}C$ , Sili	con Limited)	164*	Α
ID	-	con Limited)	116*	А	
	-	ckage Limited)	120	Α	
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	656*	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note		(Note 2)	1153	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		(Note 3)	6.0	V/ns
P <sub>D</sub>	Devuer Dissinction	(T <sub>C</sub> = 25 <sup>o</sup> C)		375	W
	Power Dissipation	- Derate Above 25°C	- Derate Above 25°C		W/ºC
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +175	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

## **Thermal Characteristics**

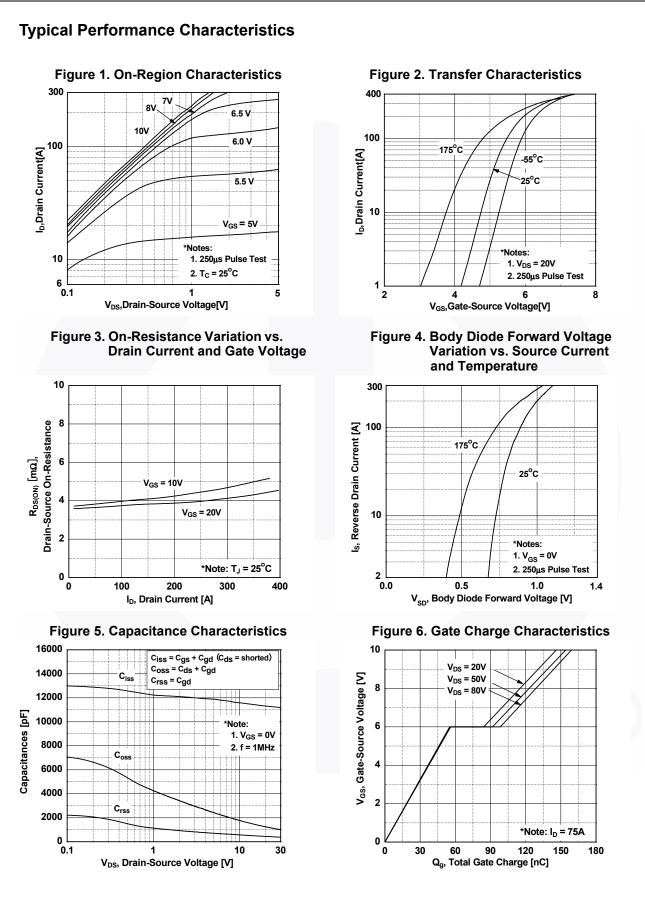
Symbol	Parameter	FDP047N10	Unit
$R_{ extsf{ heta}JC}$	<sub>eJC</sub> Thermal Resistance, Junction to Case, Max.		°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	°C/vv

1

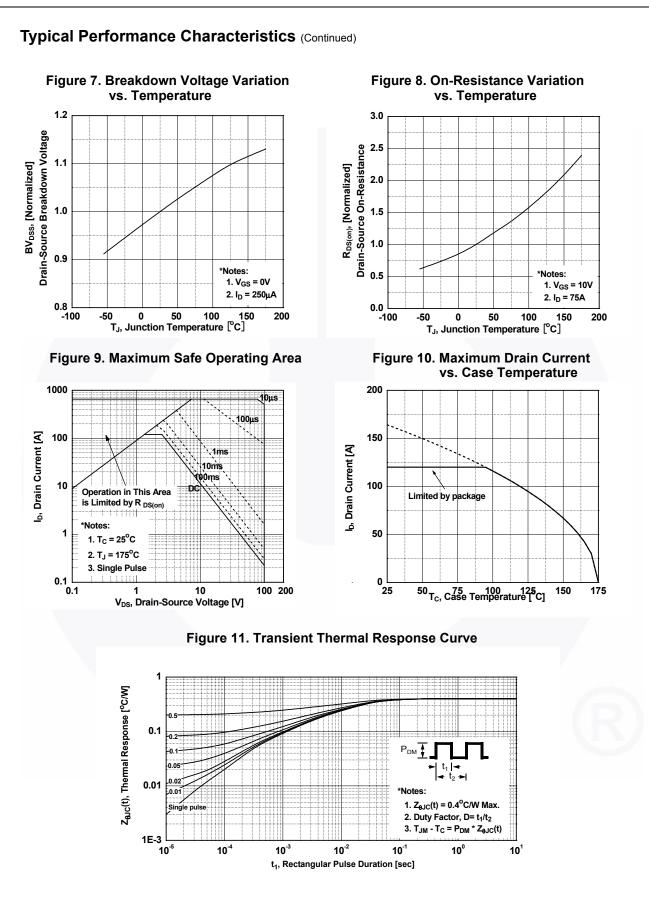
November 2013

		Package	Packing Method	Reel Size	Тар	e Width	Qua	ntity	
		TO-220	220 Tube N/A		N/A		50 units		
Electrical	Char	acteristics T <sub>C</sub> = 25°0	C unless otl	nerwise noted.					
Symbol		Parameter		Test Conditio	ons	Min.	Тур.	Max.	Unit
Off Charact	eristic	s							
BV <sub>DSS</sub>	1	Source Breakdown Voltag	e li	<sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V,	$T_1 = 25^{\circ}C_1$	100	-	-	V
∆BV <sub>DSS</sub>		own Voltage Temperature				100			
$/\Delta T_J$	Coefficie		I.	$_{\rm D}$ = 250 $\mu$ A, Reference	d to 25°C	-	0.1	-	V/ºC
	Zoro Gr	Zana Cata Maltana Dusia Cumant		$\frac{V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}}{V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{C} = 150^{\circ}\text{C}}$		-	-	1	
DSS	Zero Gate Voltage Drain Current		V			-	-	500	μA
GSS	Gate to	Body Leakage Current	V	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V		-	-	±100	nA
On Charact	eristic	S							
V <sub>GS(th)</sub>	Gate Th	nreshold Voltage	١	/ <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA		2.5	3.5	4.5	V
R <sub>DS(on)</sub>	Static D	rain to Source On Resistar		$I_{GS} = 10 \text{ V}, I_{D} = 75 \text{ A}$		-	3.9	4.7	mΩ
9FS	Forward	d Transconductance	١	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 75 A		-	170	-	S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Output (	apacitance Capacitance e Transfer Capacitance		V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		-	11500 1120 455	15265 1500 680	pF pF pF
Switching (	Charac	teristics	, i		·				
t <sub>d(on)</sub>	1	Delay Time		V <sub>DD</sub> = 50 V, I <sub>D</sub> = 75 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 25 Ω		-	174	358	ns
t <sub>r</sub>	Turn-On	Rise Time	\ \			-	386	782	ns
t <sub>d(off)</sub>	Turn-Off	f Delay Time	\ \			-	344	698	ns
t <sub>f</sub>		f Fall Time			(Note 4)	-	244	499	ns
Q <sub>g(tot)</sub>	Total Ga	te Charge at 10V	,			-	160	210	nC
Q <sub>gs</sub>		Source Gate Charge		/ <sub>DS</sub> = 80 V, I <sub>D</sub> = 75 A, / <sub>GS</sub> = 10 V	_	-	56	-	nC
Q <sub>gd</sub>	Gate to	Drain "Miller" Charge		(Note 4)		-	36	-	nC
	ce Dioc	e Characteristics			I			1	
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current					-	-	164*	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode					-	-	656	Α
V <sub>SD</sub>		Source Diode Forward Vol				-	-	1.25	V
t <sub>rr</sub>		Recovery Time		$V_{GS} = 0 V, I_{SD} = 75 A,$ dI <sub>F</sub> /dt = 100 A/µs		-	88	-	ns
	Reverse	Recovery Charge				-	245	/ -	nC
Q <sub>rr</sub>							1		1

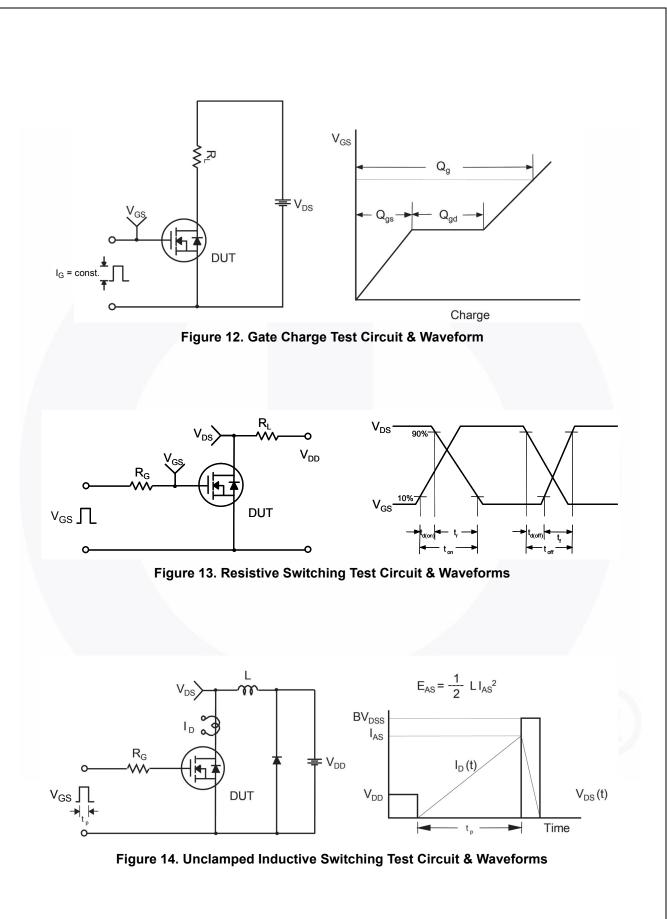
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# ©2008 Fairchild Semiconductor Corporation FDP047N10 Rev. C2



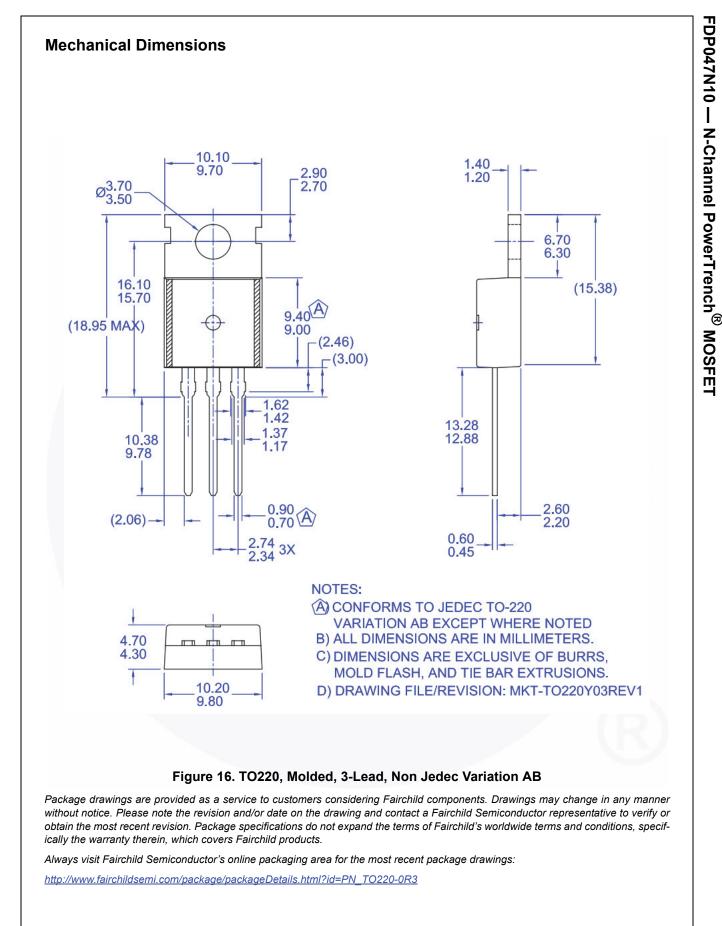
FDP047N10 — N-Channel PowerTrench<sup>®</sup> MOSFET



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DUT +  $v_{DS}$ a ۱<sub>SD</sub> م L Driver R<sub>G</sub>, Same Type as DUT L F ∨<sub>DD</sub>  $\prod V_{GS}$ • dv/dt controlled by  $R_{G}$ • I<sub>SD</sub> controlled by pulse period Î Gate Pulse Width V<sub>GS</sub> D = Gate Pulse Period 10V (Driver) I<sub>FM</sub>, Body Diode Forward Current I <sub>SD</sub> di/dt (DUT)  $I_{RM}$ Body Diode Reverse Current  $V_{DS}$ (DUT) Body Diode Recovery dv/dt  $V_{SD}$ V<sub>DD</sub> Body Diode Forward Voltage Drop Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

FDP047N10 — N-Channel PowerTrench<sup>®</sup> MOSFET





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