EP5348UI 400mA PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EP5348UI delivers the optimal trade-off between footprint and efficiency. It is a perfect alternative to replace less efficient LDOs in space constrained applications that require improved efficiency.

The EP5348UI is a 400mA PowerSoC which integrates MOSFET switches, control, compensation, and the magnetics in a micro-QFN Package. This highly integrated DC-DC solution offers up to 46-points better efficiency than the comparable LDO. A significant reduction in power loss and improved thermals are achieved. It enables extended battery life and helps Meet Energy Star requirements.

Integrated magnetics enables a tiny solution footprint, low output ripple, and high reliability, while maintaining high efficiency. The complete solution size is similar to an LDO and much smaller than a comparable DC-DC.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- Integrated Inductor Technology
- 400mA continuous output current
- 2.0mm x 1.75mm x 0.9mm uQFN package
- Small Solution Footprint
- Efficiency, up to 90%
- V_{OUT} Range 0.6V to $V_{IN} – V_{DROP\_OUT}$
- Short circuit and over current protection
- UVLO and thermal protection
- IC level reliability in a PowerSoC solution

APPLICATIONS

- Applications where poor LDO efficiency creates:
  - Thermal challenges
  - Battery Life challenges
  - Failure to meet Energy Star requirements
- Space-constrained applications
- Portable media players and USB peripherals

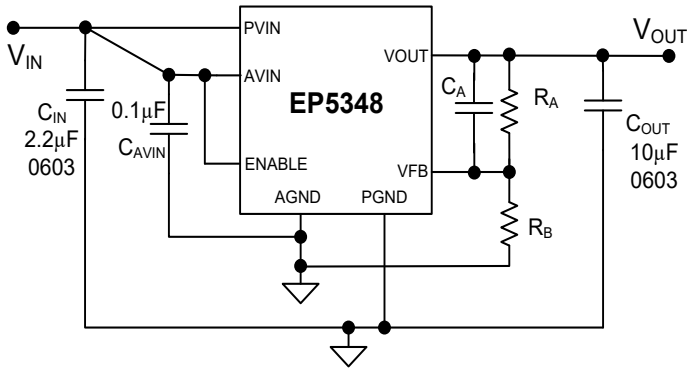


Figure 1: Simplified Applications Circuit

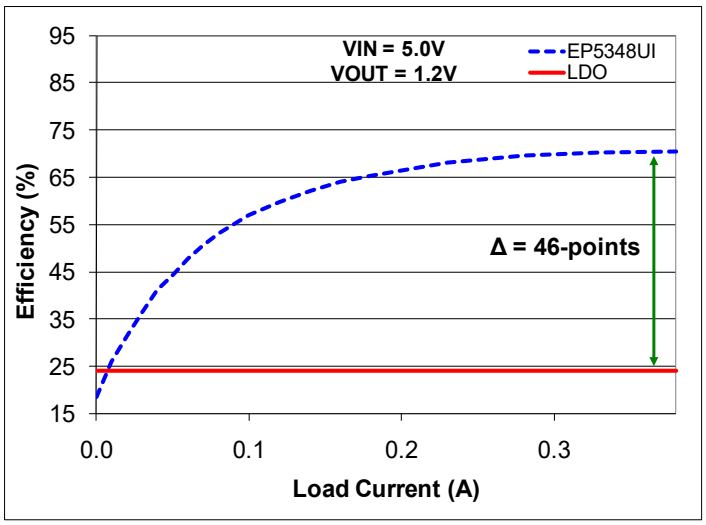


Figure 2: Highest Efficiency in Smallest Solution Size

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EP5348UI	ATXX	-40 to +125	16-pin (2.5mm x 2.25mm x 1.1mm) uQFN
EVB-EP5348UI-E		QFN Evaluation Board	

Packing and Marking Information: https://www.intel.com/content/www/us/en/products/programmable.html

PIN FUNCTIONS

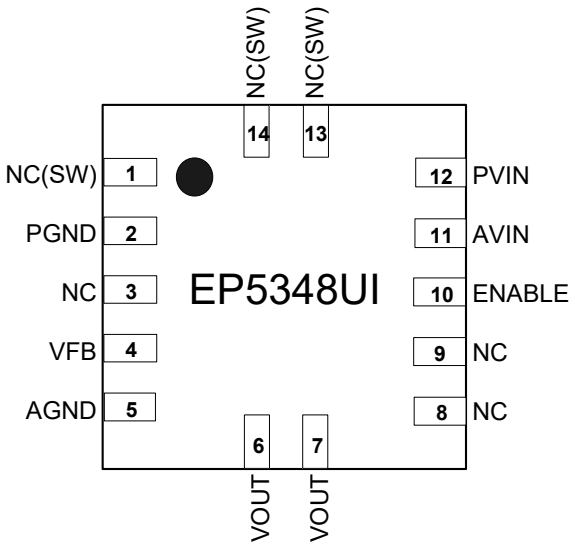


Figure 3: EP5348UI Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Black 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1,15, 14	NC(SW)	Analog	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. NC (SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage to the device.
2	PGND	Ground	Power ground. Connect this pin to the ground electrode of the Input and output filter capacitors.
3, 8, 9	NC	Analog	NO CONNECT: These pins may already be connected inside the device. Therefore, they cannot be electrically connected to each other or to any external signal, voltage, or ground. They must however be soldered to the PCB. Failure to follow this guideline may result in device damage.
4	VFB	Analog	Feedback pin for external voltage divider network.
5	AGND	Analog	Analog ground. This is the quiet ground for the internal control circuitry, and the ground return for external feedback voltage divider
6, 7	VOUT	Power	Regulated Output Voltage. Refer to application section for proper layout and decoupling.
10	ENABLE	Analog	Output Enable. Enable = logic high; Disable = logic low
11	AVIN	Power	Input power supply for the controller circuitry. Connect to VIN at a quiet point.
12	PVIN	Power	Input Voltage for the MOSFET switches.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage PVIN, AVIN, VOUT		-0.3	6.0	V
Voltages on: ENABLE		-0.3	VIN+ 0.3	V
Voltages on: VFB		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature	T_{J-ABS}		+150	°C
Storage Temperature Range	T_{STG}	-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	VIN	2.4	5.5	V
Output Voltage Range	VOUT	0.6	$V_{IN} - V_{DO}$ (1)	V
Operating Ambient Temperature	TA	-40	+85	°C
Operating Junction Temperature	TJ	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	155	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	15	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	105	°C/W

(1) V_{DO} (dropout voltage) is defined as (I_{LOAD} x Droput Resistance). Please refer to Electrical Characteristics Table.

(2) Based on 2 oz. external copper layers and proper thermal design in line with EIA/JEDEC JESD51-7 standard for high effective thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VIN = 3.6V.

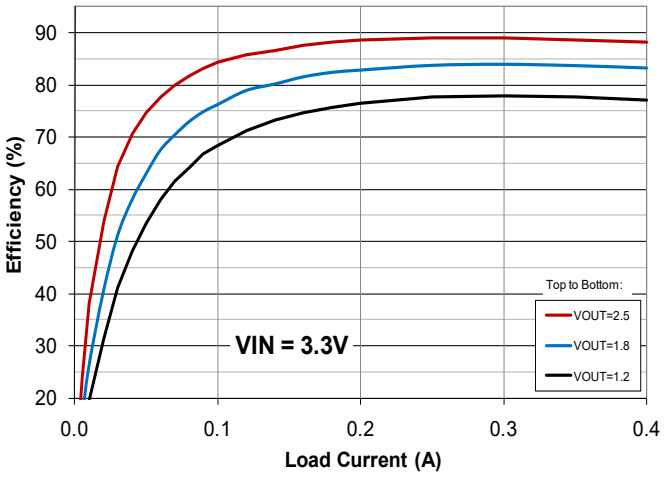
C_{IN} = 2.2µF 0603 MLCC, C_{OUT} = 10µF 0603.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage Range	V_{IN}		2.5		5.5	V
Under Voltage Lock-out – VIN Rising	V_{UVLO_R}			2.3		V
Under Voltage Lock-out – VIN Falling	V_{UVLO_F}			2.2		V
Shut-down Current	I_{SD}	Enable = Low		3		µA

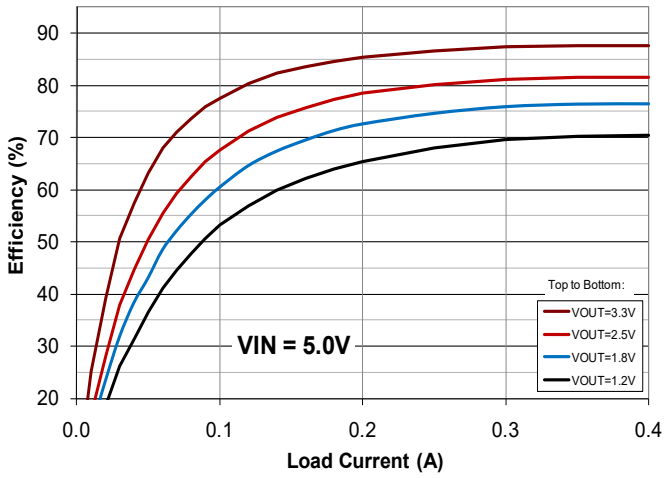
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VFB Voltage Initial Accuracy	V_{FB}	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	0.588	0.600	0.612	V
Drop Out Resistance	R_{DO}	Input to Output Resistance in 100% duty cycle operation.		350	500	mΩ
Line Regulation	ΔV_{OUT_LINE}	2.5V ≤ VIN ≤ 5.5V		0.03		%/V
Load Regulation	ΔV_{OUT_LOAD}	0A ≤ ILOAD ≤ 400mA		0.48		%/A
Temperature Variation	ΔV_{OUT_TEMPL}	-40°C ≤ TA ≤ +85°C		24		ppm/°C
Feedback Pin Input Current (3)	I_{FB}			<300		nA
Output Current Range	I_{OUT}		0		400	mA
OCP Threshold	I_{LIM}	2.5V ≤ VIN ≤ 5.5V 0.6V ≤ VOUT ≤ 3.3V		1.4		A
Output Dropout Resistance (3) Voltage (1) (3)	R_{DO} V_{DO_FL}	Input to Output Resistance V_{INMIN} - V_{OUT} at Full load		520 208	780 312	mΩ mV
Operating Output Voltage Range	V_{OUT}	V_{DO} = I_{OUT} * R_{DO}	0.6		V_{IN}-V_{DO}	V
Enable Pin Logic Low	V_{ENLO}				0.3	V
Enable Pin Logic High	V_{ENHI}		1.4			V
Enable Pin Current (3)	I_{ENABLE}			<200		nA
Operating Frequency	F_{OSC}			9		MHz
V_{OUT} Rise Time	T_{RISE}	From 0 to full output voltage	1.17	1.8	2.43	mSec

(3) Parameter guaranteed by design and characterization.

TYPICAL PERFORMANCE CURVES

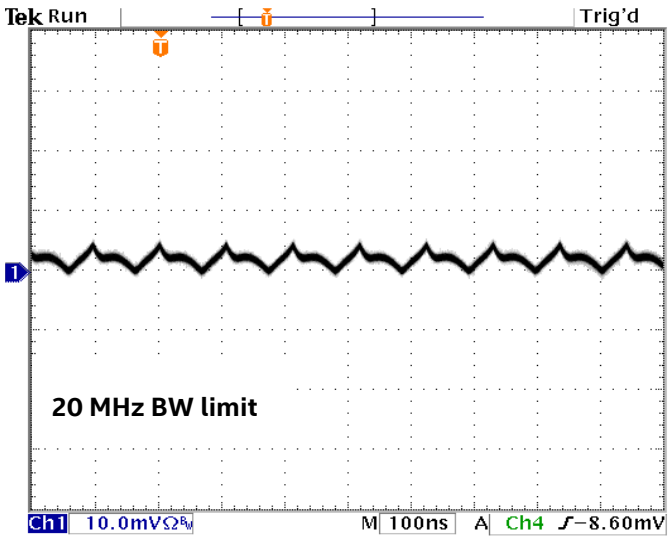


Efficiency vs. Load Current: V_{IN} = 3.3V, V_{OUT} (from top to bottom) = 2.5, 1.8, 1.2V



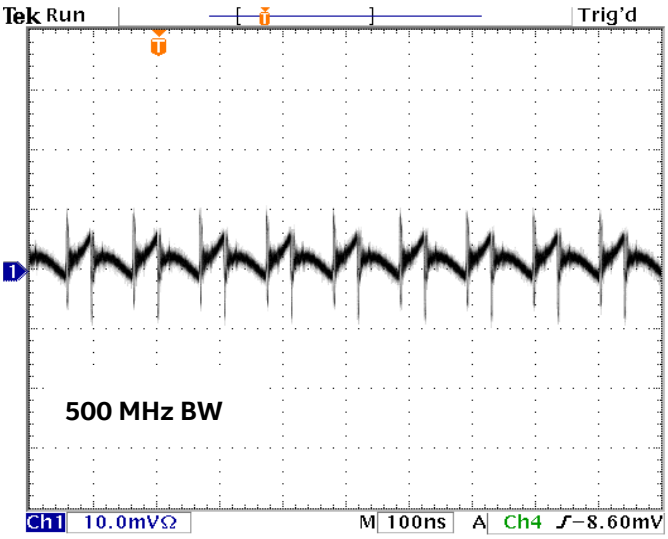
Efficiency vs. Load Current: V_{IN} = 5.0V, V_{OUT} (from top to bottom) = 3.3, 2.5, 1.8, 1.2V

TYPICAL PERFORMANCE CHARACTERISTICS



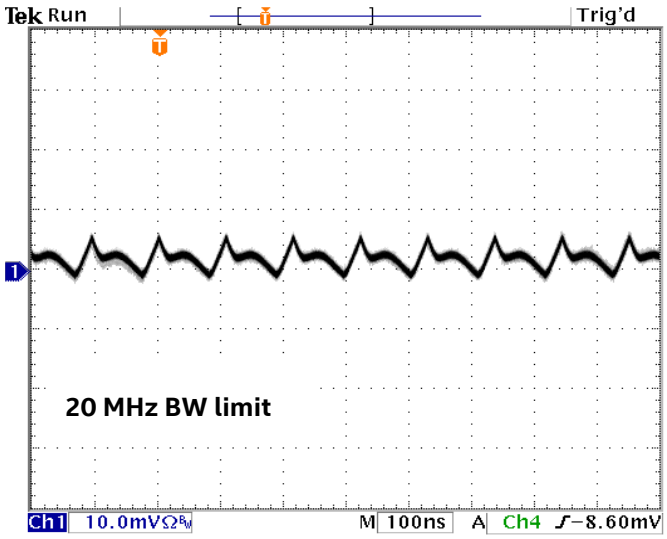
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.0V, Iout = 400mA

C_{IN} = 2.2µF/0603, C_{OUT} = 10µF/0603 + 2.2uF/0603



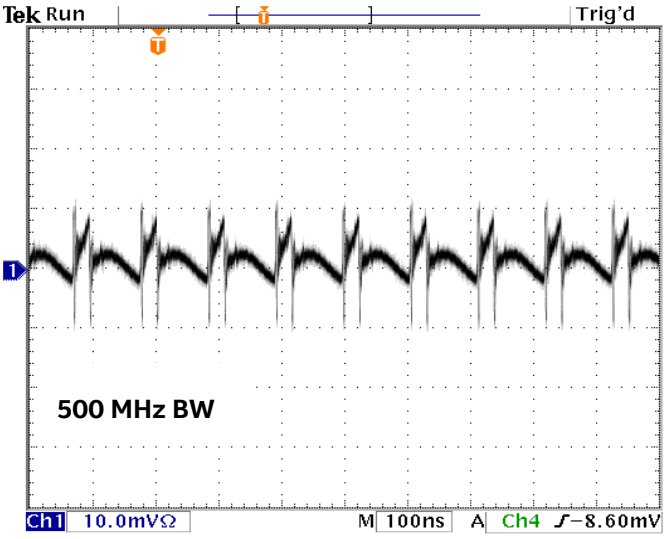
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.0V, Iout = 400mA

C_{IN} = 2.2µF/0603, C_{OUT} = 10µF/0603 + 2.2uF/0603



Output Ripple: V_{IN} = 5V, V_{OUT} = 1.0V, Iout = 400mA

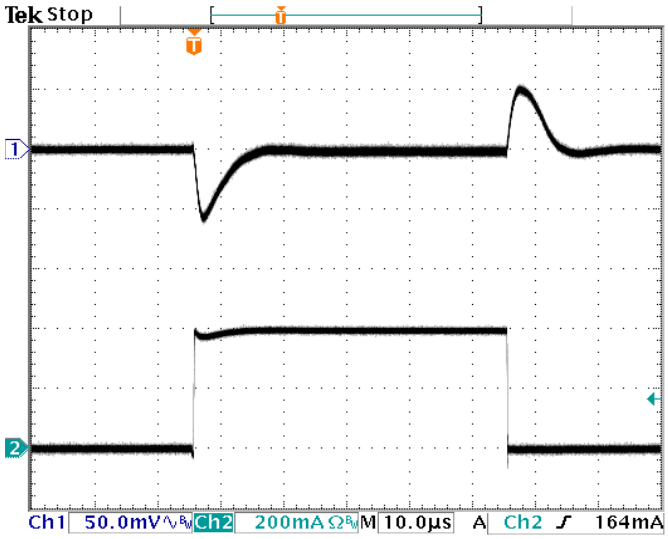
C_{IN} = 2.2µF/0603, C_{OUT} = 10µF/0603 + 2.2uF/0603



Output Ripple: V_{IN} = 5V, V_{OUT} = 1.0V, Iout = 400mA

C_{IN} = 2.2µF/0603, C_{OUT} = 10µF/0603 + 2.2uF/0603

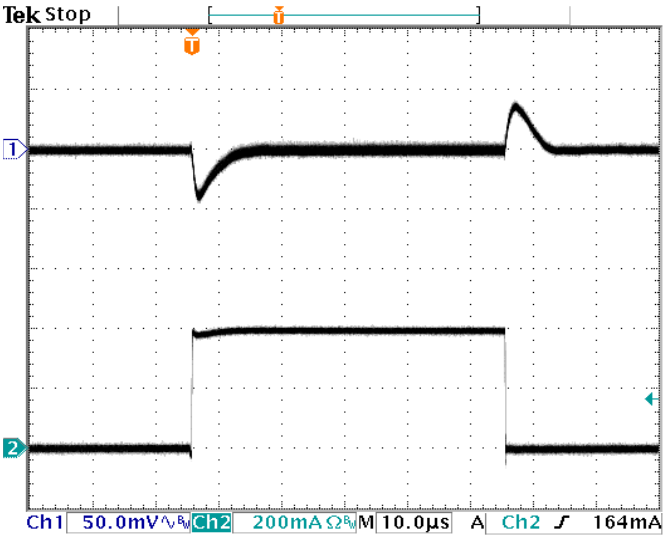
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



Load Transient: V_{IN} = 3.3V, V_{OUT} = 1.0V

Ch.1: V_{OUT}, Ch.2: I_{LOAD} 0↔400mA

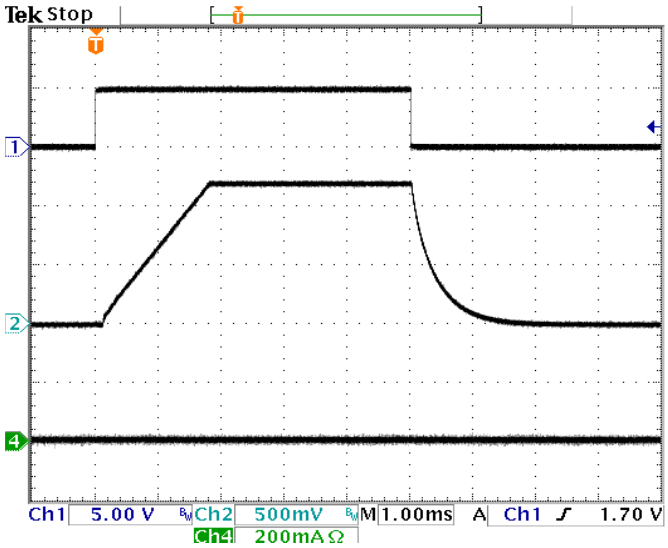
C_{IN} = 2.2µF/0603, C_{OUT} = 10µF/0603 + 2.2uF/0603



Load Transient: V_{IN} = 5V, V_{OUT} = 1.0V

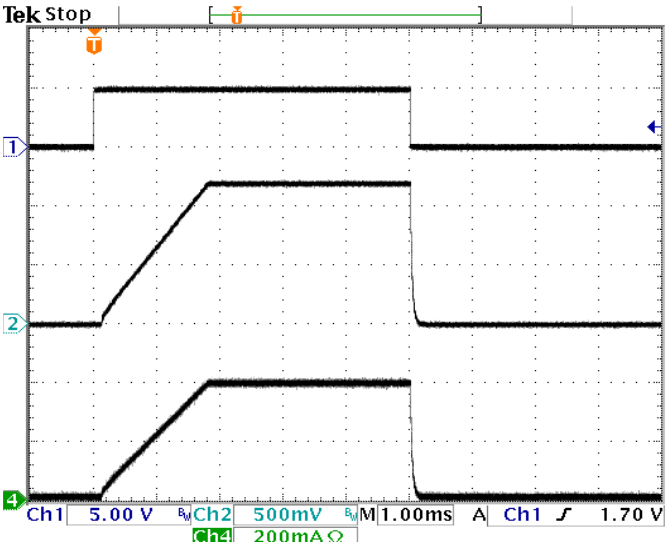
Ch.1: V_{OUT}, Ch.2: I_{LOAD} 0↔400mA

C_{IN} = 2.2µF/0603, C_{OUT} = 10µF/0603 + 2.2uF/0603



Power Up/Down at No Load: V_{IN}/V_{OUT} = 5.0V/1.2V,

Cout ≈ 10µF, Ch.1: ENABLE, Ch. 2: V_{OUT}, Ch.4: I_{OUT}



Power Up/Down into 3Ω load: V_{IN}/V_{OUT} = 5.5V/3.3V,

Cout ≈ 10µF, Ch.1: ENABLE, Ch. 2: V_{OUT}, Ch.4: I_{OUT}

FUNCTIONAL DESCRIPTION

Functional Overview

The EP5348UI requires only 2 small MLCC capacitors and a few small-signal components for a complete DC-DC converter solution. The device integrates MOSFET switches, PWM controller, Gate-drive, part of the loop compensation, and inductor into a tiny 2.0mm x 1.75mm x 0.9mm micro-QFN package. Advanced package design, along with the high level of integration, provides very low output ripple and noise. The EP5348UI uses voltage mode control for high noise immunity and load matching to advanced ≤90nm loads. An external resistor divider is used to program output setting over the 0.6V to V_{IN}-$V_{DROPOUT}$ as specified in the Electrical Characteristics Table. The EP5348UI provides the industry's highest power density of any 400mA DC-DC converter solution.

The key enabler of this revolutionary integration is Intel Enpirion's proprietary power MOSFET technology. The advanced MOSFET switches are implemented in deep-submicron CMOS to supply very low switching loss at high switching frequencies and to allow a high level of integration. The semiconductor process allows seamless integration of all switching, control, and compensation circuitry.

The proprietary magnetics design provides high-density/high-value magnetics in a very small footprint. Intel Enpirion magnetics are carefully matched to the control and compensation circuitry yielding an optimal solution with assured performance over the entire operating range.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor

The EP5348UI utilizes a proprietary low loss integrated inductor. The integration of the inductor greatly simplifies the power supply design process. The inherent shielding and compact construction of the integrated inductor reduces the noise that can couple into the traces of the printed circuit board. Further, the package layout is optimized to reduce the electrical path length for the high di/dT currents that are always present in DC-DC converters. The integrated inductor provides the optimal solution to the complexity, output ripple, and noise that plague low power DC-DC converter design.

Control Matched to sub 90nm Loads

The EP5348UI utilizes a type III compensation network. Voltage mode control is inherently impedance matched to the sub 90nm process technology that is used in today's advanced ICs. Voltage mode control also provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The very high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance.

Soft Start

Internal soft start circuits limit the rate of output voltage rise when the device starts up from a power down condition, or when the "ENABLE" pin is asserted "high". Digital control circuitry controls the V_{OUT} rise time to ensure a smooth turn-on ramp.

The EP5348UI has a fixed V_{OUT} turn-on time. Therefore, the ramp rate will vary with the output voltage setting. Output voltage rise time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. The maximum total capacitance on the output, including the output filter capacitor, and bulk and decoupling capacitance at the load, is given as:

$C_{OUT\_TOTAL\_MAX} = 9.333 \times 10^{-4} / V_{OUT}$

The nominal value for the output filter capacitor is 10uF. See the applications section for more details.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for approximately 0.5mS and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to ensure proper operation. If the voltage drops below the UVLO threshold, the lockout circuitry will disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation.

NOTE: The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown threshold, the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 15C°, the device will go through the normal startup process.

APPLICATION INFORMATION

Output Voltage Programming

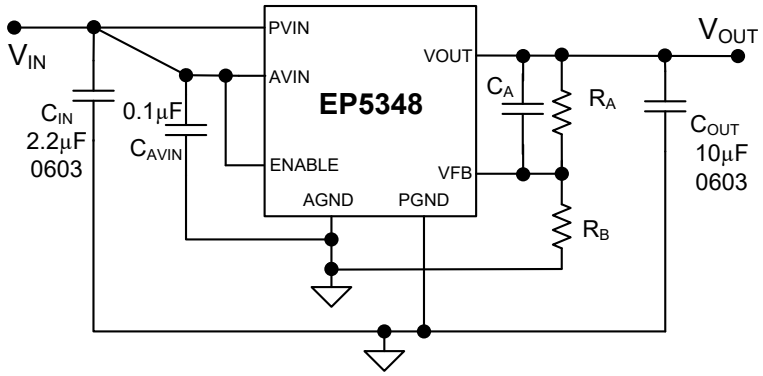


Figure 4. EP5348UI Application Circuit

The EP5348UI uses a simple resistor divider to program the output voltage.

Referring to Figure 3, use 200 kΩ, 1% or better for the upper resistor (R_A). The value of the bottom resistor (R_B) in kΩ is given as:

$$R_B = \frac{VFB * R_A}{(V_{OUT} - VFB)} \qquad VFB = 0.6V \text{ nominal}$$

A 5pF MLCC capacitor C_A is also required in parallel with R_A for compensation.

Input Filter Capacitor

C_{IN_MIN} = 2.2µF 0603 case size or larger.

The input capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input filter applications.

Output Filter Capacitor

C_{OUT_MIN} = 10uF 0603 + 2.2uF 0603 MLCC when 4.5V ≤ V_{IN} ≤ 5.5V, **AND** I_{OUT} > 300mA.

C_{OUT_MIN} = 10uF 0603 MLCC for all other use cases. However, ripple performance can always be improved by adding a second 2.2uF or 1uF output capacitor for any operating condition.

V_{OUT} has to be sensed at the last output filter capacitor next to the EP5348UI. Any additional bulk capacitance for load decoupling and byass has to be far enough from the V_{OUT} sensing point so that it does not interfere with the control loop operation. Excess total capacitance on the output (Output Filter + Bulk) can cause an over-current condition at startup. Please see the Soft Start section under Functional Overview for the maximum allowable bulk capacitance on the output rail.

The output capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter output filter applications.

LDO Replacement

The Intel Enpirion EP5348UI is a suitable replacement for inefficient LDOs and can be used to augment the LDOs in a PMU with minimum footprint impact. This integrated DCDC solution offers significantly better efficiency, and significant reduction in power loss. The resulting improved thermals and extended battery life helps meet Energy Star requirements. The total solution size is 25% smaller than a comparable LDO and half the footprint of a comparable DC-DC.

As the table below shows, EP5348UI provides the optimal trade-off between footprint and efficiency when compared to a traditional LDO:

VIN (V)	VOUT (V)	LOAD (mA)	EFF DCDC	EFF LDO	PLOSS DCDC (mW)	PLOSS LDO (mW)	Power Saved (mW)
5.0	1.2	400	70.4%	24.0%	**202**	**1520**	***1318***
5.0	1.8	400	76.4%	36.0%	**222**	**1280**	***1058***
5.0	2.5	400	81.6%	50.0%	**225**	**1000**	***775***
5.0	3.3	400	87.7%	66.0%	**185**	**680**	***495***
3.3	1.2	400	77.1%	36.4%	**143**	**840**	***697***
3.3	1.8	400	83.3%	54.5%	**144**	**600**	***456***
3.3	2.5	400	88.2%	75.8%	**134**	**320**	***186***

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Pre-Bias Start-up

The EP5348UI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EP5348UI is not pre-biased when the EP5348UI is first enabled.

LAYOUT RECOMMENDATIONS

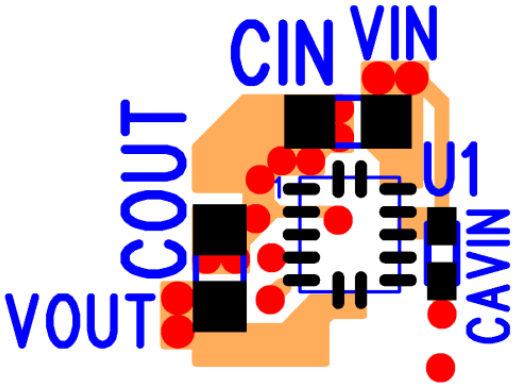


Figure 4: Top PCB Layer Critical Components and Copper for Minimum Footprint

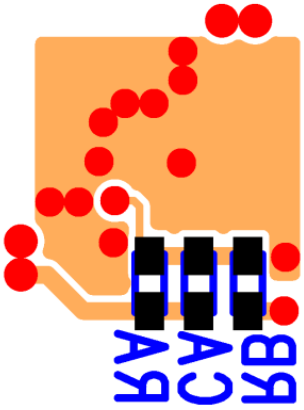


Figure 5: Bottom PCB Layer Critical Components (R_A, R_B, C_A) & Copper for Minimum Footprint

Figures 4 and 5 show critical PCB top and bottom layer components and traces for a minimum-footpint recommended EP5348 layout with ENABLE tied to V_{IN}. Alternate ENABLE configurations need to be connected and routed according to specific customer application. This layout consists of four layers. For the other 2 layers and the exact dimensions, please see the Gerber files at https://www.intel.com/enpirion. The recommendations given below are general guidelines. Customers may need to adjust these according to their own layout and manufacturing rules.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EP5348UI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EP5348UI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files at *https://www.intel.com/enpirion*.

Recommendation 3: Multiple small vias should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. See Figure 4. If the two vias cannot be put under C_{IN} or C_{OUT}, then put two vias right after the capacitors next the V_{IN} and V_{OUT} vias.

Recommendation 4: As Figure 5 shows, R_A, R_B, and C_A have been placed on the back side to minimize the footprint. These components also need to be close to the VFB pin (see Figures 3, 4 and 5). The VFB pin is a high-impedance, sensitive node. Keep any trace connected to this node as short and thin as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane. In the layout shown above, R_B goes to the via next to AGND pin using a dedicated trace on layer 3 not shown here. Please see the Gerber files at *https://www.intel.com/enpirion*.

Recommendation 5: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 4 this connection is made at the vias just before C_{IN}. There is an additional decoupling capacitor C_{AVIN} for AVIN which is connected between the device pin and the GND plane.

Recommendation 6: The via to the right of pin 2 underneath the device helps to minimize the parasitic inductances in the input and output loop ground connections.

Recommendation 7: The top layer 1 metal under the device must not be more than shown in Figure 4. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

RECOMMENDED PCB FOOTPRINT

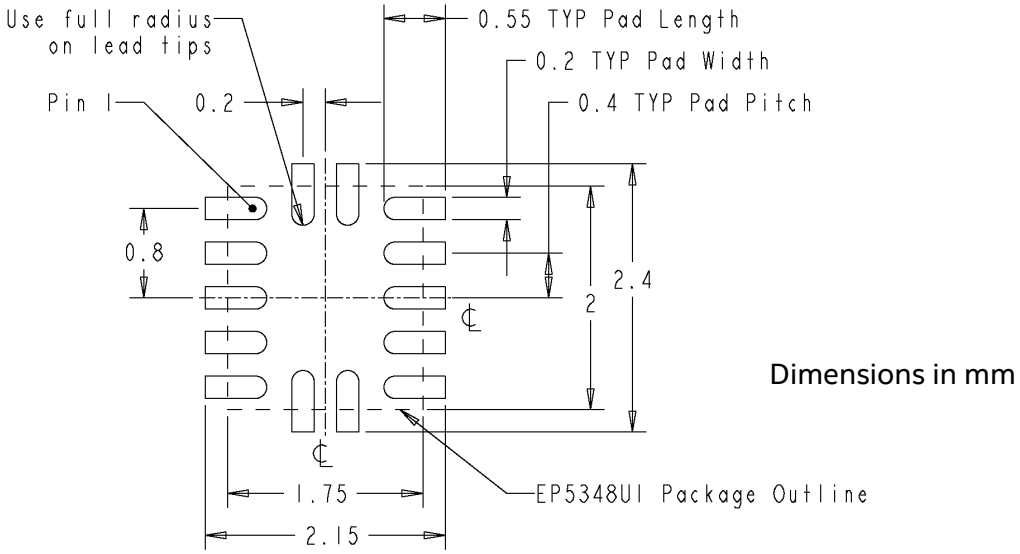


Figure 6: EP5348UI PCB Footprint (Top View)

PACKAGE DIMENSIONS

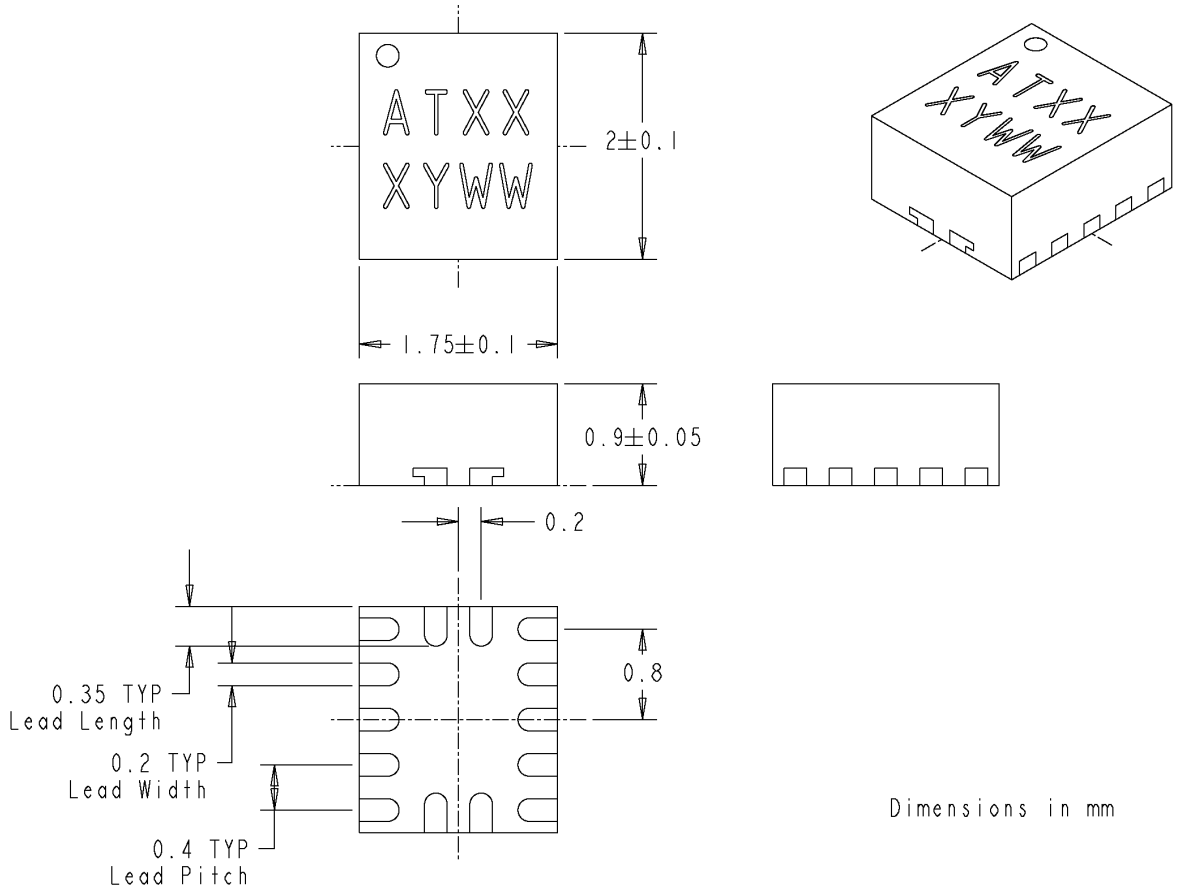


Figure 7: EP5348UI Package Dimensions (Bottom View)

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
E	Dec, 2018	Changed datasheet into Intel format.

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

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