





### N-CHANNEL ENHANCEMENT MODE MOSFET

### **Features**

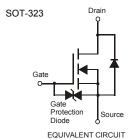
- Low On-Resistance: R<sub>DS(ON)</sub>
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected up to 2KV
- Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability

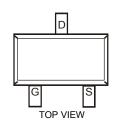
### **Mechanical Data**

- Case: SOT-323
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminals: Finish Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.006 grams (approximate)









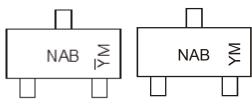
## Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2004WK-7	SOT-323	3000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green"
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html

## **Marking Information**



Chengdu A/T Site Shanghai A/T Site

NAB = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)

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\begin{align\*}
\text{YM} = Date Code Marking for SAT (Chengdu Assembly/ Test site)
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Y or  $\overline{Y}$  = Year (ex: A = 2013)

M = Month (ex: 9 = September)

Date Code Key

Date Code Ney												
Year	200	9	2010		2011	20	12	2013		2014	2	2015
Code	W		Х		Υ		Z	Α		В		С
						-		1		1		
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



## **Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Cha	racteristic		Symbol	Value	Units
Drain-Source Voltage			$V_{DSS}$	20	V
Gate-Source Voltage			$V_{GSS}$	±8	V
Drain Current (Note 5)	Steady State	T <sub>A</sub> = +25°C T <sub>A</sub> = +85°C	I <sub>D</sub>	540 390	mA
Pulsed Drain Current (Note 6)			I <sub>DM</sub>	1.5	Α

# Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	$P_{D}$	200	mW
Thermal Resistance, Junction to Ambient	$R_{ hetaJA}$	625	°C/W
Operating and Storage Temperature Range	T <sub>J,</sub> T <sub>STG</sub>	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PCB.

6. Pulse width  ${\le}10\mu S,$  Duty Cycle  ${\le}1\%.$ 

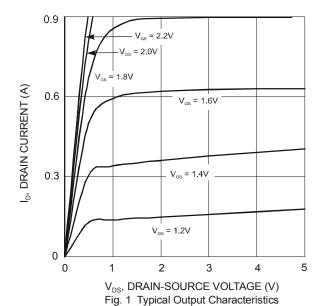
# **Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

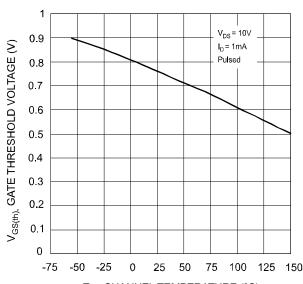
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
Characteristic   Symbol   Min   Typ   Max   Unit   Test Condition OFF CHARACTERISTICS (Note 7)							
` '	D) /	20	1			V 0V 1 40 A	
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	_		V	$V_{GS} = 0V, I_D = 10\mu A$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1	μΑ	$V_{DS} = 16V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±1	μA	$V_{GS} = \pm 4.5V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)						·	
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.5	_	1.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
			0.4	0.55		$V_{GS} = 4.5V, I_D = 540mA$	
Static Drain-Source On-Resistance	R <sub>DS (ON)</sub>	_	0.5	0.70	Ω	$V_{GS} = 2.5V, I_D = 500mA$	
			0.7	0.9		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 350mA	
Forward Transfer Admittance	Y <sub>fs</sub>	200	_		ms	V <sub>DS</sub> =10V, I <sub>D</sub> = 0.2A	
Diode Forward Voltage (Note 7)	$V_{SD}$	0.5	_	1.4	V	$V_{GS} = 0V, I_{S} = 115mA$	
DYNAMIC CHARACTERISTICS(Note 8)							
Input Capacitance	C <sub>iss</sub>	_	_	150	pF	101/11/001/	
Output Capacitance	Coss			25	pF	$V_{DS} = 16V, V_{GS} = 0V$ f = 1.0MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>			20	pF	1 - 1.0101112	

Notes: 7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to production testing.







T<sub>ch</sub>, CHANNEL TEMPERATURE (°C)
Fig. 3 Gate Threshold Voltage vs. Channel Temperature

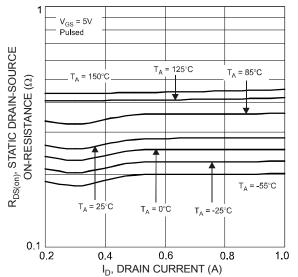


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

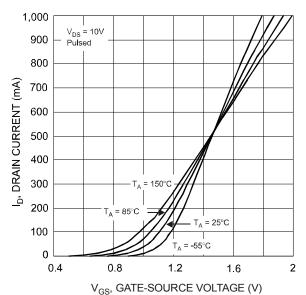


Fig. 2 Reverse Drain Current vs. Source-Drain Voltage

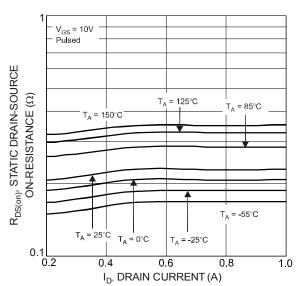


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

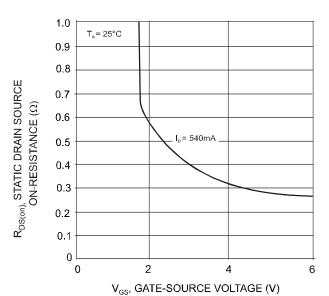


Fig. 6 Static Drain-Source, On-Resistance vs. Gate-Source Voltage



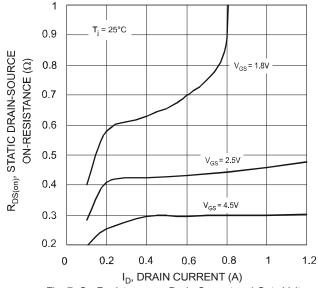
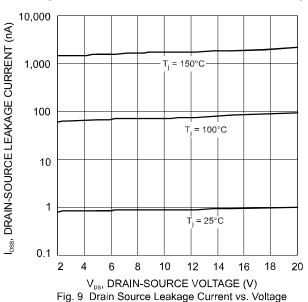


Fig. 7 On-Resistance vs. Drain Current and Gate Voltage



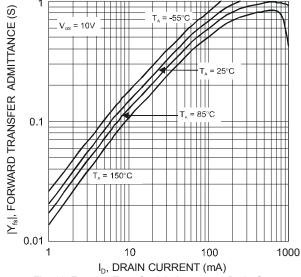


Fig. 11 Forward Transfer Admittance vs. Drain Current

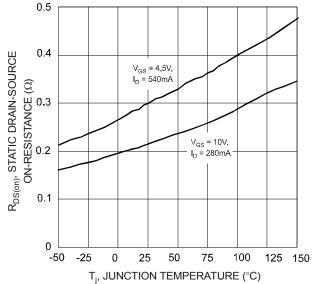


Fig. 8 Static Drain-Source, On-Resistance vs. Temperature

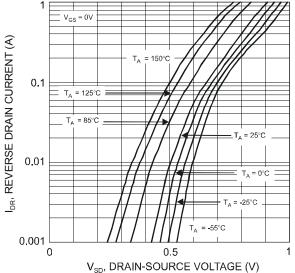
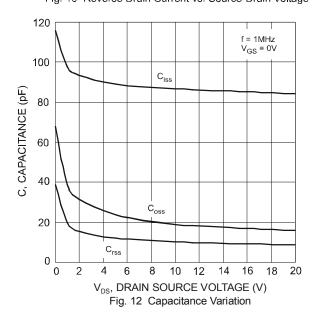


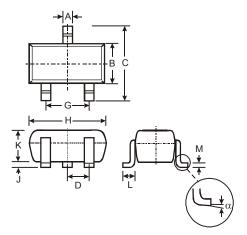
Fig. 10 Reverse Drain Current vs. Source-Drain Voltage





## **Package Outline Dimensions**

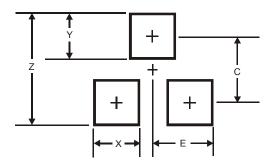
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT-323							
Dim	Min	Max	Тур				
Α	0.25	0.40	0.30				
В	1.15	1.35	1.30				
С	2.00	2.20	2.10				
D	-	-	0.65				
G	1.20	1.40	1.30				
Н	1.80	2.20	2.15				
J	0.0	0.10	0.05				
K	0.90	1.00	0.95				
L	0.25	0.40	0.30				
M	0.10	0.18	0.11				
α	0°	8°	-				
All Dimensions in mm							

## **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.8
Х	0.7
Y	0.9
С	1.9
E	1.0



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