UNITRODE

SCSI Termpower Manager

FEATURES

- Integrated Circuit Breaker Function
- Integrated 0.2Ω Power FET
- SCSI, SCSI-2, SCSI-3 Compliant
- 1µA ICC When Disabled
- Programmable On Time
- Accurate 1.65A Trip Current and 2.0A Max Current
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown

DESCRIPTION

The UCC3916 SCSI termpower manager provides complete power management, hot swap capability, and circuit breaker functions with minimal external components. For most applications, the only external component required to operate the device, other than supply bypassing, is a timing capacitor which sets the fault time.

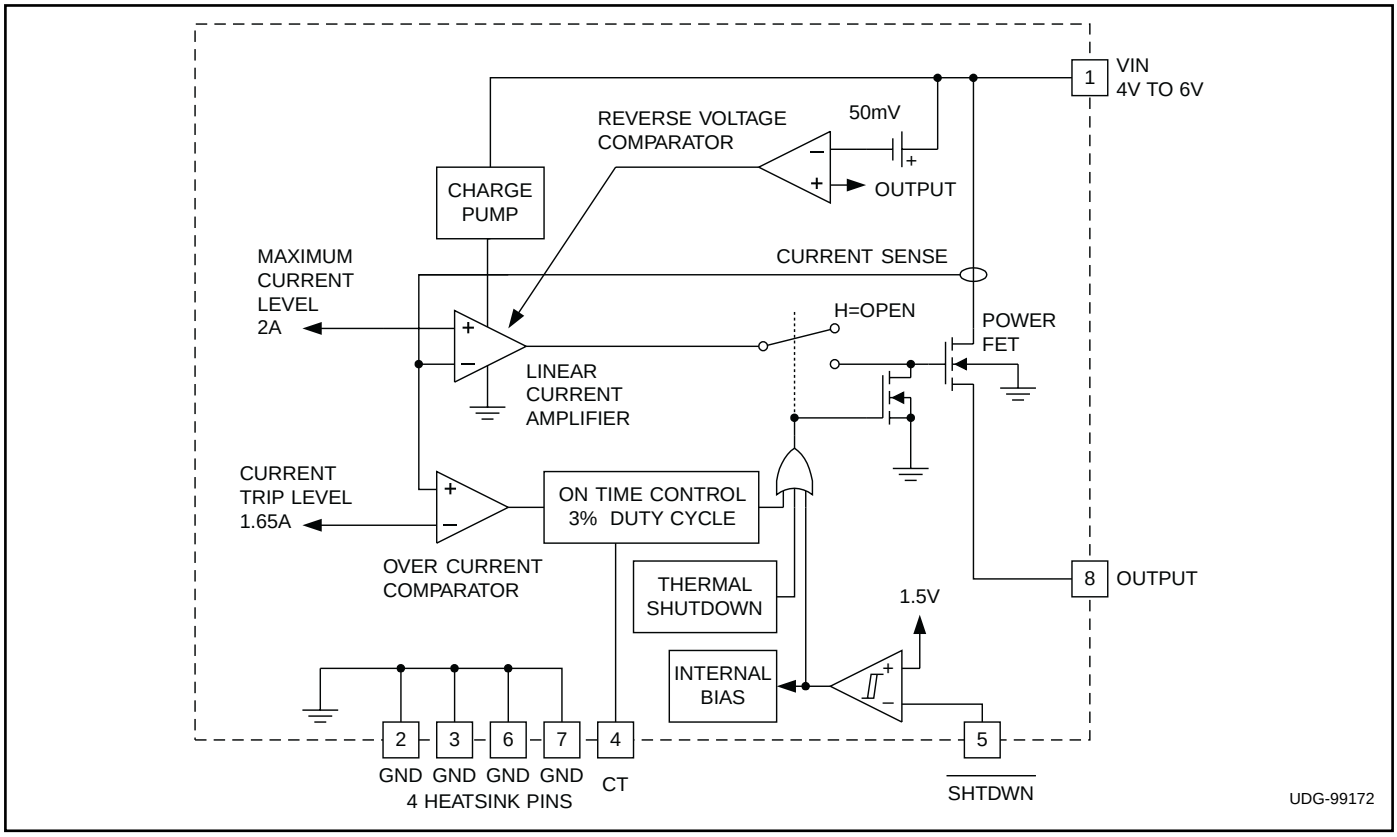
The current trip level is internally set at 1.65A, and the maximum current level is also internally programmed for 2A. While the output current is below the trip level of 1.65A, the internal power MOSFET is switched on at a nominal 220mΩ. When the output current exceeds the trip level but remains less than the maximum current level, the MOSFET remains switched on, but the fault timer starts charging CT. Once the fault time is reached, the circuit will shut off for a time which equates to a 3% duty cycle. Finally, when the output current reaches the maximum current level, the MOSFET transitions from a switch to a constant current source.

The UCC3916 is designed for uni-directional current flow, emulating a diode in series with the power MOSFET.

The UCC3916 can be put in a sleep mode, drawing only 1µA of supply current.

Other features include thermal shutdown and low thermal resistance Small Outline Power package.

BLOCK DIAGRAM



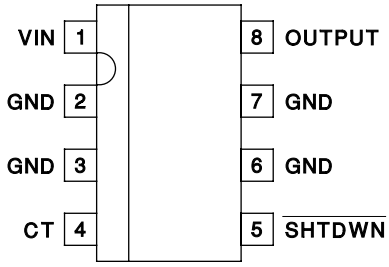
ABSOLUTE MAXIMUM RATINGS

VIN . . . . . +6V
Output Current
DC . . . . . Self Limiting
Pulse (Less than 100ns) 20A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = 0°C to +70°C; VIN = 5V, $\overline{SHTDWN}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
ICC			1.00	2.00	mA
ICC - Sleep Mode	$\overline{SHTDWN}$ = 0.2V		0.50	5	µA
Output Section					
Voltage Drop	I_{OUT} = 1A		0.22	0.33	V
	I_{OUT} = 1.5A		0.33	0.50	V
	I_{OUT} = 1.65A		0.40	0.60	V
Trip Current		–1.8	–1.65	–1.5	A
Max Current		–2.4	–2	–1.65	A
Reverse Leakage	VIN = 4.5V, V_{OUT} = 5V		6	20	µA
	VIN = 0V, V_{OUT} = 5V		0.50	9	µA
Soft Start Time	Initial Startup		50		µs
Short Circuit Response			100		ns
Fault Section					
CT Charge Current	V_{CT} = 1.0V	–45	–36.0	–27	µA
CT Discharge Current	V_{CT} = 1.0V	0.90	1.0	1.50	µA
Output Duty Cycle	V_{OUT} = 0V	2.00	3.00	6.00	%
CT Charge Threshold		0.4	0.5	0.6	V
CT Discharge Threshold		1.2	1.4	1.8	V
Thermal Shutdown			170		°C
Thermal Hysteresis			10		°C
Shutdown Section					
Shutdown Threshold			1.5	3.0	V
Shutdown Hysteresis			150	300	mV
Shutdown Bias Current	$\overline{SHTDWN}$ = 1.0V		100	500	nA

Note 1: All voltages are with respect to ground.

PIN DESCRIPTIONS

CT: A capacitor is applied between this pin and ground to set the maximum fault time. The maximum fault time must be more than the time to charge external capacitance. The maximum fault time is defined as:

$$T_{FAULT} = 28 \bullet 10^3 \bullet CT.$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 1 \bullet 10^6 \bullet CT$$

this results in a 3% duty cycle. 0.1µF is recommended for SCSI applications to achieve the normal maximum capacitance on the Termpwr line.

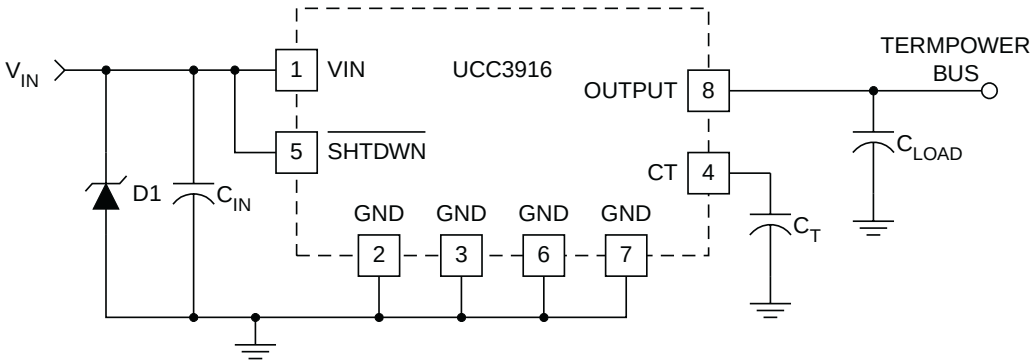
$\overline{\text{SHTDWN}}$: The IC enters a low-power sleep mode when this pin is low and exits the sleep mode when this pin is high.

VIN: Input voltage to the circuit breaker, ranging from 4V to 6V.

VOUT: Output voltage of the circuit breaker. When switched, the output voltage is approximately:

$$V_{OUT} = VIN - (220m\Omega) \bullet I_{OUT}.$$

TYPICAL APPLICATION



UDG-99169

APPLICATION INFORMATION

Protecting The UCC3916 From Voltage Transients

The parasitic inductance associated with the power distribution can cause a voltage spike at V_{IN} if the load current is suddenly interrupted by the UCC3916. *It is important to limit the peak of this spike to less than 6V to prevent damage to the UCC3916*. This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive (+) and negative (–) leads of the power supply feeding V_{IN} pin, locate the power supply close to the UCC3916 or use a PCB ground plane).
- Decoupling V_{IN} with a capacitor, C_{IN}, located close to the V_{IN}. This capacitor is typically less than 1µF to limit the inrush current.
- Clamping the voltage at V_{IN} below 6V with a Zener diode, D1, located close to the V_{IN} pin.

SAFETY RECOMMENDATIONS

Although the UCC3916 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3916 is intended for use in safety critical applications where UL© or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3916 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3916DP	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3916	Samples
UCC3916DPTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3916	Samples
UCC3916DPTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3916	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

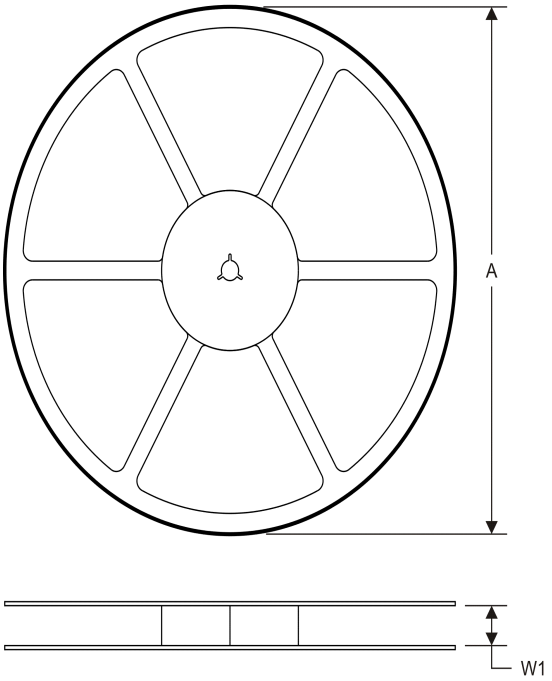
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

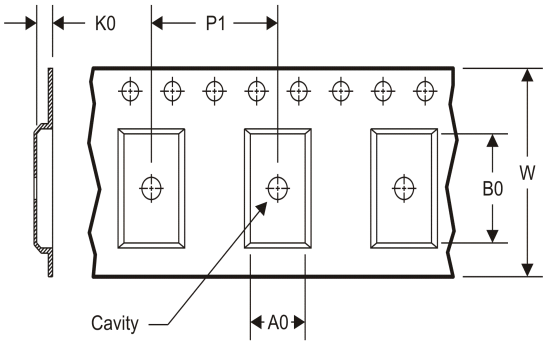
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



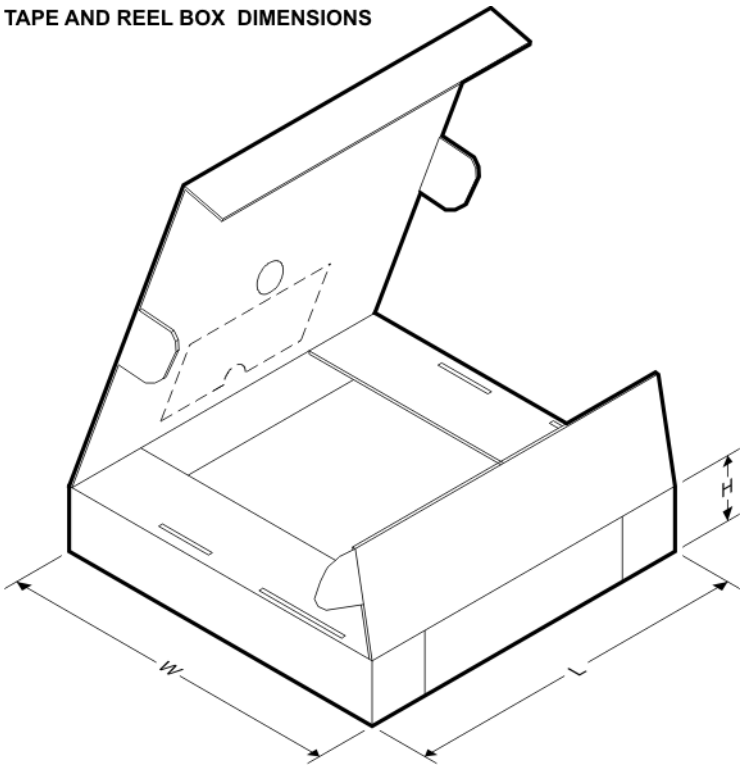
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC3916DPTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC3916DPTR	SOIC	D	8	2500	367.0	367.0	35.0

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