

HiperFET™ Power MOSFET Q3-Class

IXFR15N100Q3

$$\begin{aligned} V_{DSS} &= 1000V \\ I_{D25} &= 10A \\ R_{DS(on)} &\leq 1.2\Omega \\ t_{rr} &\leq 250ns \end{aligned}$$

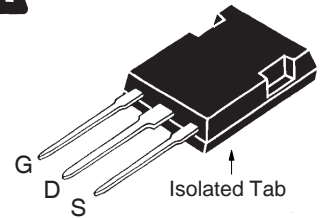
(Electrically Isolated Tab)



N-Channel Enhancement Mode
Fast Intrinsic Rectifier

| Symbol | Test Conditions | Maximum Ratings | |
|---------------|--|-----------------|------------------|
| V_{DSS} | $T_J = 25^\circ\text{C}$ to 150°C | 1000 | V |
| V_{DGR} | $T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$ | 1000 | V |
| V_{GSS} | Continuous | ± 30 | V |
| V_{GSM} | Transient | ± 40 | V |
| I_{D25} | $T_C = 25^\circ\text{C}$ | 10 | A |
| I_{DM} | $T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM} | 45 | A |
| I_A | $T_C = 25^\circ\text{C}$ | 7.5 | A |
| E_{AS} | $T_C = 25^\circ\text{C}$ | 1.0 | J |
| dv/dt | $I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$ | 50 | V/ns |
| P_D | $T_C = 25^\circ\text{C}$ | 400 | W |
| T_J | | -55 ... +150 | $^\circ\text{C}$ |
| T_{JM} | | 150 | $^\circ\text{C}$ |
| T_{stg} | | -55 ... +150 | $^\circ\text{C}$ |
| T_L | 1.6mm (0.062 in.) from Case for 10s | 300 | $^\circ\text{C}$ |
| T_{SOLD} | Plastic Body for 10s | 260 | $^\circ\text{C}$ |
| V_{ISOL} | 50/60 Hz, 1 Minute | 2500 | V~ |
| F_C | Mounting Force | 20..120/4.5..27 | N/lb. |
| Weight | | 5 | g |

ISOPLUS247
E153432



G = Gate D = Drain
S = Source

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- Low Intrinsic Gate Resistance
- 2500V~ Electrical Isolation
- Fast Intrinsic Rectifier
- Avalanche Rated
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- DC Choppers
- Temperature and Lighting Controls

| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified) | Characteristic Values | | |
|--------------|---|-----------------------|------|----------------------------|
| | | Min. | Typ. | Max. |
| BV_{DSS} | $V_{GS} = 0V$, $I_D = 1mA$ | 1000 | | V |
| $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 4mA$ | 3.5 | | 6.5 V |
| I_{GSS} | $V_{GS} = \pm 30V$, $V_{DS} = 0V$ | | | ± 100 nA |
| I_{DSS} | $V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$ | | | 25 μA 1.5 mA |
| $R_{DS(on)}$ | $V_{GS} = 10V$, $I_D = 7.5A$, Note 1 | | | 1.2 Ω |

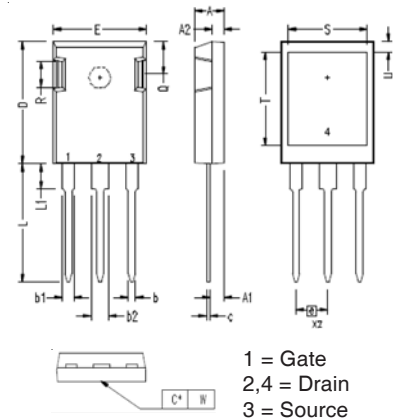
| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified) | Characteristic Values | | |
|--------------|--|-----------------------|------|--------------------|
| | | Min. | Typ. | Max. |
| g_{fs} | $V_{DS} = 20\text{V}, I_D = 7.5\text{A}$, Note 1 | 7.5 | 12.5 | S |
| C_{iss} | $V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ | | 3250 | pF |
| C_{oss} | | | 265 | pF |
| C_{rss} | | | 24 | pF |
| R_{Gi} | Gate Input Resistance | | 0.20 | Ω |
| $t_{d(on)}$ | Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 7.5\text{A}$ $R_G = 2\Omega$ (External) | | 28 | ns |
| t_r | | | 10 | ns |
| $t_{d(off)}$ | | | 30 | ns |
| t_f | | | 8 | ns |
| $Q_{g(on)}$ | $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 7.5\text{A}$ | | 64 | nC |
| Q_{gs} | | | 23 | nC |
| Q_{gd} | | | 27 | nC |
| R_{thJC} | | | 0.31 | $^\circ\text{C/W}$ |
| R_{thCS} | | 0.15 | | $^\circ\text{C/W}$ |

Source-Drain Diode

| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified) | Characteristic Values | | |
|----------|--|-----------------------|------|--------|
| | | Min. | Typ. | Max. |
| I_S | $V_{GS} = 0\text{V}$ | | | 15 A |
| I_{SM} | Repetitive, Pulse Width Limited by T_{JM} | | | 60 A |
| V_{SD} | $I_F = I_S, V_{GS} = 0\text{V}$, Note 1 | | | 1.4 V |
| t_{rr} | $I_F = 7.5\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$ | | | 250 ns |
| I_{RM} | | | 7.6 | A |
| Q_{RM} | | | 660 | nC |

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

ISOPLUS247 (IXFR) Outline



| SYM | INCHES | | MILLIMETERS | |
|-----|----------|------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .190 | .205 | 4.83 | 5.21 |
| A1 | .090 | .100 | 2.29 | 2.54 |
| A2 | .075 | .085 | 1.91 | 2.16 |
| b | .045 | .055 | 1.14 | 1.40 |
| b1 | .075 | .085 | 1.91 | 2.15 |
| b2 | .115 | .126 | 2.92 | 3.20 |
| C | .024 | .033 | 0.61 | 0.83 |
| D | .819 | .840 | 20.80 | 21.34 |
| E | .620 | .635 | 15.75 | 16.13 |
| e | .215 BSC | | 5.45 BSC | |
| L | .780 | .811 | 19.81 | 20.60 |
| L1 | .150 | .172 | 3.81 | 4.38 |
| Q | .220 | .244 | 5.59 | 6.20 |
| R | .170 | .191 | 4.32 | 4.85 |
| S | .520 | .540 | 13.21 | 13.72 |
| T | .620 | .640 | 15.75 | 16.26 |
| U | .065 | .080 | 1.65 | 2.03 |
| W | 0 | .004 | 0 | 0.10 |

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

| | | | | | | | | | | |
|--|-----------|-----------|-----------|-----------|--------------|--------------|--------------|--------------|--------------|-------------|
| IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: | 4,835,592 | 4,931,844 | 5,049,961 | 5,237,481 | 6,162,665 | 6,404,065 B1 | 6,683,344 | 6,727,585 | 7,005,734 B2 | 7,157,338B2 |
| | 4,850,072 | 5,017,508 | 5,063,307 | 5,381,025 | 6,259,123 B1 | 6,534,343 | 6,710,405 B2 | 6,759,692 | 7,063,975 B2 | |
| | 4,881,106 | 5,034,796 | 5,187,117 | 5,486,715 | 6,306,728 B1 | 6,583,505 | 6,710,463 | 6,771,478 B2 | 7,071,537 | |

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

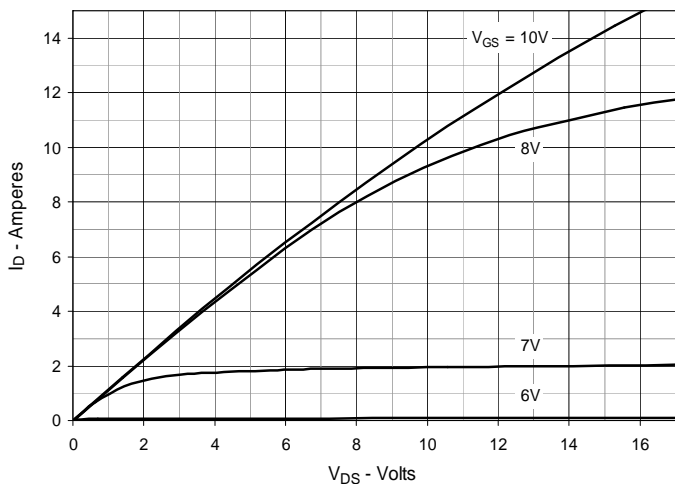


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

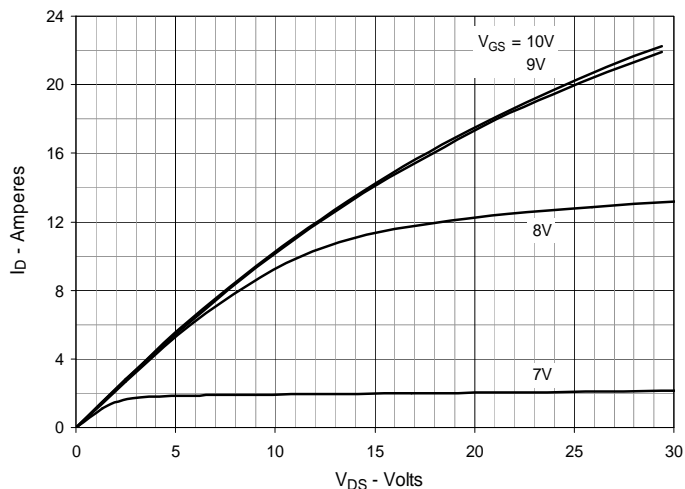


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

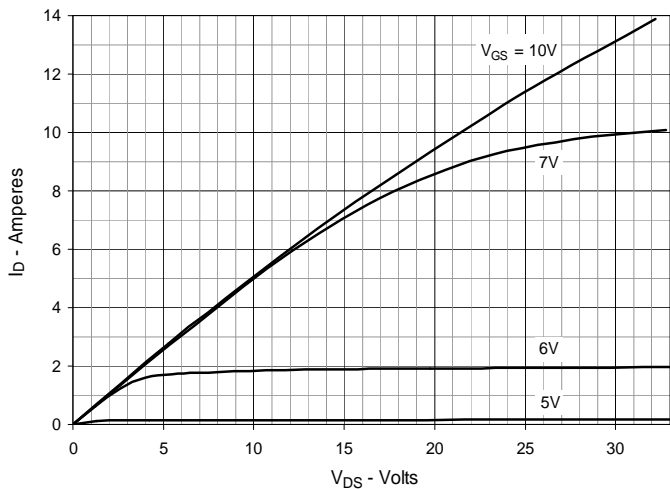


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 7.5\text{A}$ Value vs. Junction Temperature

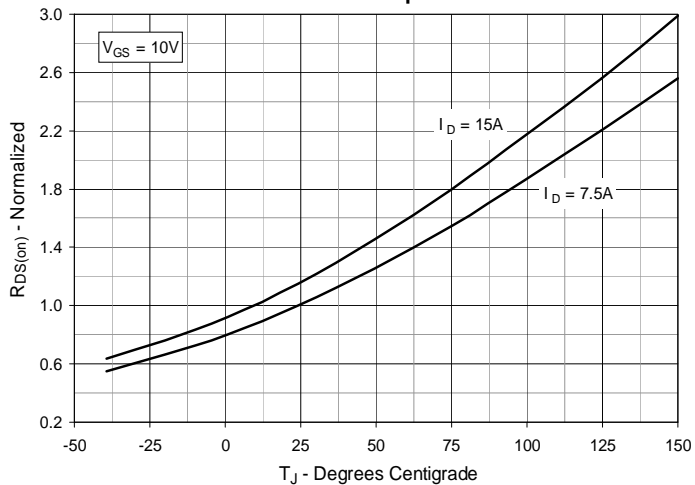


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 7.5\text{A}$ Value vs. Drain Current

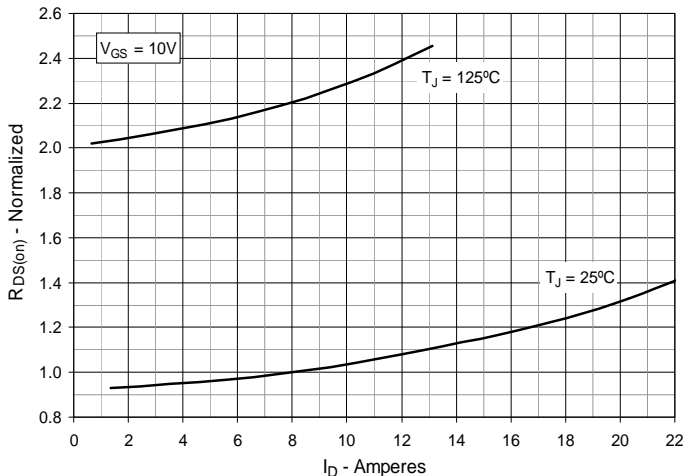


Fig. 6. Maximum Drain Current vs. Case Temperature

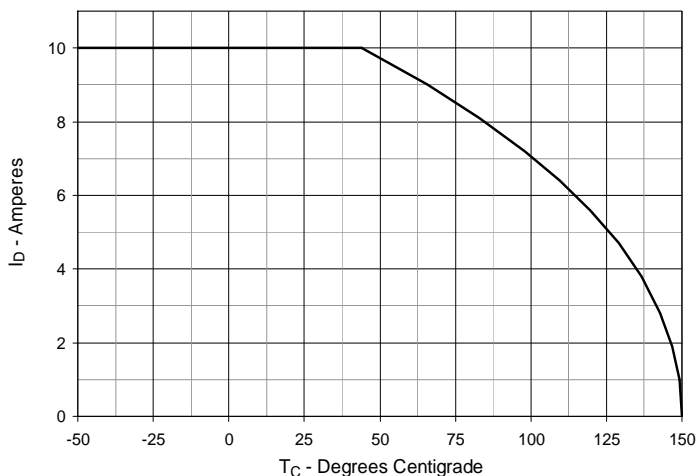


Fig. 7. Input Admittance

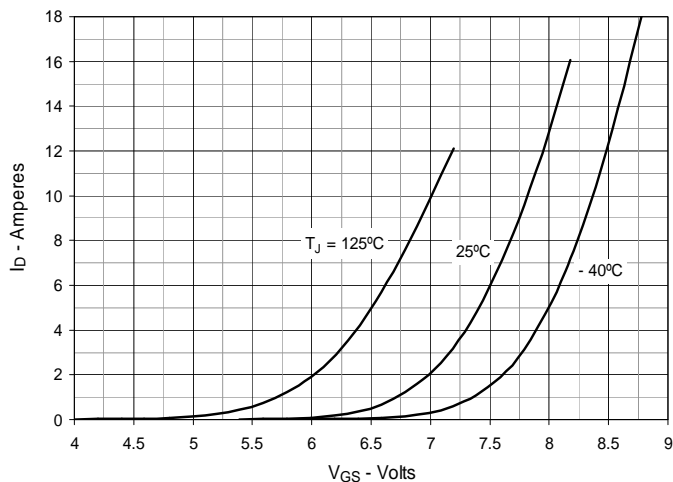


Fig. 8. Transconductance

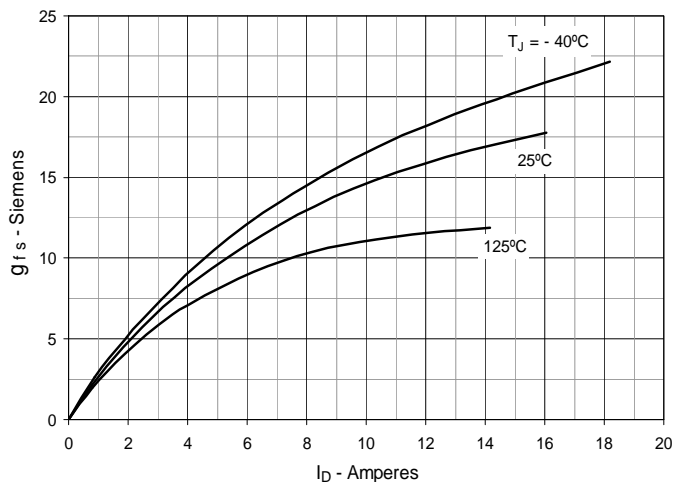


Fig. 9. Forward Voltage Drop of Intrinsic Diode

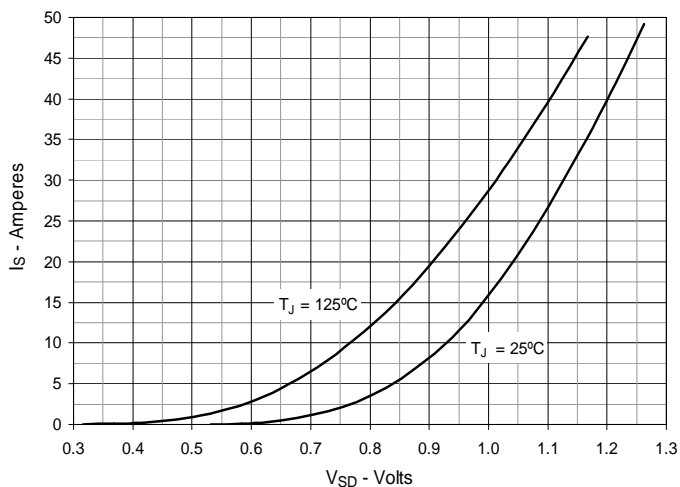


Fig. 10. Gate Charge

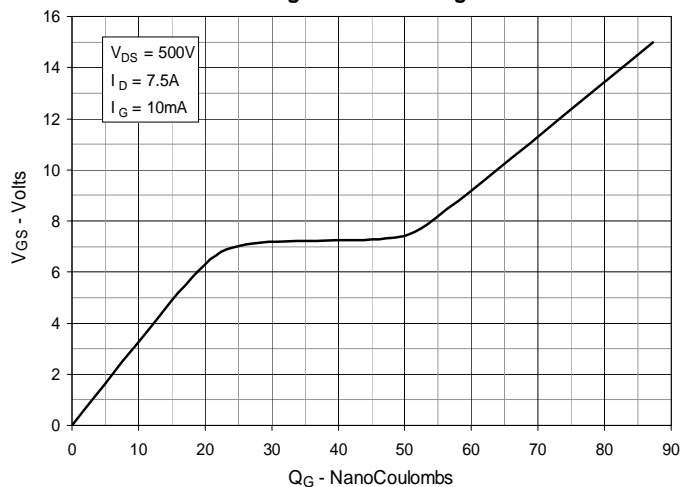


Fig. 11. Capacitance

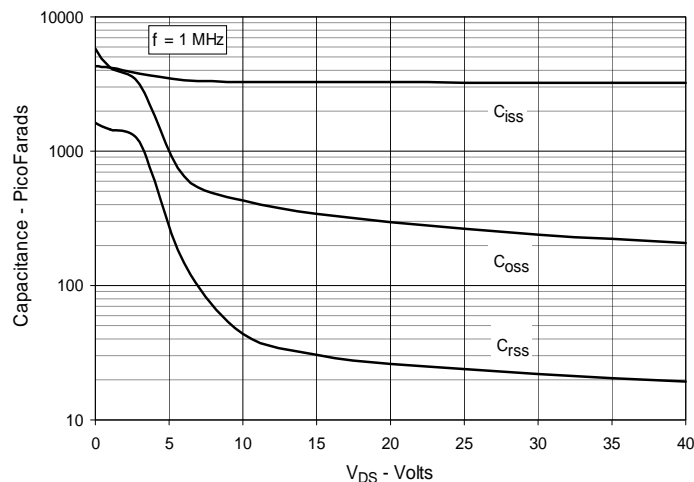


Fig. 12. Forward-Bias Safe Operating Area

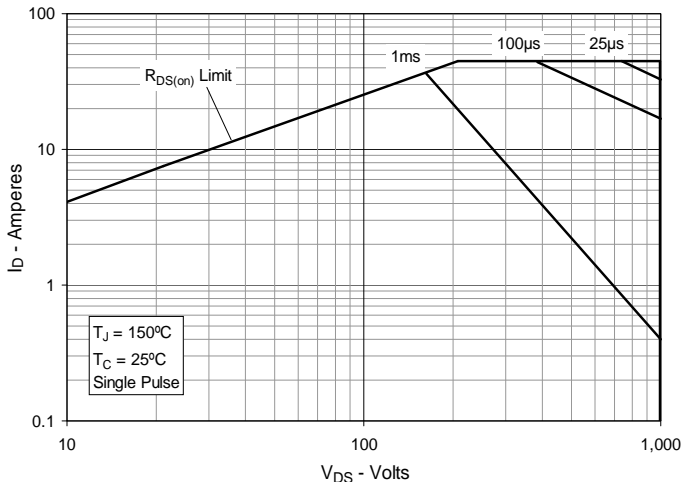
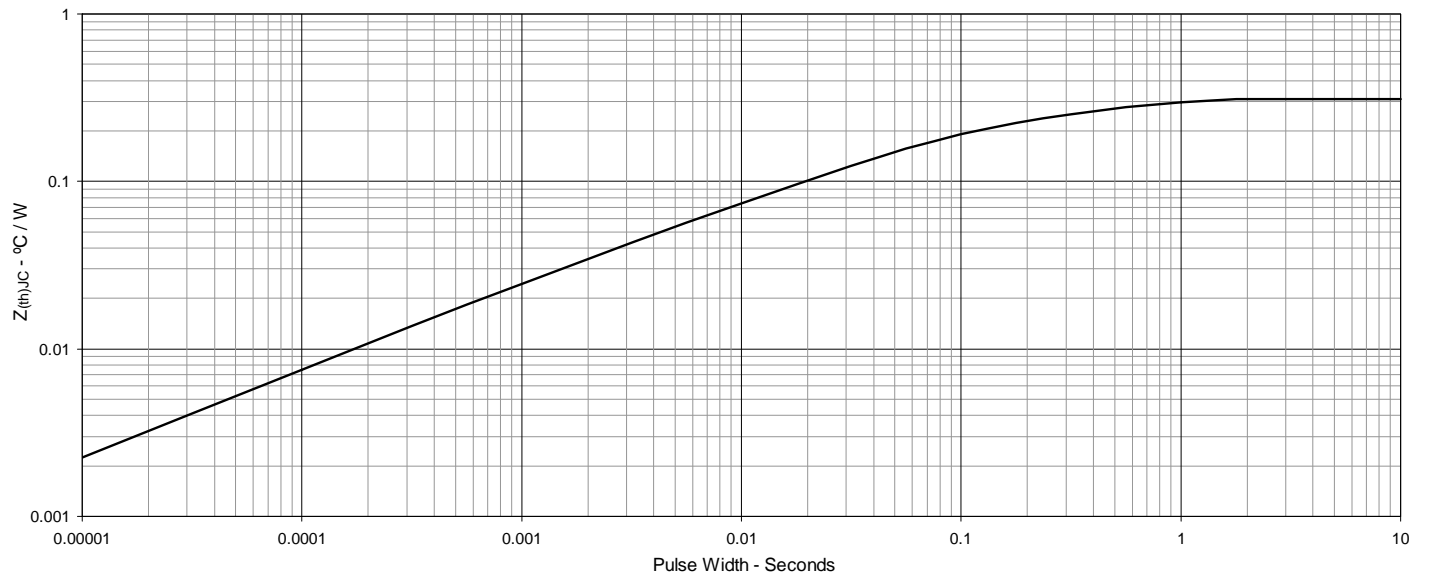


Fig. 13. Maximum Transient Thermal Impedance



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