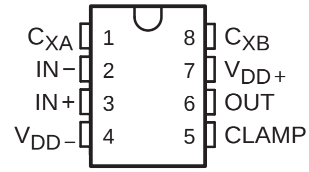
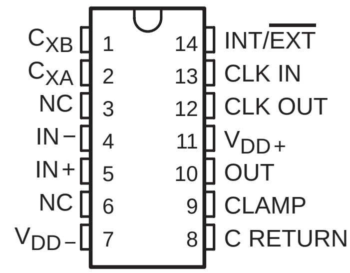
- **Extremely Low Offset Voltage . . . 1 μV Max**
- **Extremely Low Change on Offset Voltage With Temperature . . . 0.003 μV/°C Typ**
- **Low Input Offset Current**
  500 pA Max at T_A = − 55°C to 125°C
- **A_{VD} . . . 135 dB Min**
- **CMRR . . . 120 dB Min**
- **k_{SVR} . . . 110 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation With External Capacitors Connected to V_{DD-}**

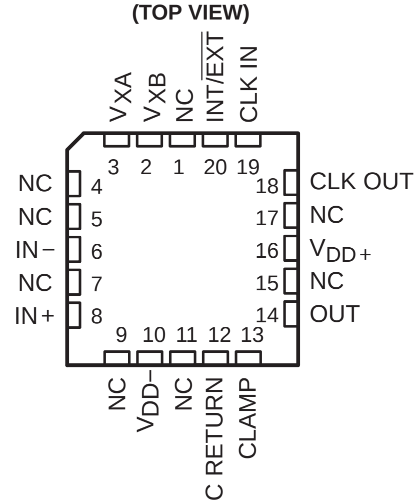
D008, JG, OR P PACKAGE
(TOP VIEW)



D014, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TLC2652 and TLC2652A are high-precision chopper-stabilized operational amplifiers using Texas Instruments Advanced LinCMOS™ process. This process, in conjunction with unique chopper-stabilization circuitry, produces operational amplifiers whose performance matches or exceeds that of similar devices available today.

Chopper-stabilization techniques make possible extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. In addition, low-frequency noise voltage is significantly reduced. This high precision, coupled with the extremely high input impedance of the CMOS input stage, makes the TLC2652 and TLC2652A an ideal choice for low-level signal processing applications such as strain gauges, thermocouples, and other transducer amplifiers. For applications that require extremely low noise and higher usable bandwidth, use the TLC2654 or TLC2654A device, which has a chopping frequency of 10 kHz.

The TLC2652 and TLC2652A input common-mode range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±1.9 V.

Two external capacitors are required for operation of the device; however, the on-chip chopper-control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is made accessible to allow the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold level of the TLC2652 and TLC2652A requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

description (continued)

Innovative circuit techniques are used on the TLC2652 and TLC2652A to allow exceptionally fast overload recovery time. If desired, an output clamp pin is available to reduce the recovery time even further.

The device inputs and output are designed to withstand ±100-mA surge currents without sustaining latch-up. Additionally the TLC2652 and TLC2652A incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

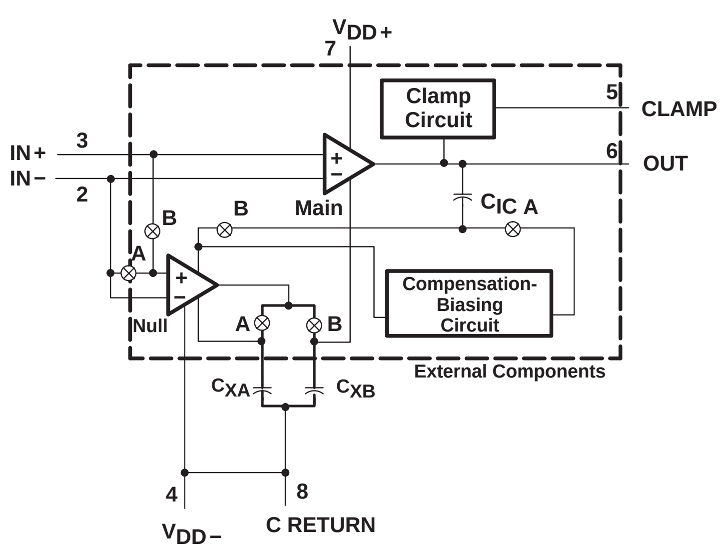
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The Q-suffix devices are characterized for operation from −40°C to125°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to125°C.

AVAILABLE OPTIONS(1)

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES							CHIP FORM (Y)
		8 PIN			14 PIN			20 PIN	
		SMALL OUTLINE (D008)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SMALL OUTLINE (D014)	CERAMIC DIP (J)	PLASTIC DIP (N)	CHIP CARRIER (FK)	
0°C to 70°C	1 µV 3 µV	TLC2652AC-8D TLC2652C-8D	— —	TLC2652ACP TLC2652CP	TLC2652AC-14D TLC2652C-14D	— —	TLC2652ACN TLC2652CN	— —	TLC2652Y
−40°C to 85°C	1 µV 3 µV	TLC2652AI-8D TLC2652A-8D	— —	TLC2652AIP TLC2652IP	TLC2652AI-14D TLC2652I-14D	— —	TLC2652AIN TLC2652IN	— —	—
−40°C to 125°C	3.5 µV	TLC2652Q-8D	—	—	—	—	—	—	—
−55°C to 125°C	3 µV 3.5 µV	TLC2652AM-8D TLC2652M-8D	TLC2652AMJG TLC2652MJG	TLC2652AMP TLC2652MP	TLC2652AM-14D TLC2652M-14D	TLC2652AMJ TLC2652MJ	TLC2652AMN TLC2652MN	TLC2652AMFK TLC2652MFK	—

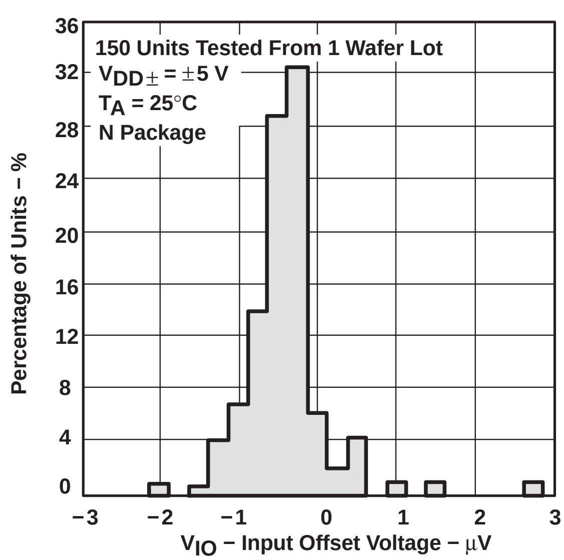
The D008 and D014 packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2652AC-8DR). Chips are tested at 25°C.
NOTE (1): For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

functional block diagram



Pin numbers shown are for the D (14 pin), JG, and N packages.

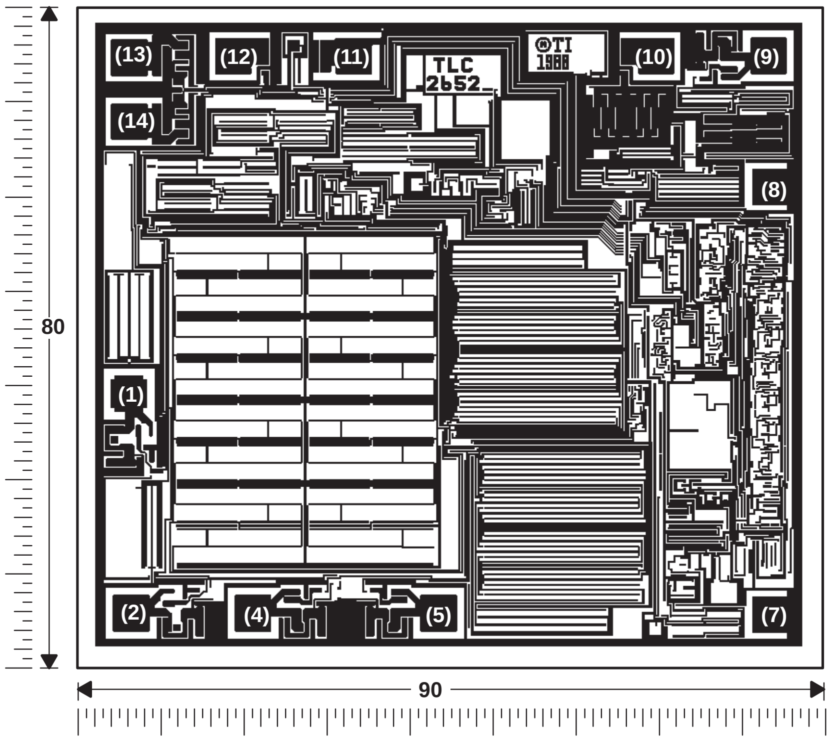
DISTRIBUTION OF TLC2652 INPUT OFFSET VOLTAGE



TLC2652Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2652C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (7) IS INTERNALLY CONNECTED TO BACK SIDE OF CHIP.

FOR THE PINOUT, SEE THE FUNCTIONAL BLOCK DIAGRAM.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage V_{DD+} (see Note 1) . . . 8 V
Supply voltage V_{DD-} (see Note 1) . . . −8 V
Differential input voltage, V_{ID} (see Note 2) . . . ±16 V
Input voltage, V_I (any input, see Note 1) . . . ±8 V
Voltage range on CLK IN and INT/$\overline{EXT}$ . . . V_{DD-} to V_{DD-} + 5.2 V
Input current, I_I (each input) . . . ±5 mA
Output current, I_O . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . unlimited
Current into CLK IN and INT/$\overline{EXT}$ . . . ±5 mA
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . 0°C to 70°C
I suffix . . . −40°C to 85°C
Q suffix . . . −40°C to 125°C
M suffix . . . −55°C to 125°C
Storage temperature range . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JG package . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D008	725 mV	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mV	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mV	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mV	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mV	8.4 mW/°C	672 mW	546 mW	210 mW
N	1575 mV	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mV	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±1.9	±8	±1.9	±8	±1.9	±8	±1.9	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −1.9	V_{DD-}	V_{DD+} −1.9	V_{DD-}	V_{DD+} −1.9	V_{DD-}	V_{DD+} −1.9	V
Clock input voltage	V_{DD-}	V_{DD-} +5	V_{DD-}	V_{DD-} +5	V_{DD-}	V_{DD-} +5	V_{DD-}	V_{DD-} +5	V
Operating free-air temperature, T_A	0	70	−40	85	−40	125	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD}\pm = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652C			TLC2652AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3		0.5	1	μV
			Full range			4.35			2.35	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06		0.003	0.02	μV/mo
I_{IO}	Input offset current		25°C		2	60		2	60	pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		4	60		4	60	pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	120	150		135	150		dB
			Full range	120			130			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm1.9$ V to ±8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	135		110	135		dB
			Full range	110			110			
I_{DD}	Supply current		25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

† Full range is 0° to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated at $T_A = 25°$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652C			TLC2652AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/µs
			Full range	1.5			1.5			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/µs
			Full range	1.8			1.8			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94			94	140	nV/√Hz
		f = 1 kHz	25°C		23			23	35	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		µV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 10 kHz	25°C		0.004			0.004		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
φm	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is 0° to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD}\pm = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652I			TLC2652AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3		0.5	1	μV
			Full range			4.95			2.95	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06		0.003	0.02	μV/mo
I_{IO}	Input offset current		25°C		2	60		2	60	pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		4	60		4	60	pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 10$ kΩ	25°C	120	150		135	150		dB
			Full range	120			125			
	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm1.9$ V to ±8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	135		110	135		dB
			Full range	110			110			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

† Full range is −40° to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated at $T_A = 25$° using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652I			TLC2652AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/µs
			Full range	1.4			1.4			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/µs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94			94	140	nV/√Hz
		f = 1 kHz	25°C		23			23	35	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		µV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕm	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is −40° to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD}\pm = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652Q TLC2652M			TLC2652AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 7)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3.5		0.5	3	μV
			Full range			10			8	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03*		0.003	0.03*	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06*		0.003	0.02*	μV/mo
I_{IO}	Input offset current		25°C		2	60		2	60	pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		4	60		4	60	pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	120	150		135	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$V_O = -5$ V to 5 V	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$R_L = 100$ kΩ	25°C			100			100	pA
			Full range			500			500	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	135		110	135		dB
			Full range	110			110			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Full range is −40° to 125°C for Q suffix, −55° to 125°C for M suffix.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated at $T_A = 25°$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.
7. This parameter is not production tested. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652Q TLC2652M TLC2652AM MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		V/µs
			Full range	1.3			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		V/µs
			Full range	1.6			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		94		nV/√Hz
		f = 1 kHz	25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8		µV
		f = 0 to 10 Hz	25°C		2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°		

† Full range is −40° to 125°C for the Q suffix, −55° to 125°C for the M suffix.

electrical characteristics at $V_{DD\pm} = \pm 5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2652Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$R_S = 50\ \Omega$		0.6	3	µV
	Input offset voltage long-term drift (see Note 4)				0.003	0.006	µV/mo
I_{IO}	Input offset current				2	60	pA
I_{IB}	Input bias current				4	60	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ,	See Note 5	4.7	4.8		V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ,	See Note 5	−4.7	−4.9		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V,	$R_L = 10$ kΩ	120	150		dB
f_{ch}	Internal chopping frequency				450		Hz
	Clamp on-state current	$R_L = 100$ kΩ		25			µA
	Clamp off-state current	$V_O = -4$ V to 4 V				100	pA
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = V_{ICR}$min,	120	140		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $R_S = 50\ \Omega$	$V_O = 0$,	110	135		dB
I_{DD}	Supply current	$V_O = 0$,	No load		1.5	2.4	mA

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated at $T_A = 25°$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at $V_{DD\pm} = \pm 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TLC2652Y			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $C_L = 100$ pF	$R_L = 10$ kΩ,	2	2.8		V/µs
SR−	Negative slew rate at unity gain			2.3	3.1		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			94		nV/√Hz
		f = 1 kHz			23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz			0.8		µV
		f = 0 to 10 Hz			2.8		
I_n	Equivalent input noise current	f = 1 kHz					pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF	$R_L = 10$ kΩ,		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ,	$C_L = 100$ pF		48°		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Normalized input offset voltage	vs Chopping frequency	1
I_{IB}	Input bias current	vs Common-mode input voltage vs Chopping frequency vs Free-air temperature	2 3 4
I_{IO}	Input offset current	vs Chopping frequency vs Free-air temperature	5 6
	Clamp current	vs Output voltage	7
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	8
V_{OM}	Maximum peak output voltage	vs Output current vs Free-air temperature	9, 10 11, 12
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	13 14
	Chopping frequency	vs Supply voltage vs Free-air temperature	15 16
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	19 20
SR	Slew rate	vs Supply voltage vs Free-air temperature	21 22
	Voltage-follower pulse response	Small-signal Large-signal	23 24
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	28 29
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	30 31 32
	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

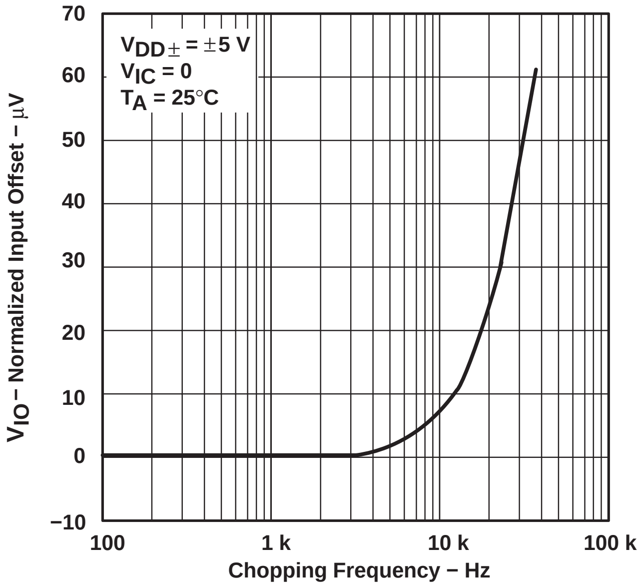


Figure 1

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

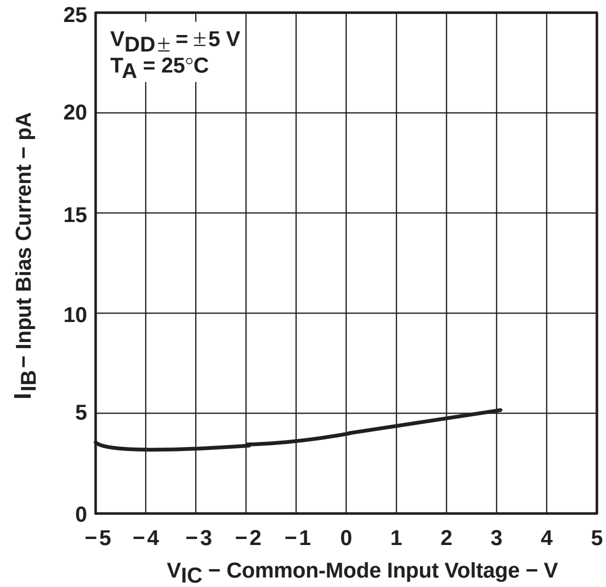


Figure 2

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

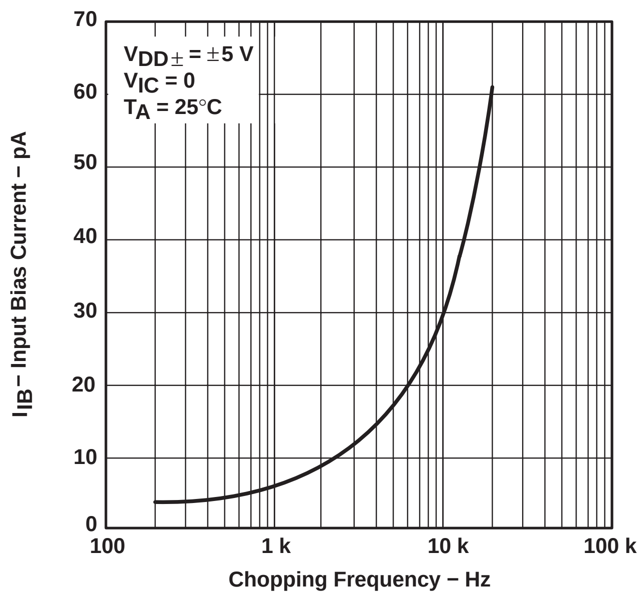


Figure 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

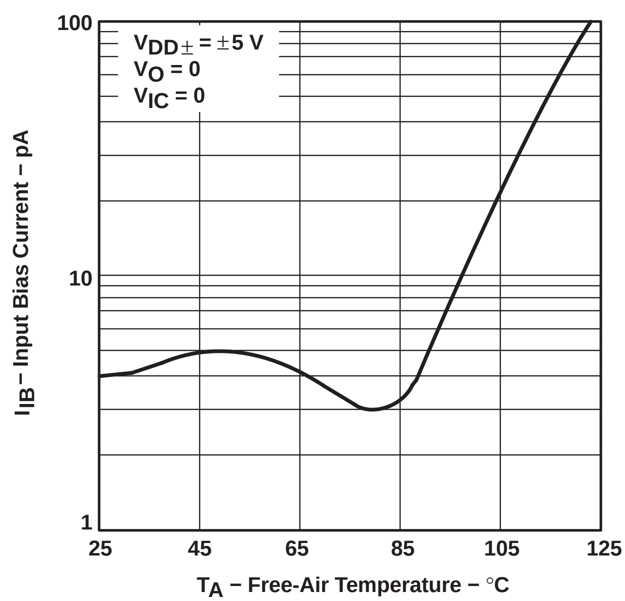


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

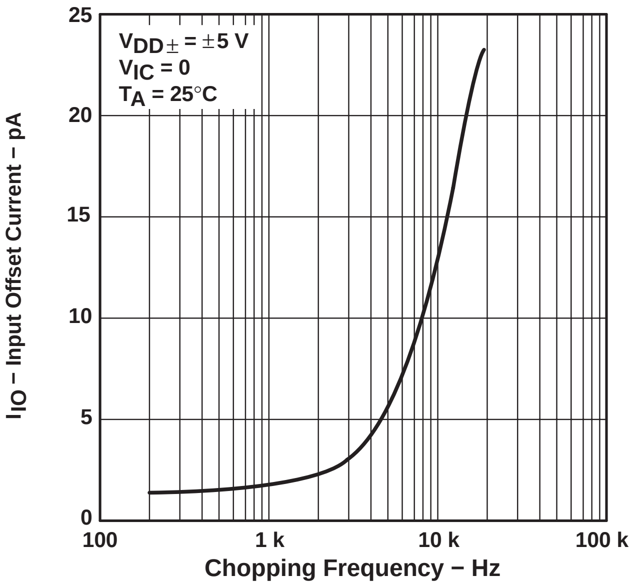


Figure 5

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

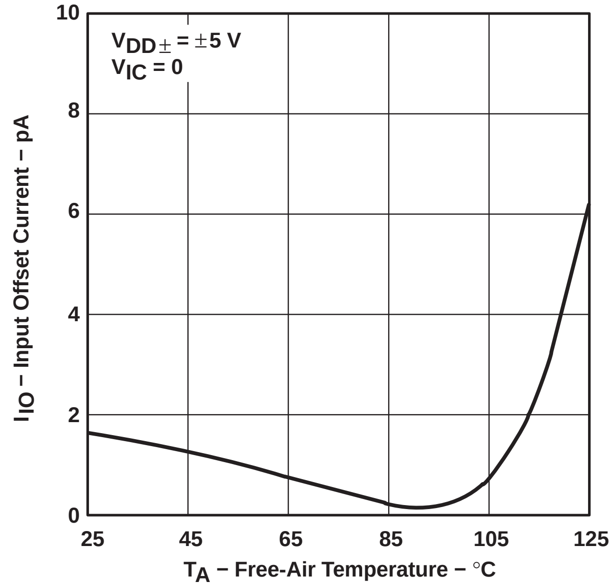


Figure 6

CLAMP CURRENT
vs
OUTPUT VOLTAGE

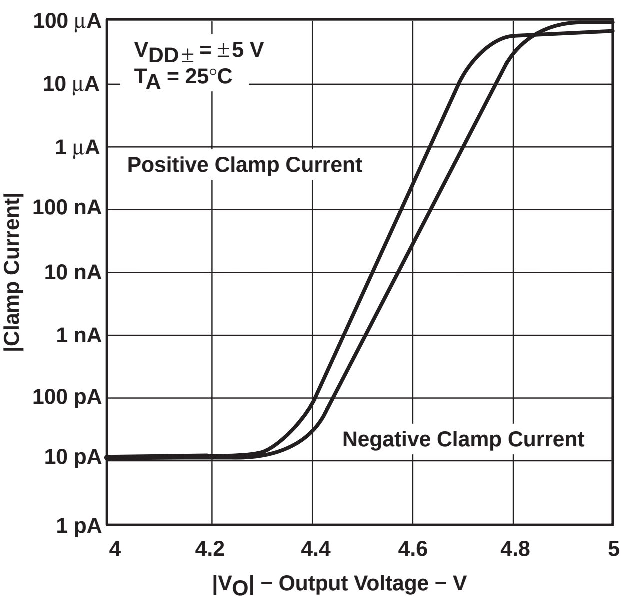


Figure 7

MAXIMUM PEAK-TO-PEAK OUTPUT
VOLTAGE
vs
FREQUENCY

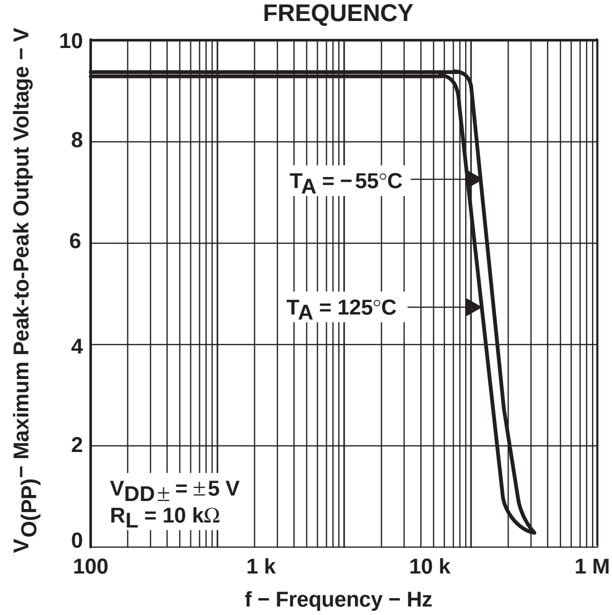


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

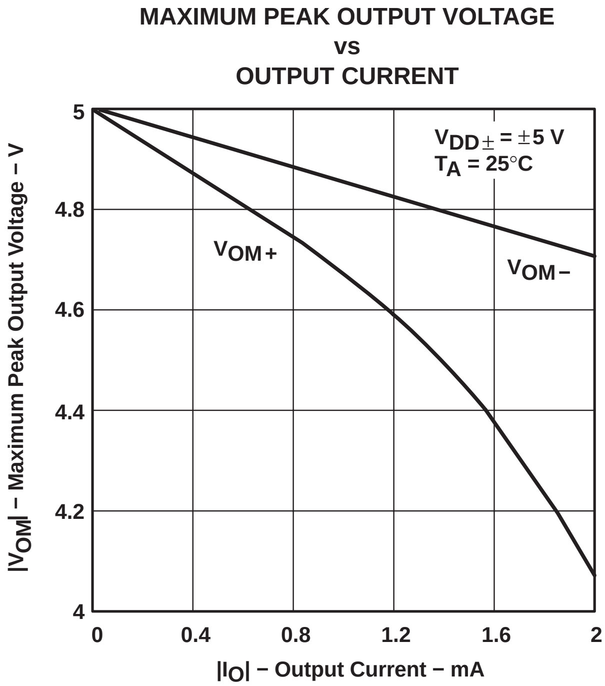


Figure 9

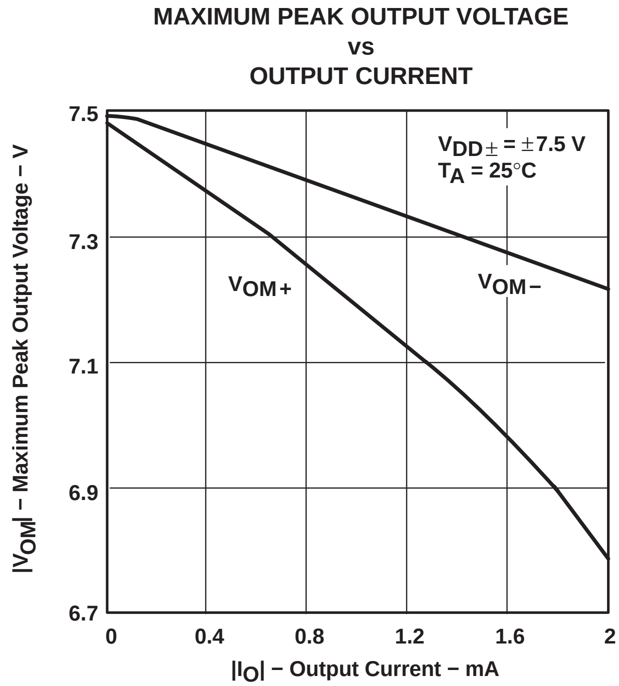


Figure 10

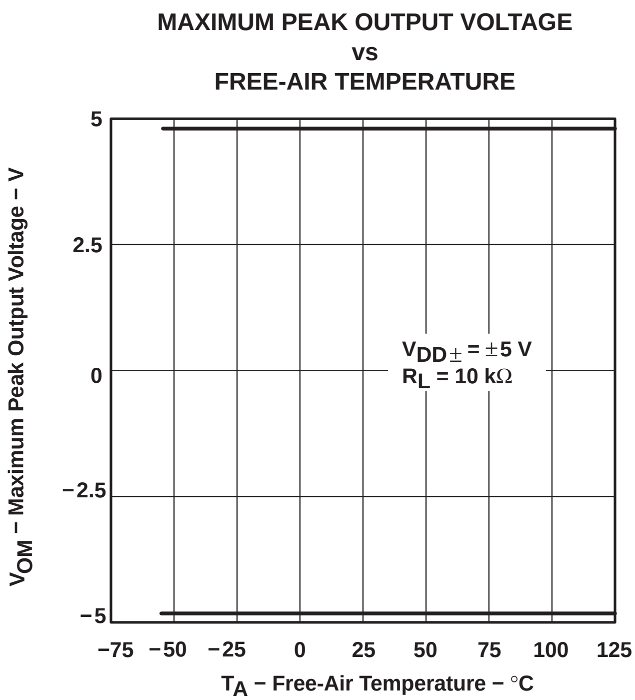


Figure 11

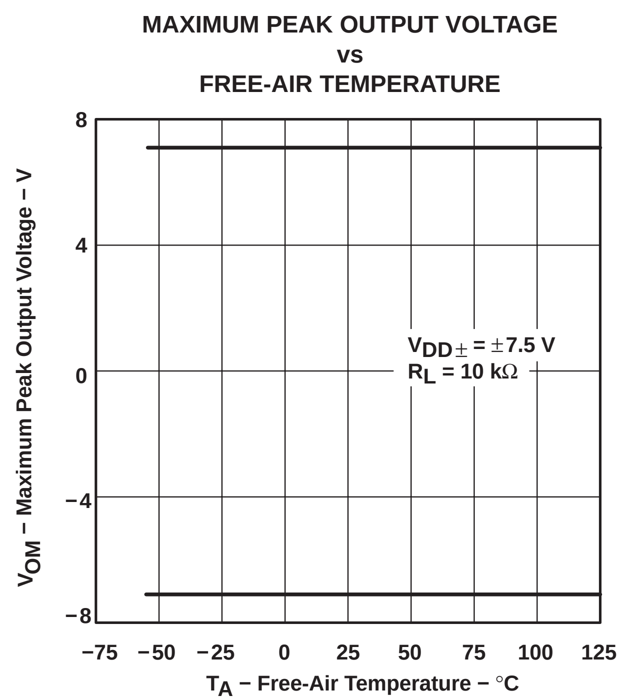


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

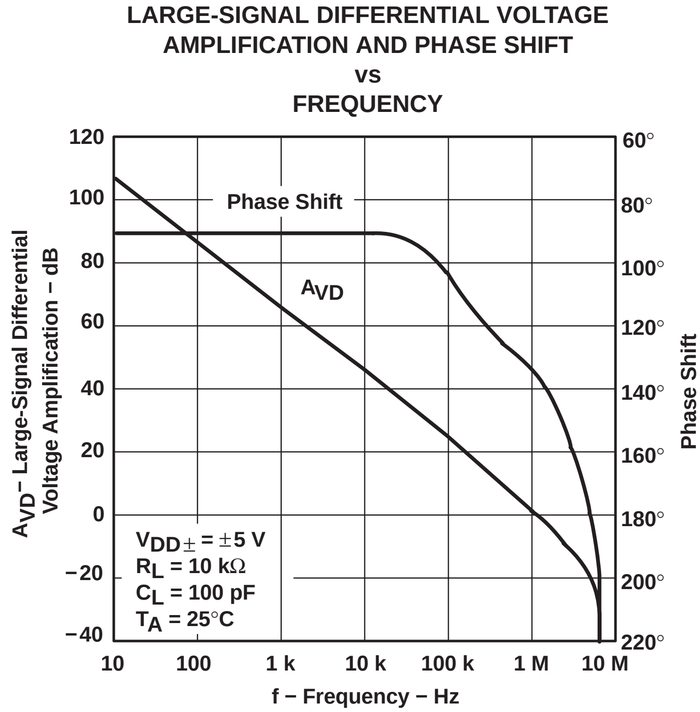


Figure 13

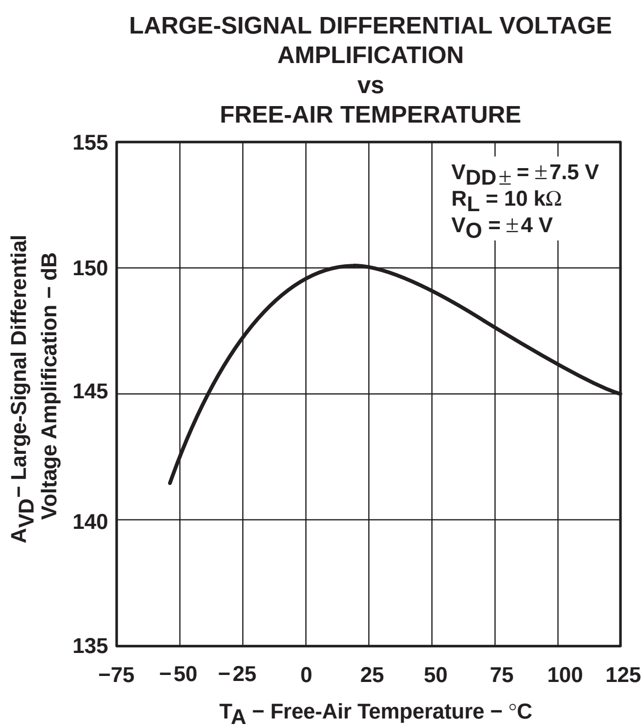


Figure 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

CHOPPING FREQUENCY
vs
SUPPLY VOLTAGE

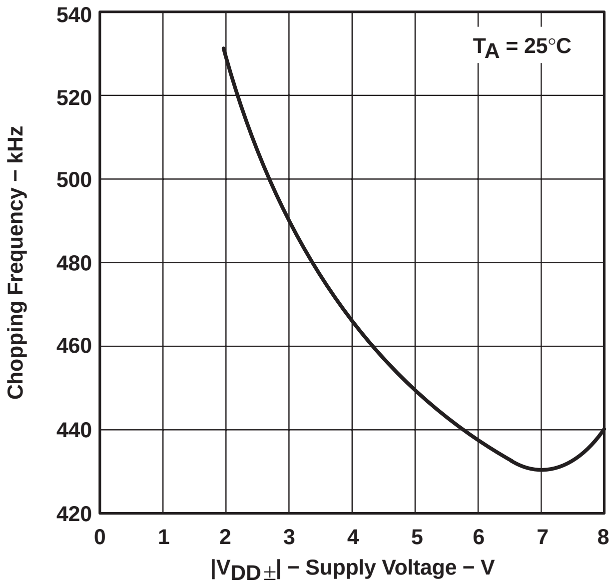


Figure 15

CHOPPING FREQUENCY
vs
FREE-AIR TEMPERATURE

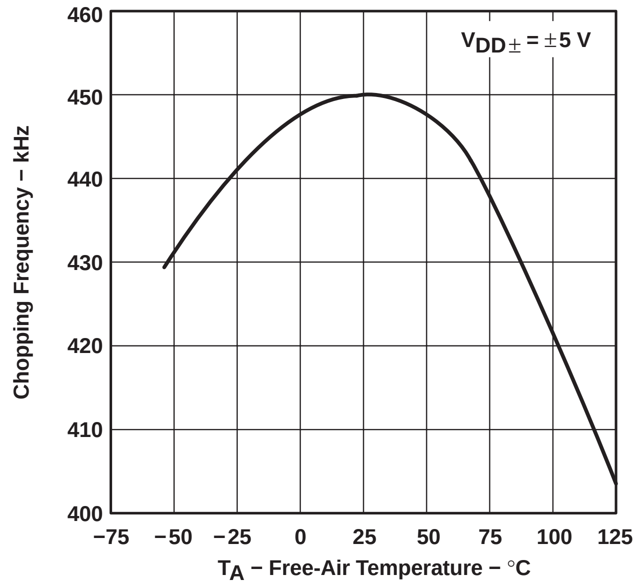


Figure 16

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

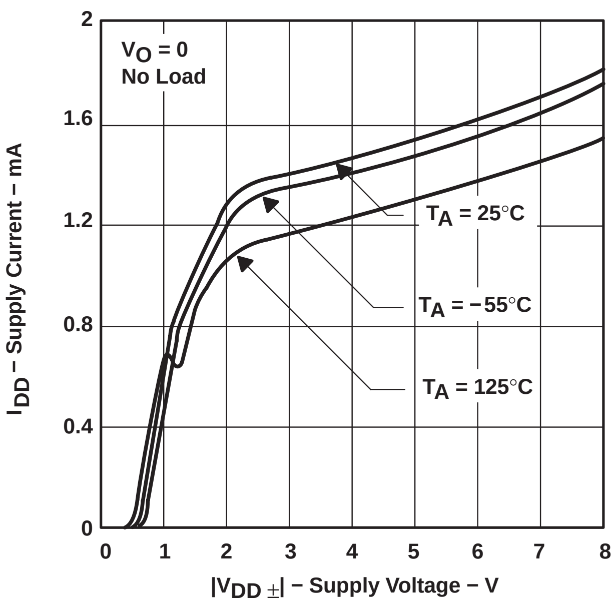


Figure 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

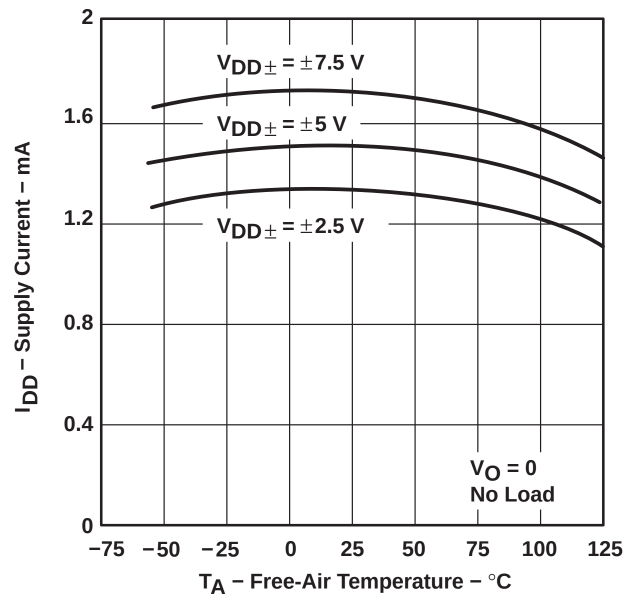


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

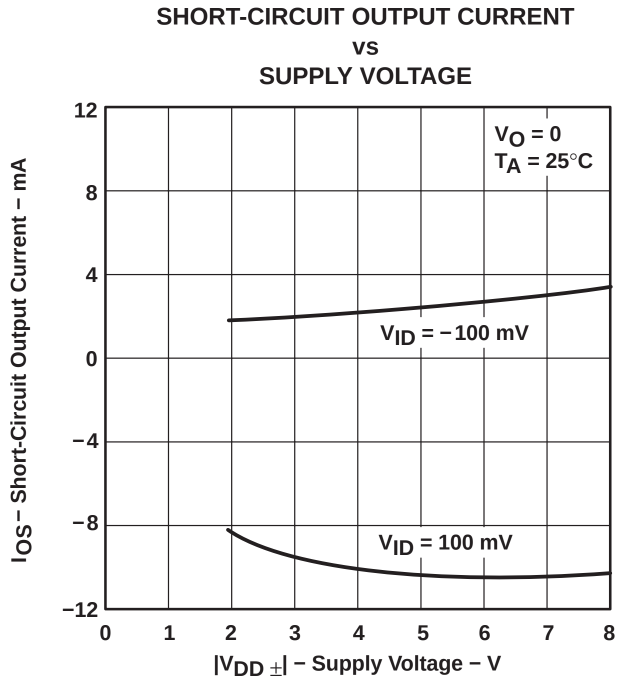


Figure 19

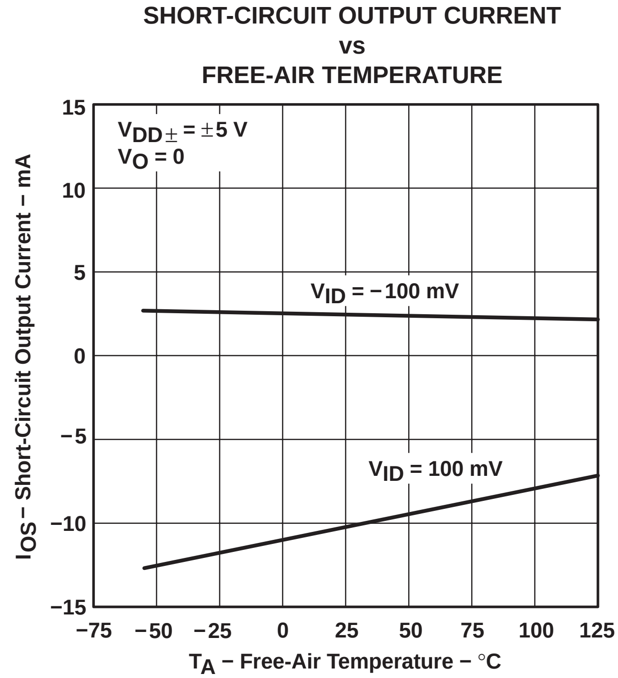


Figure 20

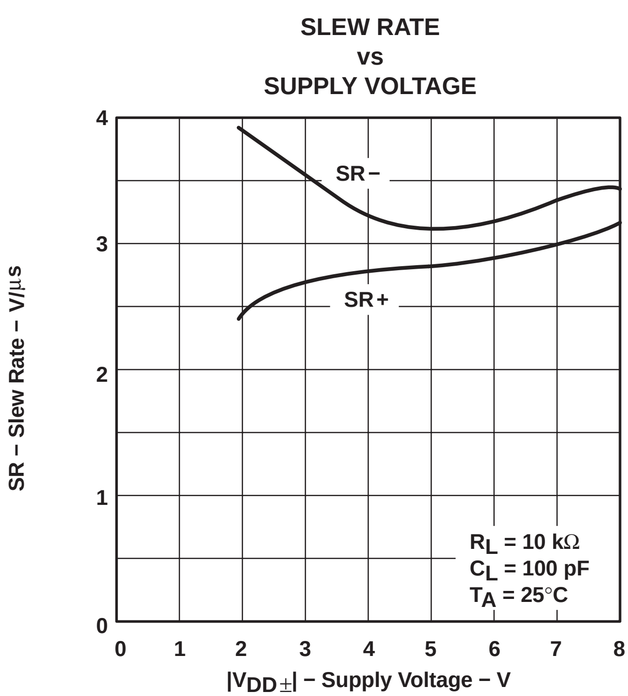


Figure 21

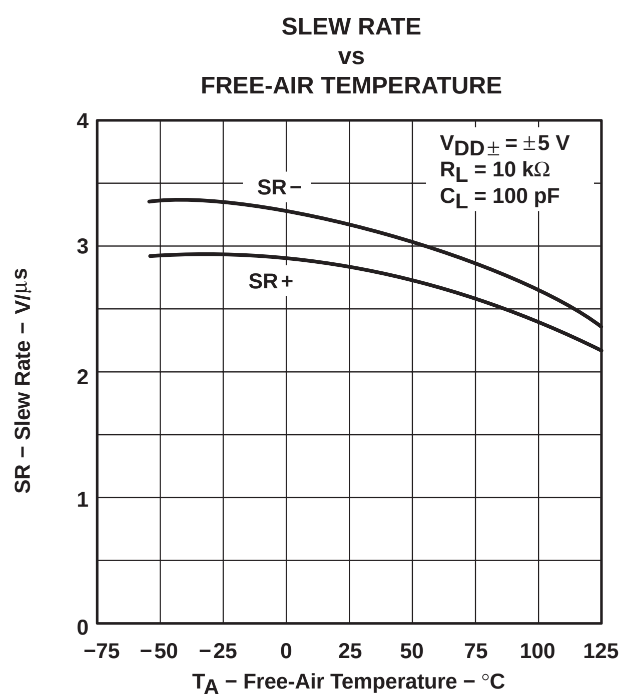


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

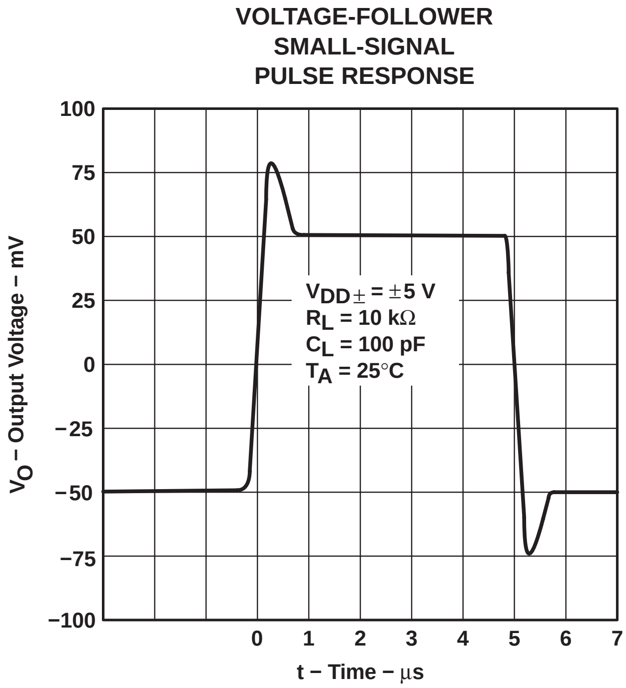


Figure 23

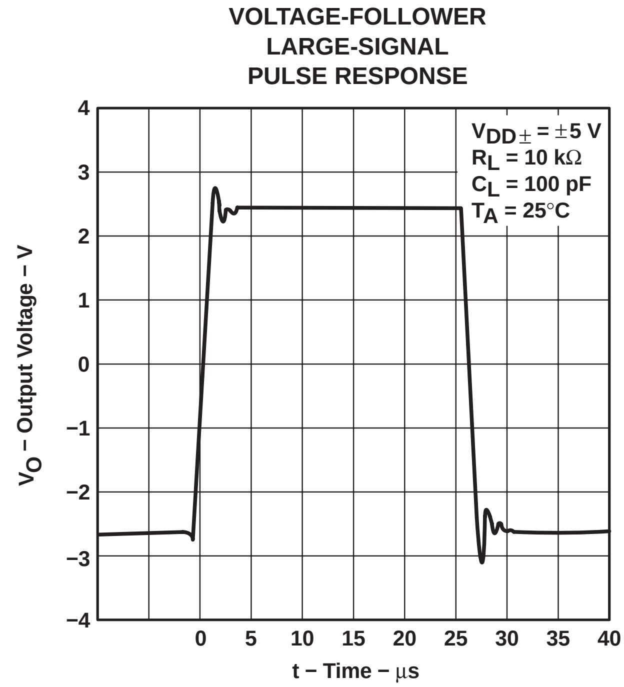


Figure 24

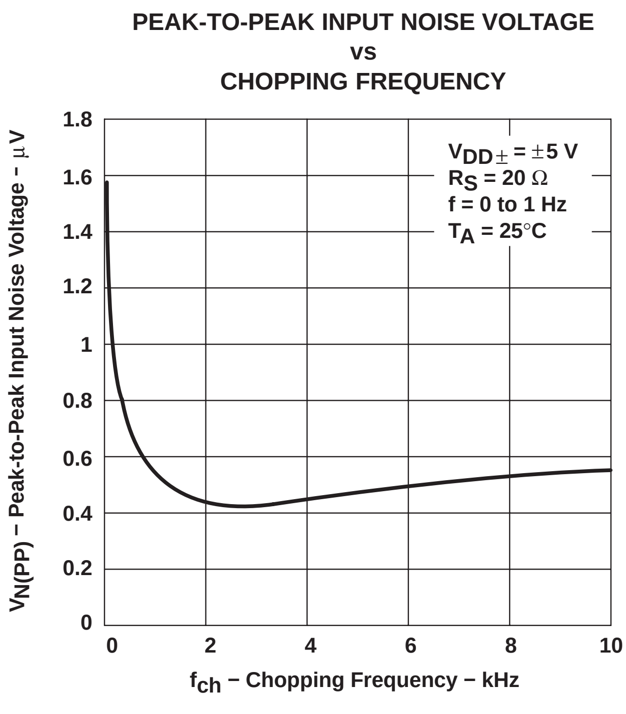


Figure 25

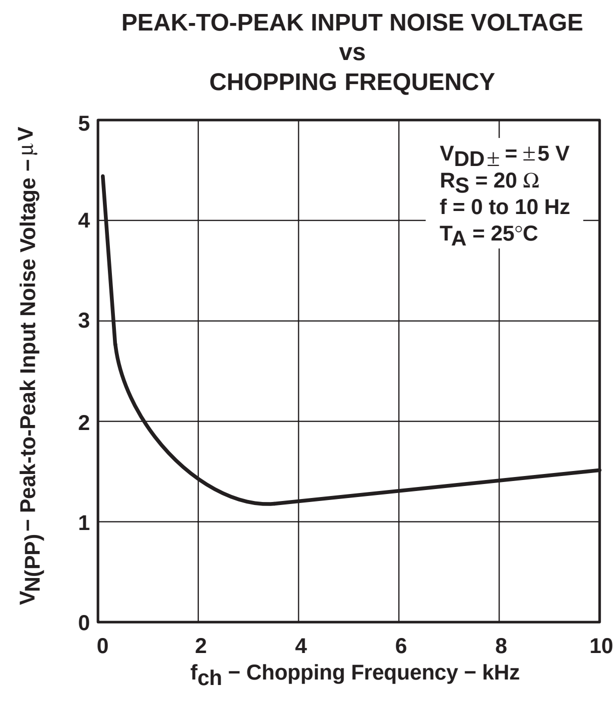


Figure 26

TYPICAL CHARACTERISTICS†

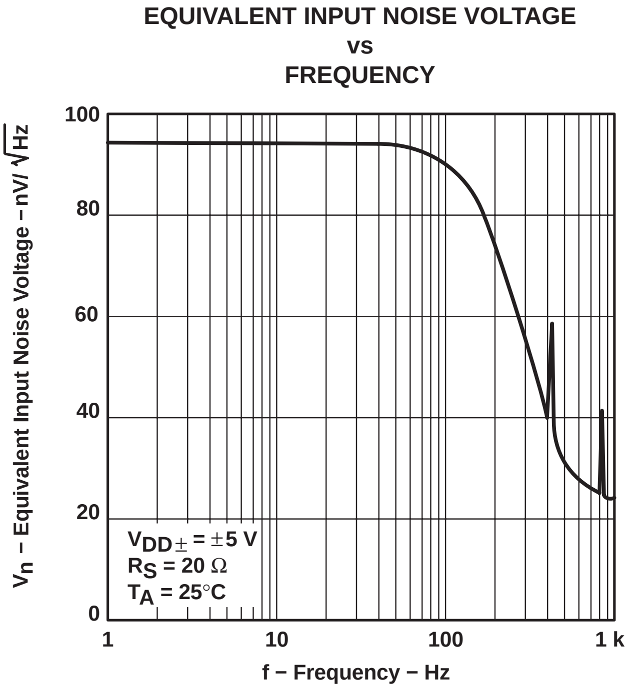


Figure 27

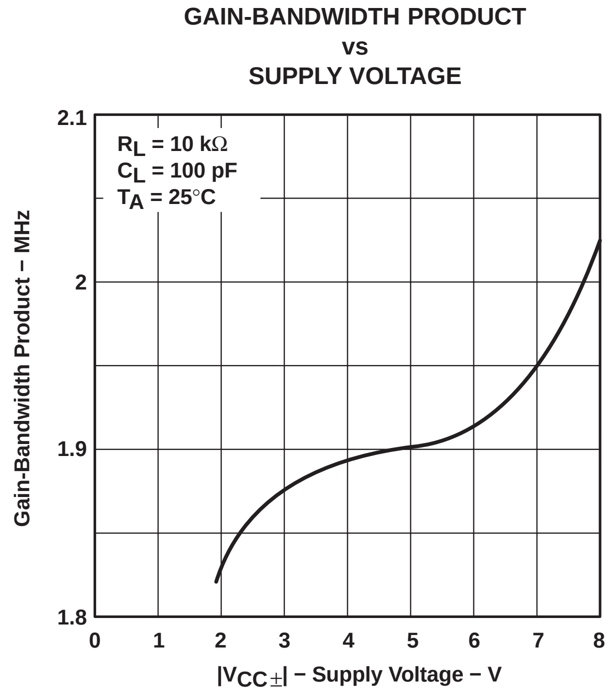


Figure 28

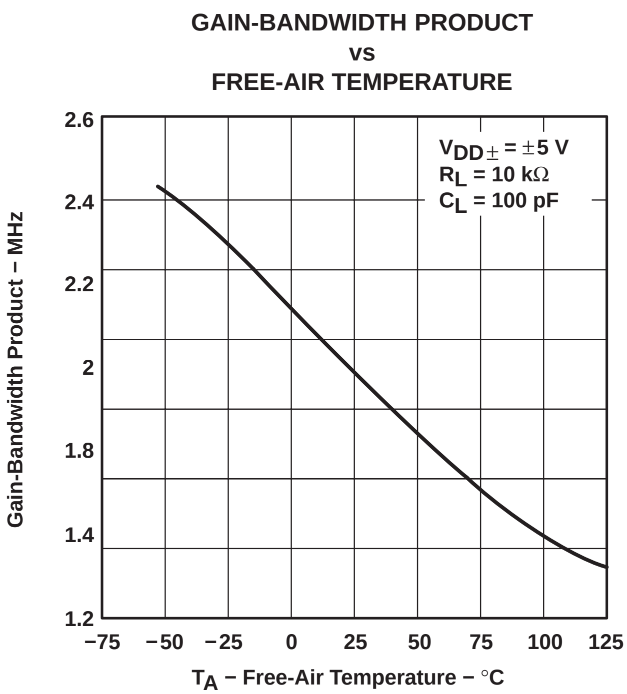


Figure 29

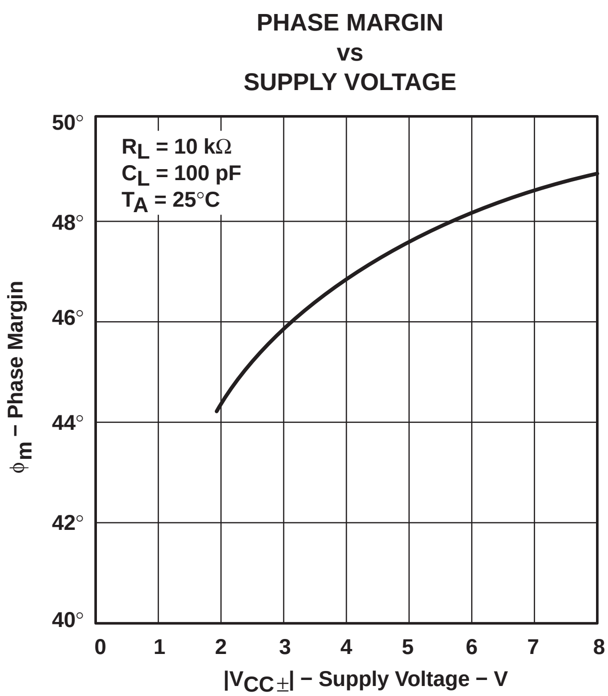


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

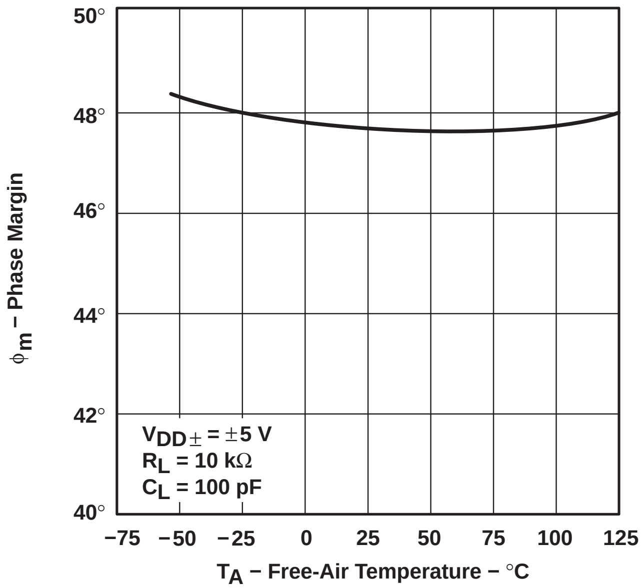


Figure 31

PHASE MARGIN
vs
LOAD CAPACITANCE

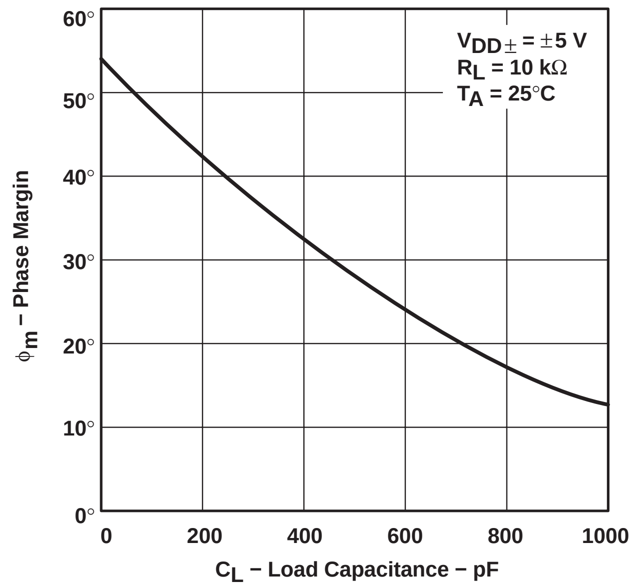


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

capacitor selection and placement

The two important factors to consider when selecting external capacitors C_{XA} and C_{XB} are leakage and dielectric absorption. Both factors can cause system degradation, negating the performance advantages realized by using the TLC2652.

Degradation from capacitor leakage becomes more apparent with the increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guard bands are recommended around the capacitor connections on both sides of the printed circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset voltage is needed, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor can suffice.

Unlike many choppers available today, the TLC2652 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either V_{DD-} or C RETURN. On many choppers, connecting these capacitors to V_{DD-} causes degradation in noise performance. This problem is eliminated on the TLC2652.

APPLICATION INFORMATION

internal/external clock

The TLC2652 has an internal clock that sets the chopping frequency to a nominal value of 450 Hz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency can be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 450-Hz clock, no connection is necessary. If external clocking is desired, connect INT/$\overline{\text{EXT}}$ to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, CLK IN can be driven from the negative rail to 5 V above the negative rail. If this level is exceeded, damage could occur to the device unless the current into CLK IN is limited to ±5 mA. When operating in the single-supply configuration, this feature allows the TLC2652 to be driven directly by 5-V TTL and CMOS logic. A divide-by-two frequency divider interfaces with CLK IN and sets the clock chopping frequency. The duty cycle of the external clock is not critical but should be kept between 30% and 60%.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2652, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2652 is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through CLAMP if required.

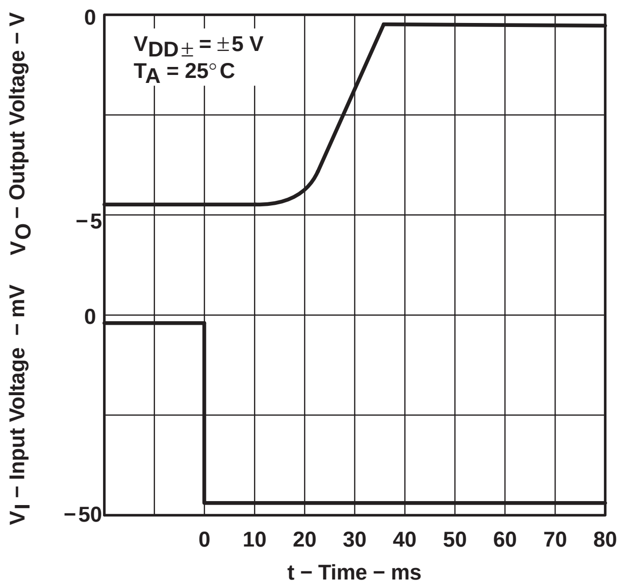


Figure 33. Overload Recovery

The clamp is a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced, and the TLC2652 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 7), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage drift of the TLC2652, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-µV/°C typical of the TLC2652).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit-board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

APPLICATION INFORMATION

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2652 inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques to reduce the chance of latch-up should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latch-up occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2652 incorporates internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers, a main amplifier and a nulling amplifier, plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2652 on-chip control logic produces two dominant clock phases: a nulling phase and an amplifying phase. The term chopper-stabilized derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2652. Switches A and B are make-before-break types.

During the nulling phase, switch A is closed shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

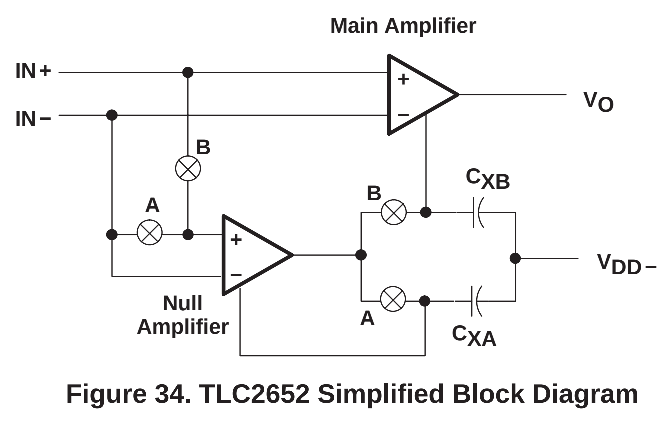


Figure 34. TLC2652 Simplified Block Diagram

APPLICATION INFORMATION

theory of operation (continued)

During the amplifying phase, switch B is closed connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2652 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2652 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9089501MPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	9089501MPA TLC2652M	Samples
5962-9089503MCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9089503MC A TLC2652AMJB	Samples
5962-9089503MPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	9089503MPA TLC2652AM	Samples
TLC2652AC-14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652AC	Samples
TLC2652AC-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652AC	Samples
TLC2652ACN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type		TLC2652ACN	Samples
TLC2652ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type		TLC2652AC	Samples
TLC2652AI-14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652AI	Samples
TLC2652AI-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652AI	Samples
TLC2652AI-8DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652AI	Samples
TLC2652AIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type		TLC2652AIN	Samples
TLC2652AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type		TLC2652AI	Samples
TLC2652AMJB	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9089503MC A TLC2652AMJB	Samples
TLC2652AMJG	ACTIVE	CDIP	JG	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	TLC2652 AMJG	Samples
TLC2652AMJGB	ACTIVE	CDIP	JG	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	9089503MPA TLC2652AM	Samples
TLC2652C-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2652C-8DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652C	Samples
TLC2652C-8DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652C	Samples
TLC2652CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type		TLC2652CN	Samples
TLC2652CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type		TLC2652CP	Samples
TLC2652I-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652I	Samples
TLC2652I-8DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2652I	Samples
TLC2652IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type		TLC2652IP	Samples
TLC2652M-8DG4	ACTIVE	SOIC	D	8	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		T2652M	Samples
TLC2652MJG	ACTIVE	CDIP	JG	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	TLC2652MJG	Samples
TLC2652MJGB	ACTIVE	CDIP	JG	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	9089501MPA TLC2652M	Samples
TLC2652Q-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2652Q	Samples
TLC2652Q-8DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		T2652Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

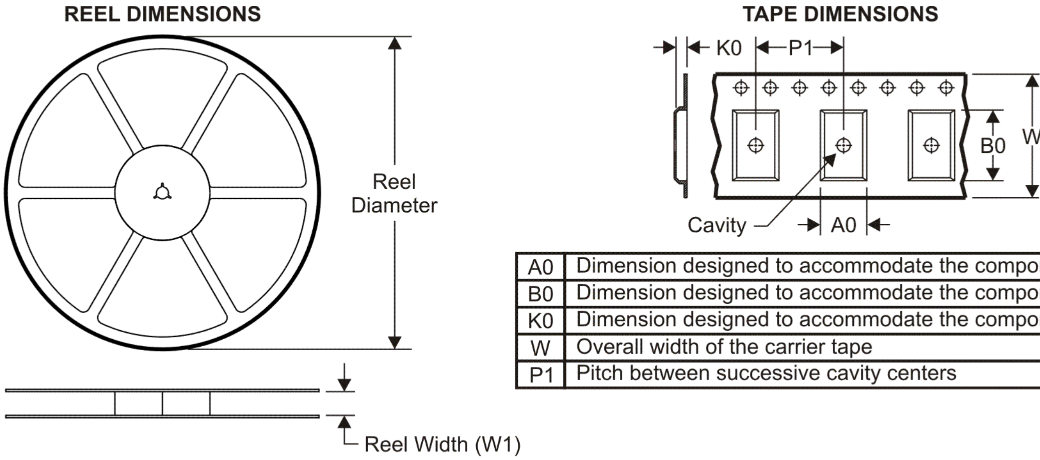
OTHER QUALIFIED VERSIONS OF TLC2652, TLC2652A, TLC2652AM, TLC2652M :

- Catalog: TLC2652A, TLC2652
- Military: TLC2652M, TLC2652AM

NOTE: Qualified Version Definitions:

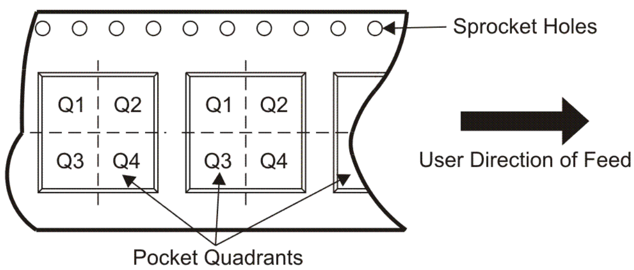
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

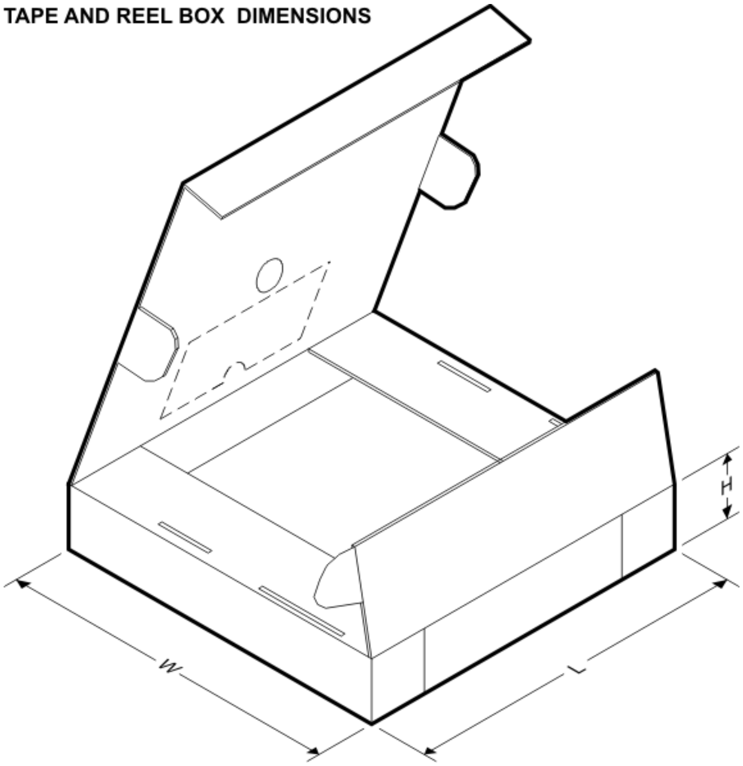
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2652AI-8DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2652C-8DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2652I-8DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

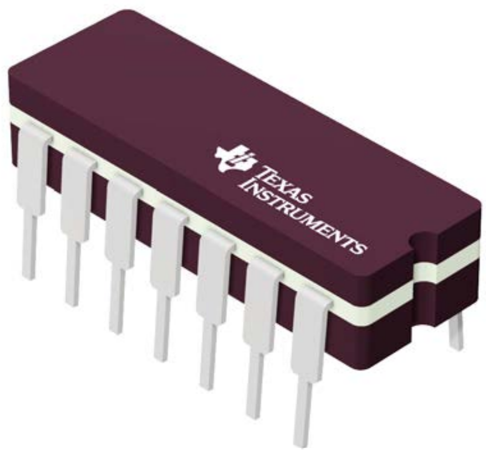


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2652AI-8DR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2652C-8DR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2652I-8DR	SOIC	D	8	2500	340.5	338.1	20.6

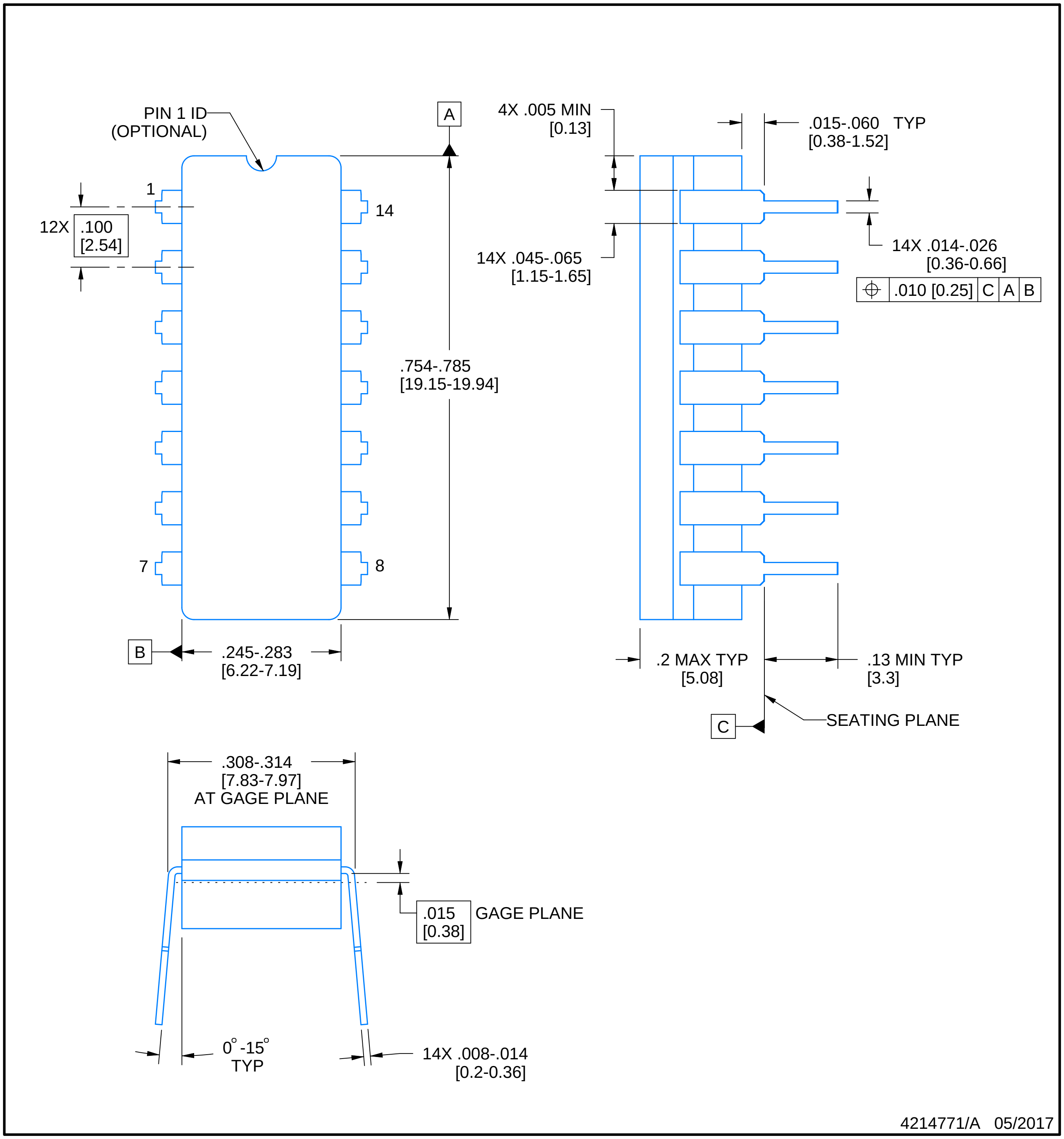
J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



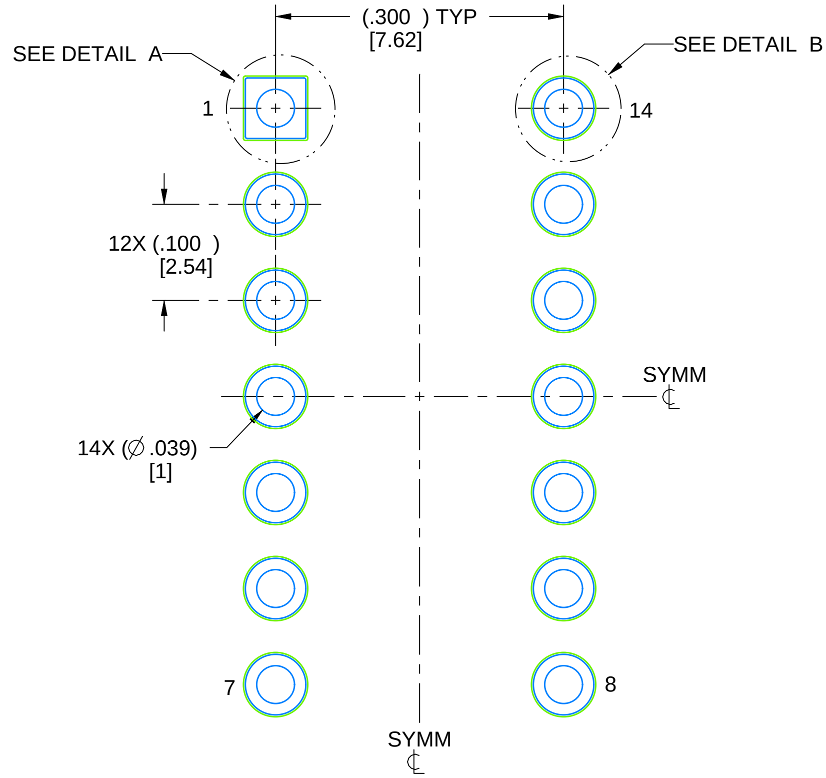
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

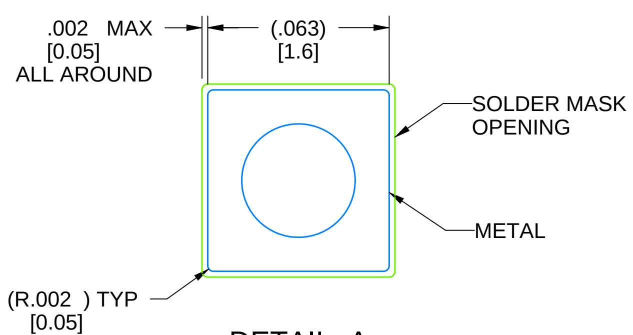


NOTES:

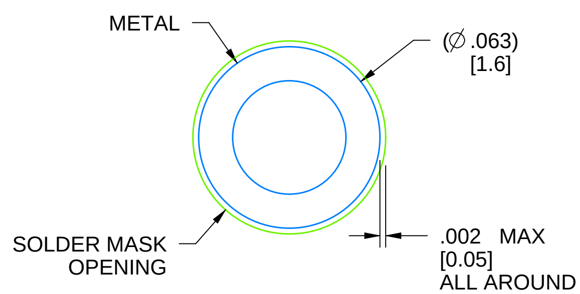
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



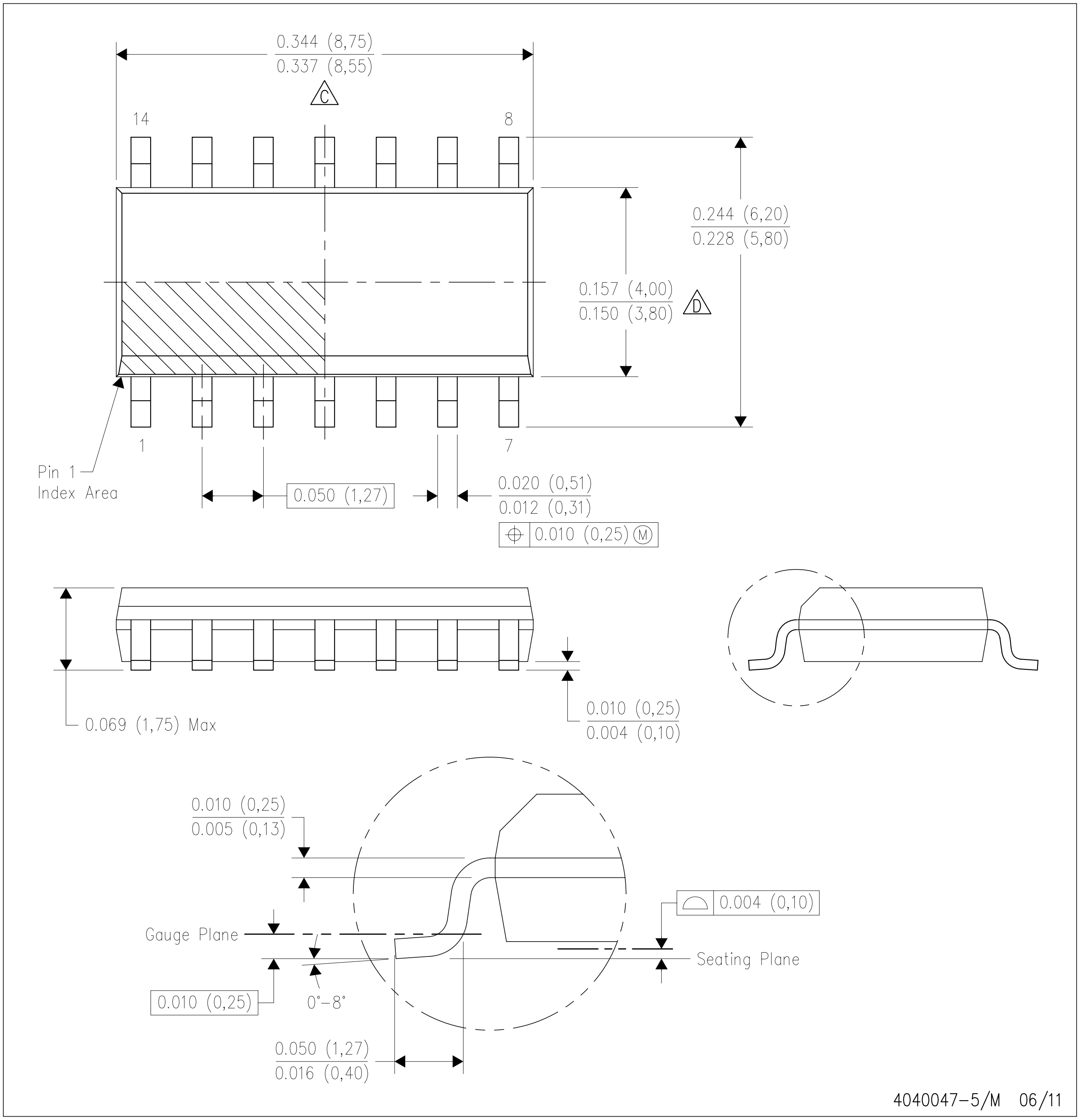
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

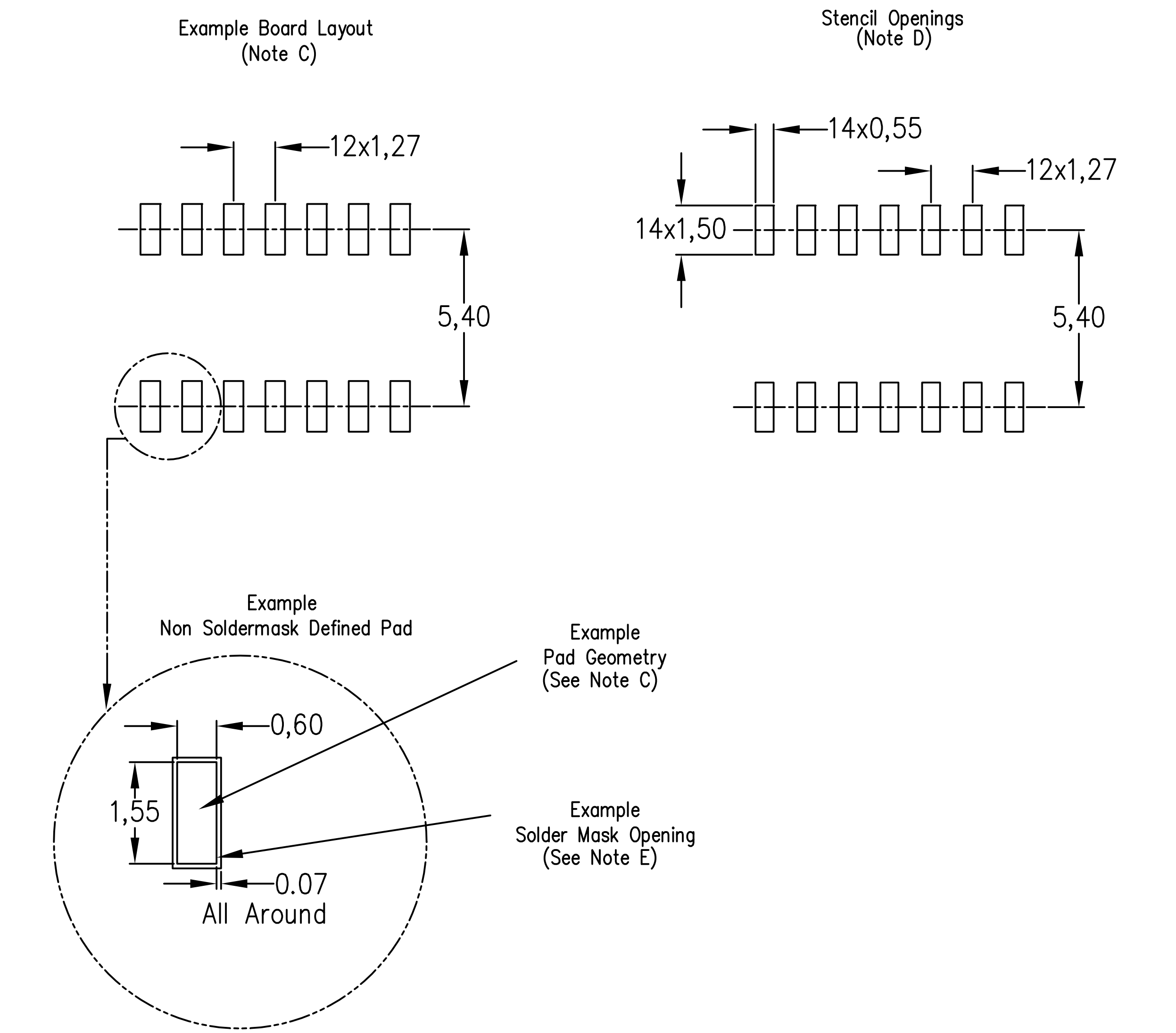
4214771/A 05/2017

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



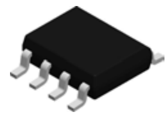
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4211283–3/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

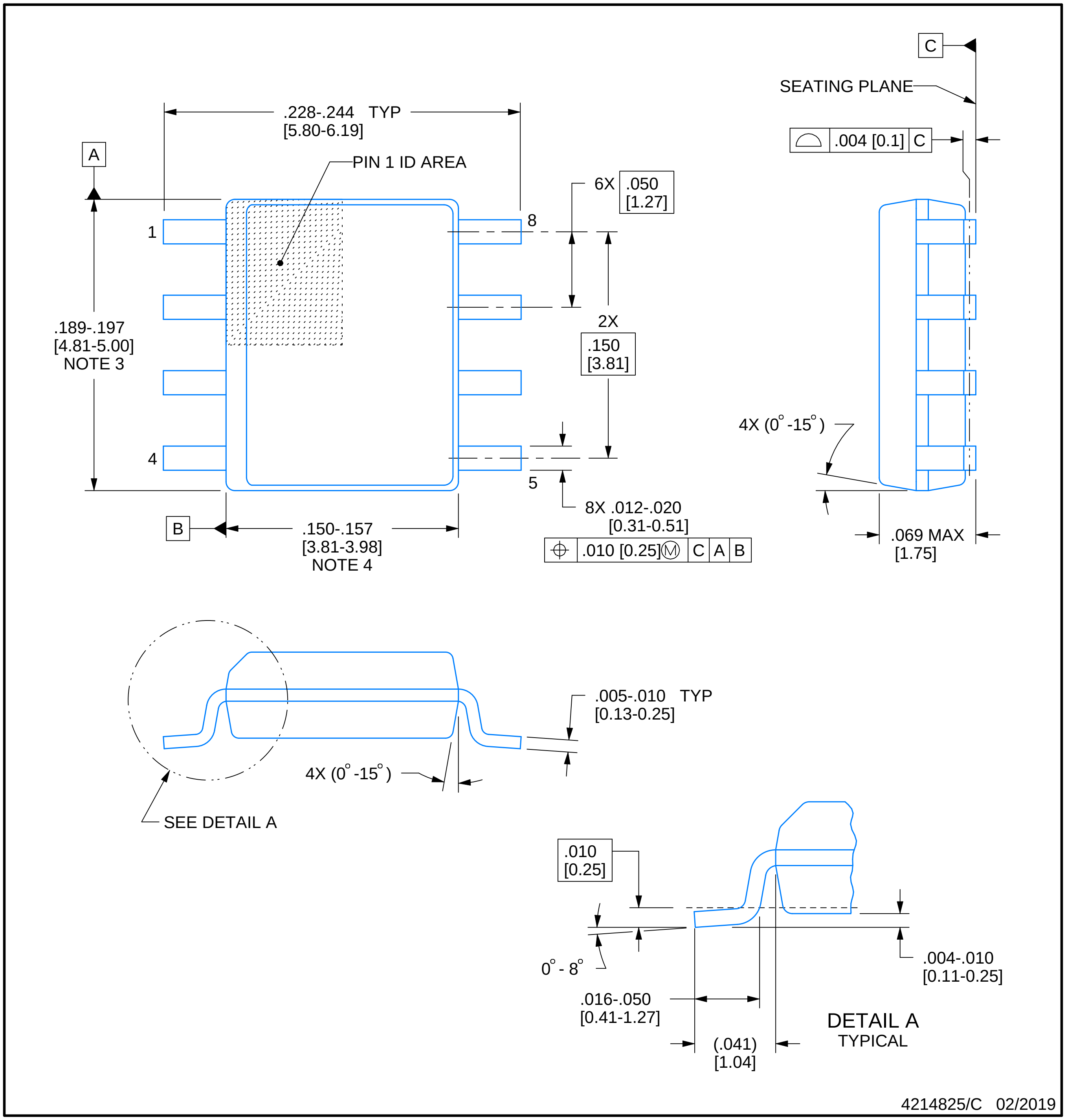


PACKAGE OUTLINE

D0008A

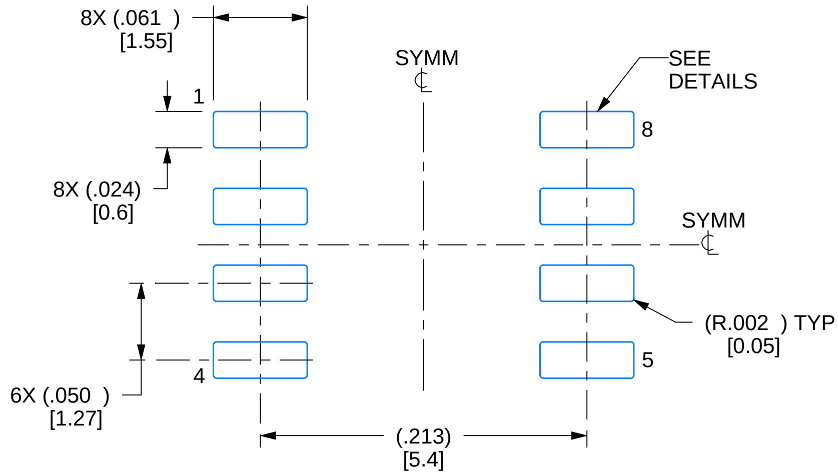
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

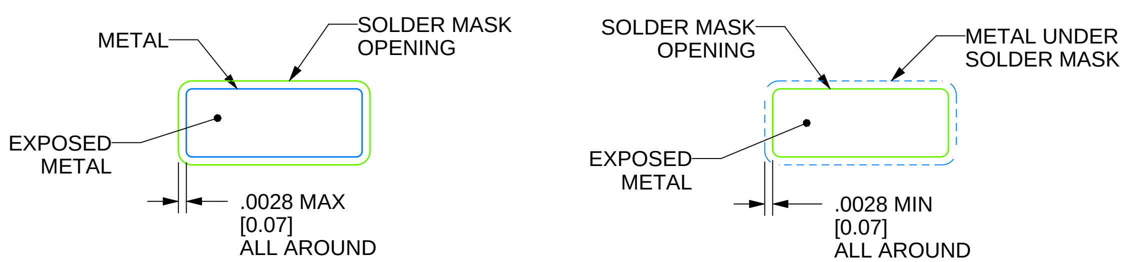


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

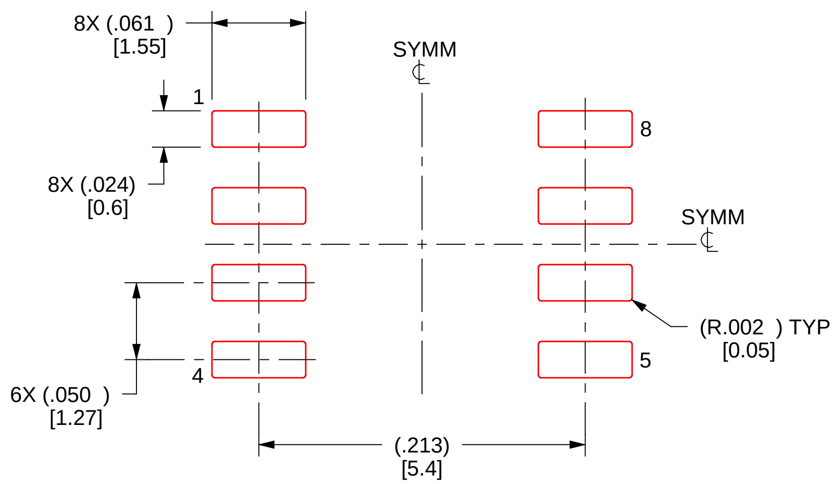
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



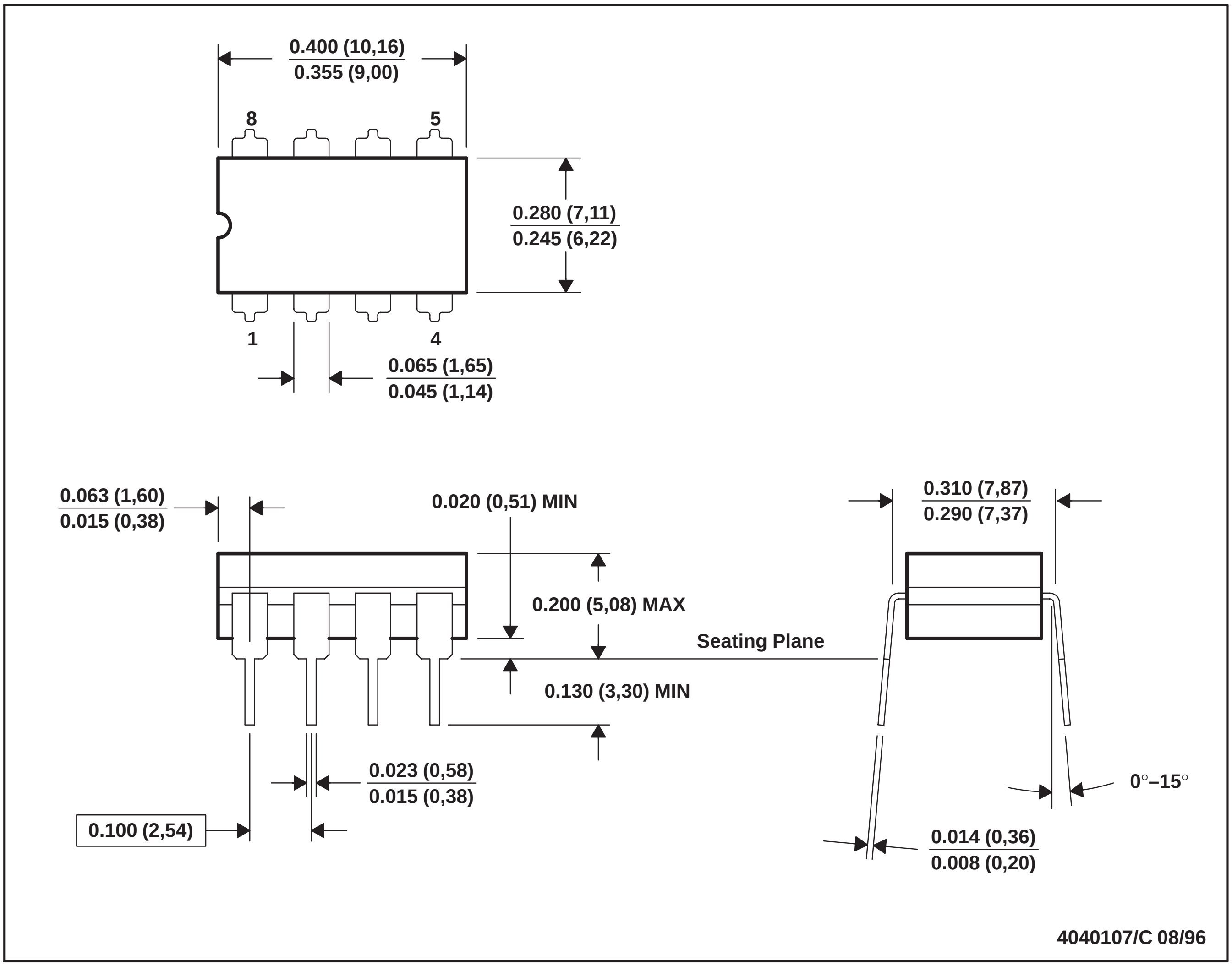
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

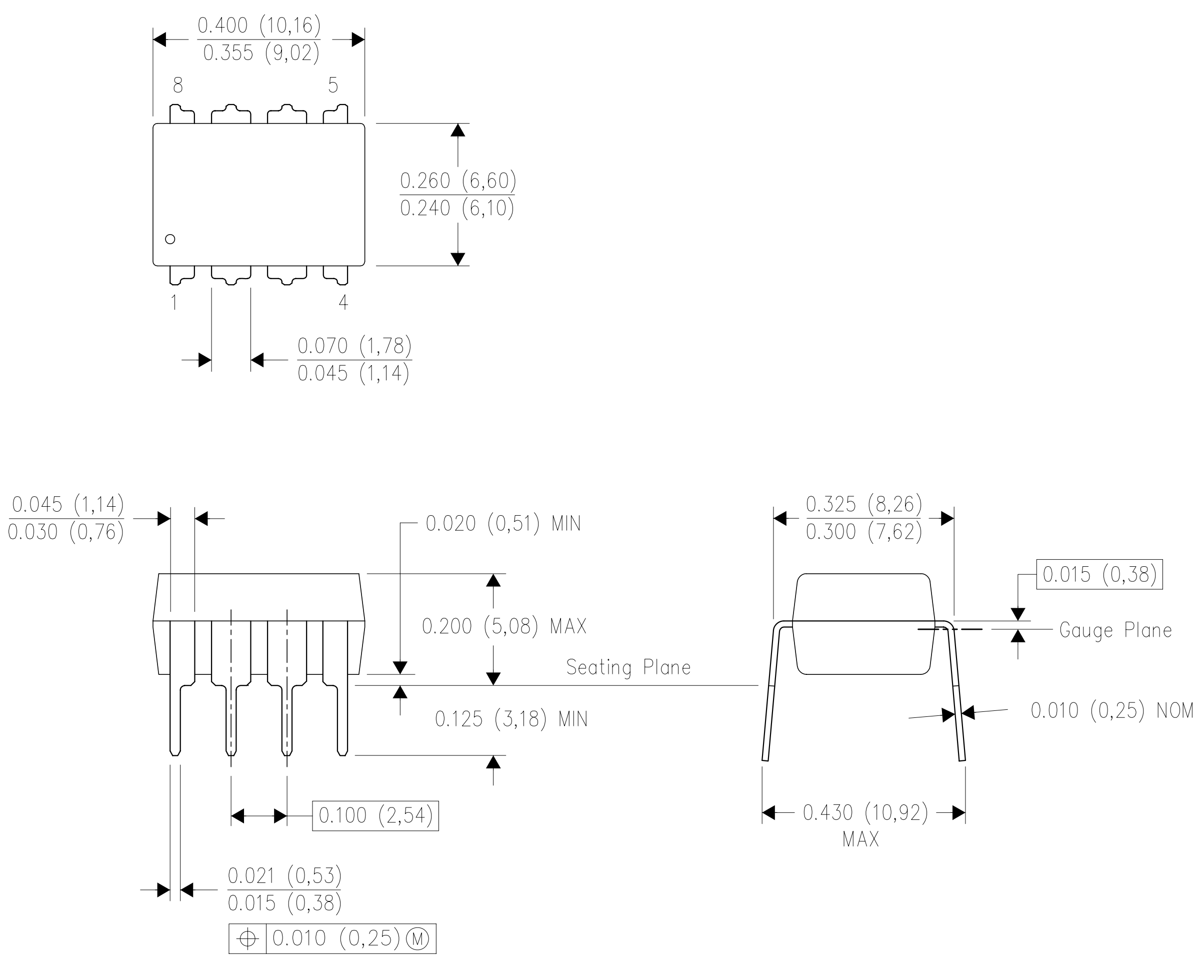
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE

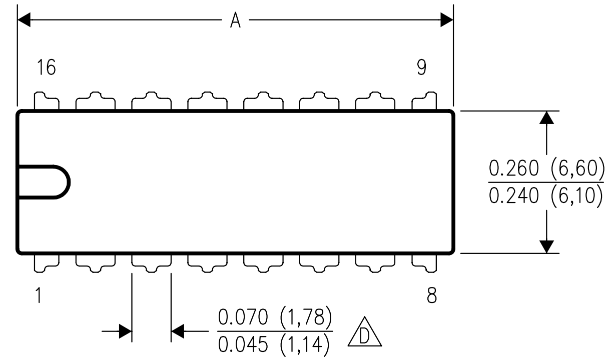


4040082/E 04/2010

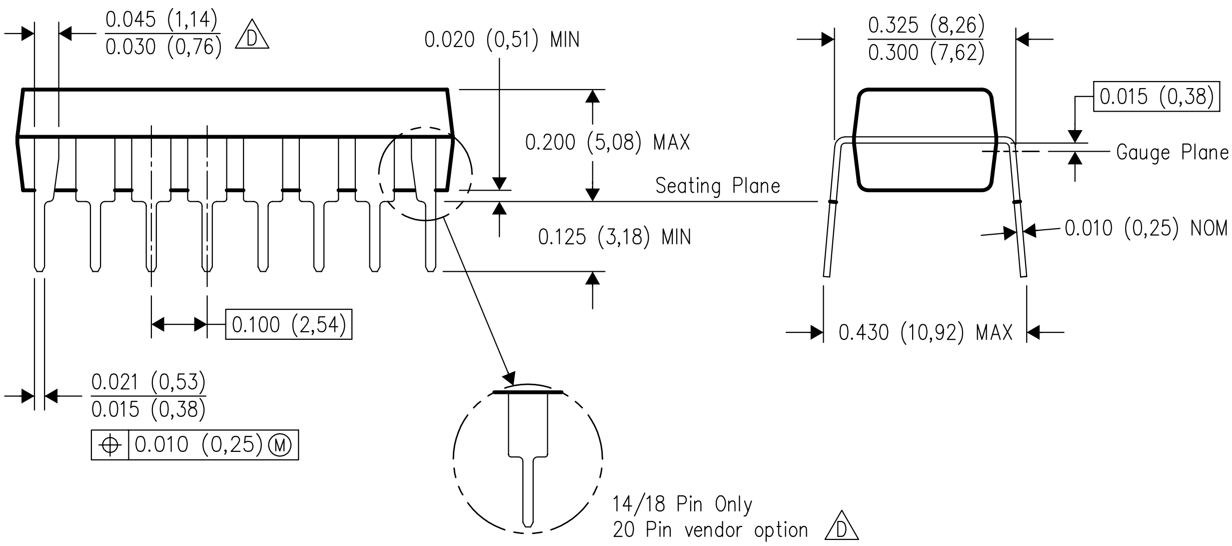
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- (C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.