LM5051 Low Side OR-ing FET Controller

Check for Samples: LM5051

FEATURES

- **Wide operating input voltage range: -6V to -100V**
- **-100V Transient Capability**
- **Gate drive for external N-Channel MOSFET**
- **MOSFET diagnostic test mode**
- **Fast 50ns response to current reversal**
- **2A peak gate turn-off current**
- **Package: 8-Lead SOIC**

APPLICATIONS

- **Active OR-ing of Redundant (N+1) Power Supplies**

DESCRIPTION

The LM5051 Low Side OR-ing FET Controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This OR-ing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

The LM5051 controller provides gate drive for an external N-Channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5051 can connect power supplies ranging from -6V to -100V and can withstand transients up to -100V.

The LM5051 also provides a FET test diagnostic mode which allows the system controller to test for shorted MOSFETs.

Typical Application Circuits

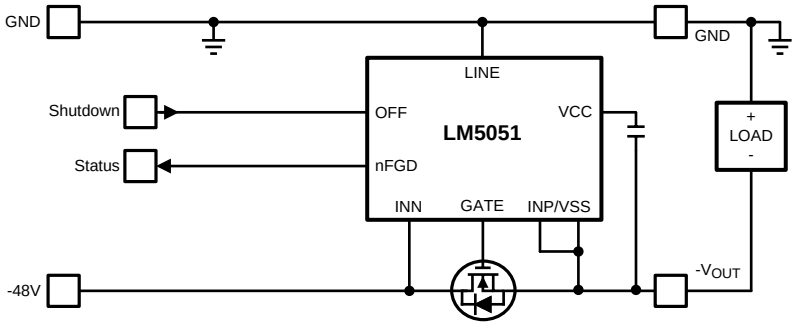


Figure 1. Full Application with MOSFET Diagnostic

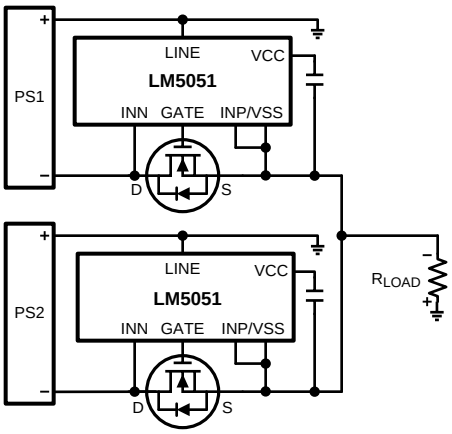
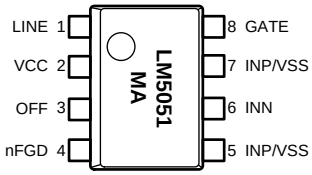


Figure 2. Typical Redundant Supply Configuration

Connection Diagram

Top View



Device Pin 5 (INP) is internally connected to Device Pin 7 (VSS)

Figure 3. LM5051MA
8-Lead SOIC D Package

PIN DESCRIPTIONS

Pin #	Name	Function
1	LINE	Power supply pin to bias the internal 12V zener shunt regulator at the VCC pin through an internal 50 kΩ (typical) series resistor. See the APPLICATION INFORMATION section.
2	VCC	Connection to the internal 12V zener shunt voltage regulator. Bypass this pin with minimum 0.1µF capacitor to the VSS pin. This pin can be biased via an external resistor rather than via the internal resistor from the LINE pin (pin 1). See the APPLICATION INFORMATION section.
3	OFF	FET Test Mode control input. Logic low or open state at the OFF pin will deactivate the FET Test Mode and allow normal operation. A logic high state at the OFF pin will pull the GATE pin low and turn off the external MOSFET. If the body diode forward voltage of the MOSFET (from source to drain) is greater than 260mV the nFGD pin will indicate that the MOSFET is not shorted by pulling to the active low state.
4	nFGD	Open drain output for the FET Test circuit. An active low state on nFGD indicates that the forward voltage (from source to drain) of the external MOSFET is greater than 260 mV typical. The nFGD pin requires an external pull-up resistor to a voltage not higher than VSS + 5.5V.
5	INP/VSS	See device Pin 7.
6	INN	Voltage sense connection to the external MOSFET Drain pin
7	INP/VSS	Internally connected to device Pin 5. Negative supply voltage connection and MOSFET voltage sense connected to the external MOSFET common source connection. All device voltages and currents are referenced to this pin, unless otherwise stated. See the INP/VSS PINS section.

PIN DESCRIPTIONS (continued)

Pin #	Name	Function
8	GATE	Connection to the external MOSFET Gate.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

LINE Pin to INP/VSS	-0.3V to 103V
INN Pin to INP/VSS	-2V to 103V
OFF Pin to INP/VSS	-0.3V to 7V
VCC Pin Sink to INP/VSS	-0.1mA to 20mA
nFGD Pin to INP/VSS (Off)	-0.3V to 7V
Storage Temperature Range	−65°C to 150°C
ESD (HBM) (2)	±2 kV
Peak Reflow Temperature (3)	260°C, 30sec

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including in-operability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For ensured specifications and conditions, see Electrical Characteristics.
(2) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Applicable test standard is JESD-22-A114-C.
(3) For soldering specifications see the LM5051 Product Folder at www.national.com, general information at www.national.com/analog/packaging/, and reflow information at www.national.com/ms/MS/MS-SOLDERING.pdf .

Operating Ratings (1)

Relative to VSS pin

LINE Pin Voltage	36V to 100V
INN Pin Voltage	-1V to 100V
VCC Pin Current	1 mA to 10 mA
OFF Pin Voltage	0.0V to 5.0V
nFGD Voltage (Off)	0.0V to 5.0V
nFGD Sink Current (On)	0 mA to 2 mA
Junction Temperature Range (T_J)	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including in-operability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For ensured specifications and conditions, see Electrical Characteristics.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated all conditions and measurements are referenced to device pin 7 (INP/VSS), and the following conditions apply: V_{LINE}= 48.0V, V_{INN}= -150 mV, V_{OFF}= 0.0V, C_{GATE}= 47 nF, C_{VCC}= 0.1 µF, and T_J= 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LINE Pin						
I_{LINE}	LINE Pin current	V_{LINE} = 48.0V VCC Pin = Open	-	690	**780**	µA
VCC Pin						
VCC	Operating Voltage Range	LINE Pin = Open	**4.50**	-	**V_Z**	V
V_Z	VCC Shunt Zener Voltage	I_{VCC} = 2 mA	**11.9**	13.0	**14.3**	V
		I_{VCC} = 10 mA	**12.5**	13.5	**14.5**	
ΔV_Z	Shunt Zener Regulation	I_{VCC} = 2 mA to 10 mA	-	0.50	**1.11**	V
I_{VCC}	Supply Current	V_{VCC} = V_Z - 100mV	-	1.0	**1.50**	mA
		V_{VCC} = 5.0V	-	0.4	**1.10**	
INN Pin						
I_{INN}	INN Pin Current	V_{INN} = 0.0V	-	3.1	-	µA
		V_{INN} = 90V	-	0.04	-	
GATE						
I_{GATE}	GATE Charge Current	V_{GATE} = 5.5V V_{INN} = -150mV	**0.28**	0.66	**0.95**	mA
	GATE Discharge Current	V_{GATE} = 5.5V V_{INN} = -150 mV to +300 mV t ≤ 10 ms	**2.4**	3.5	-	A
V_{GATE}	GATE Pin High Voltage	V_{LINE} = 48.0V	-	13.0	-	V
		V_{VCC} = 10.25V, LINE = Open	**9.98**	10.2	-	
		V_{VCC} = 5.0V, LINE= Open	**4.70**	4.95	-	
$V_{SD(REV)}$	Reverse Threshold	V_{INN} going negative until Gate Drive Turns ON	**-112.2**	-45	**+11.4**	mV
$\Delta V_{SD(REV)}$	Reverse Threshold Hysteresis	V_{INN} going positive from $V_{SD(REV)}$ Threshold until Gate Drive Turns OFF	-	50	-	mV
$V_{SD(REG)}$	Regulated $V_{INP/VSS}$ to V_{INN} Threshold		**-10.8**	12	**30.8**	mV
$t_{GATE(REV)}$	Gate Capacitance Discharge Time at Forward to Reverse Transition See Figure 6	C_{GATE} = 0 (1)	-	34	**50**	ns
		C_{GATE} = 10 nF (1)	-	60	-	
		C_{GATE} = 47 nF (1)	-	90	**230**	
$t_{GATE(OFF)}$	Gate Capacitance Discharge Time at OFF pin Low to High Transition See Figure 7	C_{GATE} = 47 nF (2)	-	120	-	ns
OFF Pin						
$V_{OFF(IH)}$	OFF Input High Threshold Voltage	V_{INN} = -400 mV V_{OFF} Rising until Gate is Low	**1.28**	1.50	**1.65**	V
$V_{OFF(IL)}$	OFF Input Low Threshold Voltage	V_{INN} = -400 mV V_{OFF} Falling until Gate is High	-	1.48	-	
ΔV_{OFF}	OFF Threshold Voltage Hysteresis	$V_{OFF(IH)}$ - $V_{OFF(IL)}$	-	20	-	mV
$I_{OFF(IH)}$	OFF Pin Internal Pull-down	V_{OFF} = 5.0V	-	4.6	**6.00**	µA
$I_{OFF(IL)}$		V_{OFF} = 0.0V	-	-0.03	-	µA

(1) Time from V_{INN} voltage transition from -200 mV to +500 mV until Gate pin voltage falls to ≤ 1.00V. See Figure 6
(2) Time from V_{OFF} voltage transition from 0.0V to 5.0V until GATE pin voltage falls to ≤ 1.0V. See Figure 7

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated all conditions and measurements are referenced to device pin 7 (INP/VSS), and the following conditions apply: V_{LINE}= 48.0V, V_{INN}= -150 mV, V_{OFF}= 0.0V, C_{GATE}= 47 nF, C_{VCC}= 0.1 µF, and T_J= 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET Test Comparator						
$V_{SD(TST)}$	FET Test Threshold Voltage V_{INP} - V_{INN}	V_{OFF} = 5.0V $V_{INN/VSS}$ going negative from V_{INP} until nFGD pin goes Hi-Z	**-360**	-260	**-183**	mV
$\Delta V_{SD(TST)}$	FET Test Threshold Voltage Hysteresis	V_{OFF} = 5.0V V_{INN} going positve from $V_{SDT(ST)}$ until nFGD pin goes Lo-Z	-	6.5	-	mV
nFGD Pin						
$nFGD_{VOL}$	nFGD Output Low Voltage nFGD Output = On	V_{OFF} = 5V I_{nFGD} = 1mA Sinking	-	285	**450**	mV
$nFGD_{IOL}$	nFGD Output Leakage Current nFGD Output = Off	V_{OFF} = 0V V_{nFGD} = 5.0V	-	0.01	**0.7**	µA

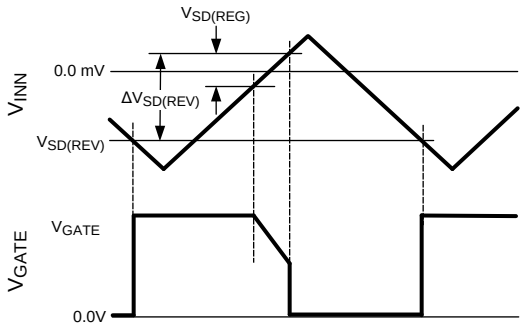


Figure 4. $V_{SD(REV)}$ Threshold Definitions

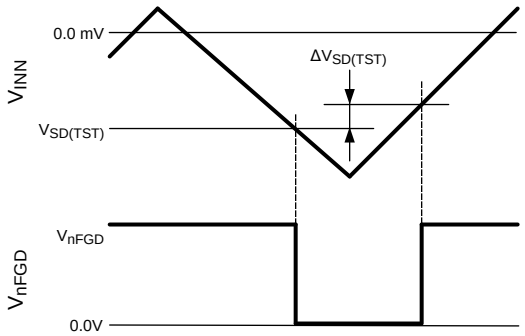


Figure 5. $V_{SD(TST)}$ Threshold Definitions

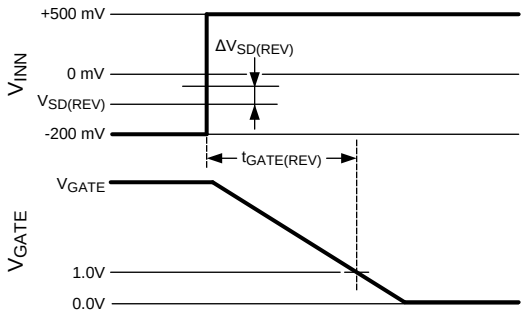


Figure 6. Gate Off Timing for $V_{SD(REV)}$ Transition

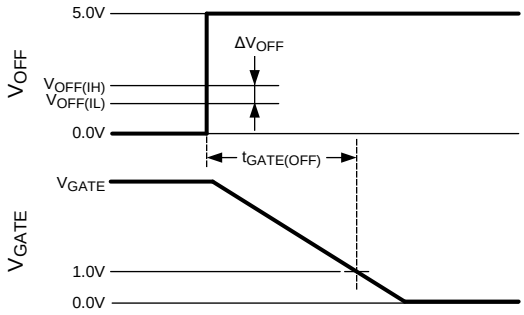


Figure 7. Gate Off Timing for V_{OFF} Transition

Typical Performance Characteristics

Unless otherwise stated: All conditions and measurements are referenced to device pin 7 (INP/VSS), V_{LINE} = 48V, V_{OFF} = 0.0V, V_{INN} = -150 mV, C_{VCC} = 0.1 µF, C_{GATE} = 47 nF, and T_J = 25°C

Gate Charge Time, C_{GATE} = 47 nF

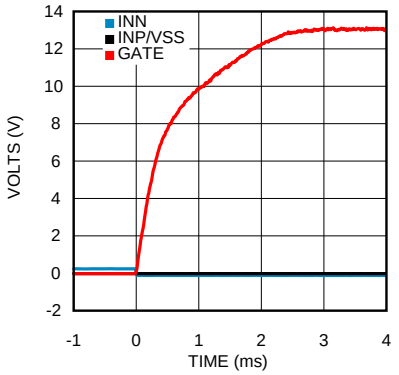


Figure 8.

GATE Discharge Time, $t_{GATE(REV)}$, C_{GATE} = 47 nF

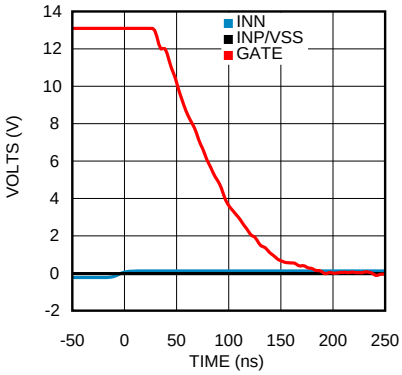


Figure 9.

I_{GATE} Discharge Current vs Temperature, V_{GATE} = 5.5V

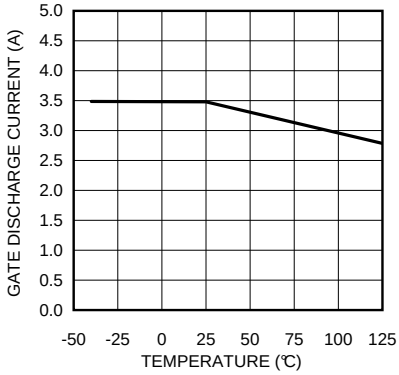


Figure 10.

Gate Discharge Time vs Temperature

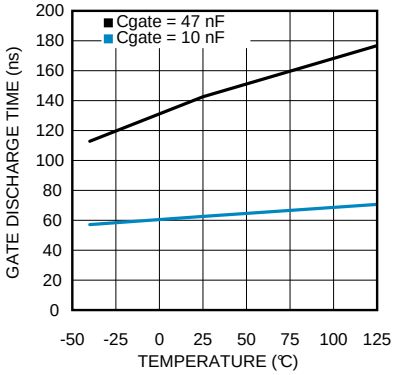


Figure 11.

Gate Discharge Time vs C_{GATE}

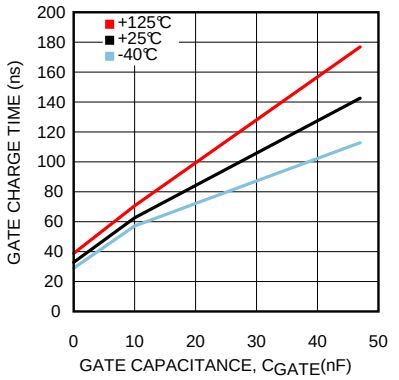


Figure 12.

I_{GATE} Charge Current vs Temperature, V_{GATE} = 5.5V

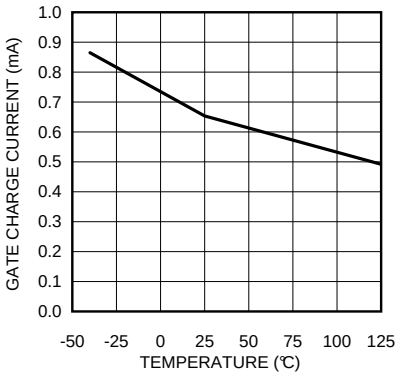


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise stated: All conditions and measurements are referenced to device pin 7 (INP/VSS), V_{LINE} = 48V, V_{OFF} = 0.0V, V_{INN} = -150 mV, C_{VCC} = 0.1 µF, C_{GATE} = 47 nF, and T_J = 25°C

Gate Charge Time vs Temperature, V_{GATE}= 0.0V to 5.5V

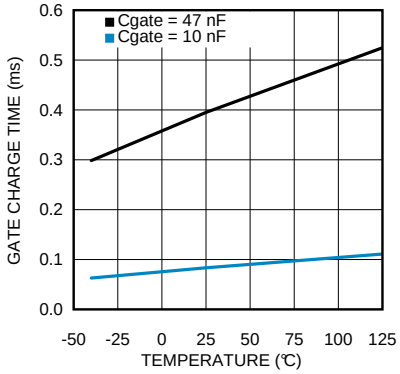


Figure 14.

$V_{SD(TST)}$ Thresholds vs Temperature

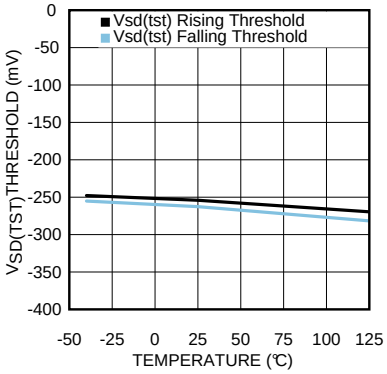


Figure 15.

OFF Thresholds vs Temperature

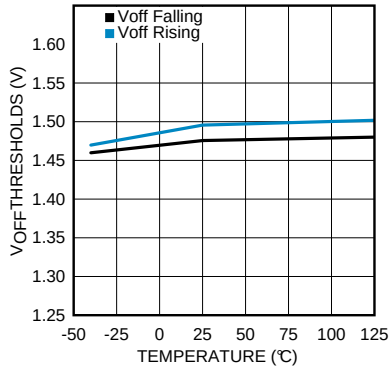


Figure 16.

V_Z vs Temperature, V_{INN}= –100 mV

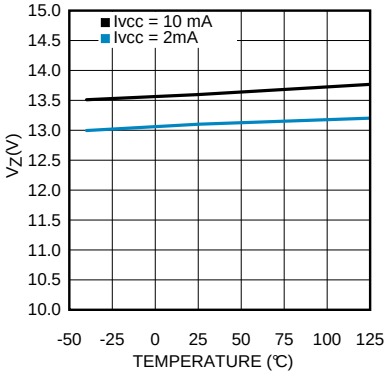


Figure 17.

V_Z vs V_{LINE}, V_{INN}= –100 mV

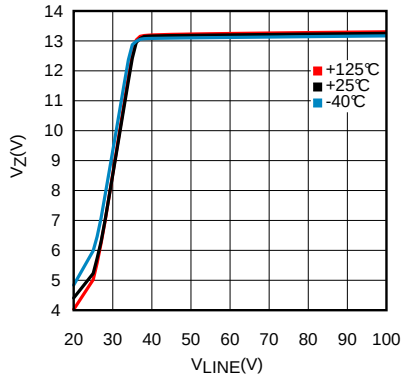


Figure 18.

I_{LINE} vs V_{LINE}

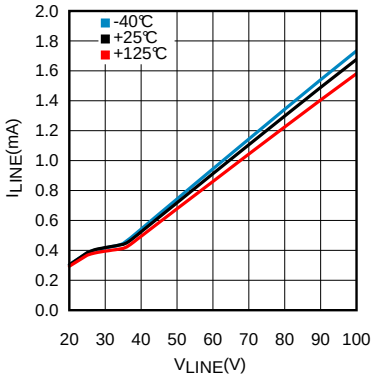


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise stated: All conditions and measurements are referenced to device pin 7 (INP/VSS), V_{LINE} = 48V, V_{OFF} = 0.0V, V_{INN} = -150 mV, C_{VCC} = 0.1 µF, C_{GATE} = 47 nF, and T_J = 25°C

I_{GATE} Charge Current vs V_{LINE} , V_{GATE} = 0.0V

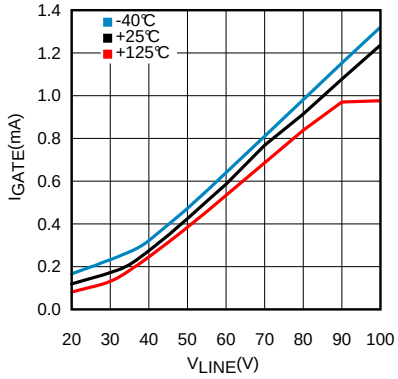


Figure 20.

V_{GATE} vs V_{LINE}

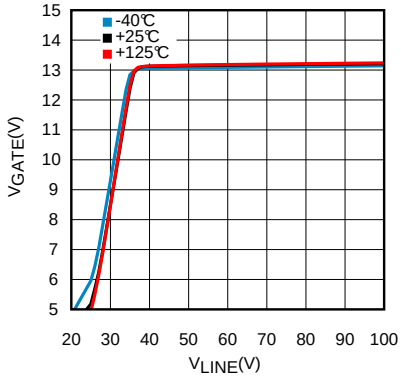


Figure 21.

$nFGD_{VOL}$ vs Temperature

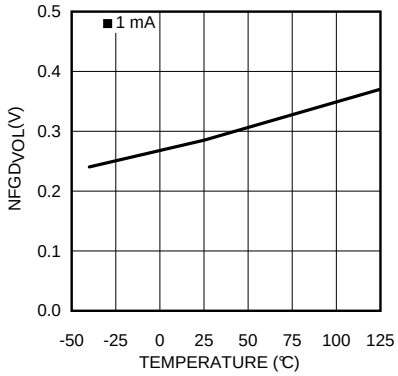


Figure 22.

$V_{SD(REV)}$ Thresholds vs Temperature

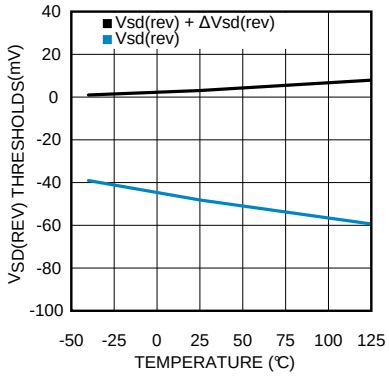


Figure 23.

I_{INN} vs V_{INN}

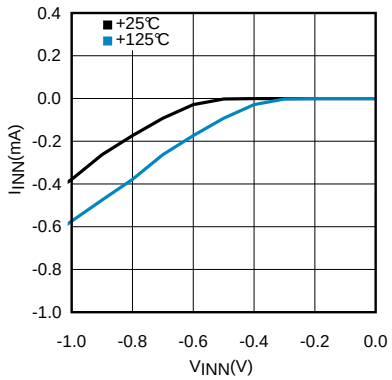


Figure 24.

V_{GATE} vs V_{OFF} , V_{INN} = -100mV

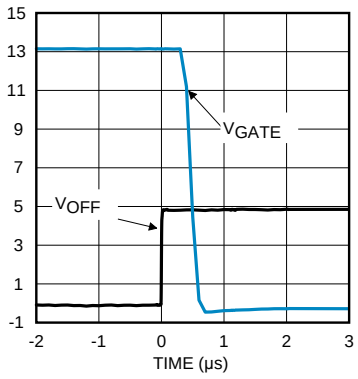
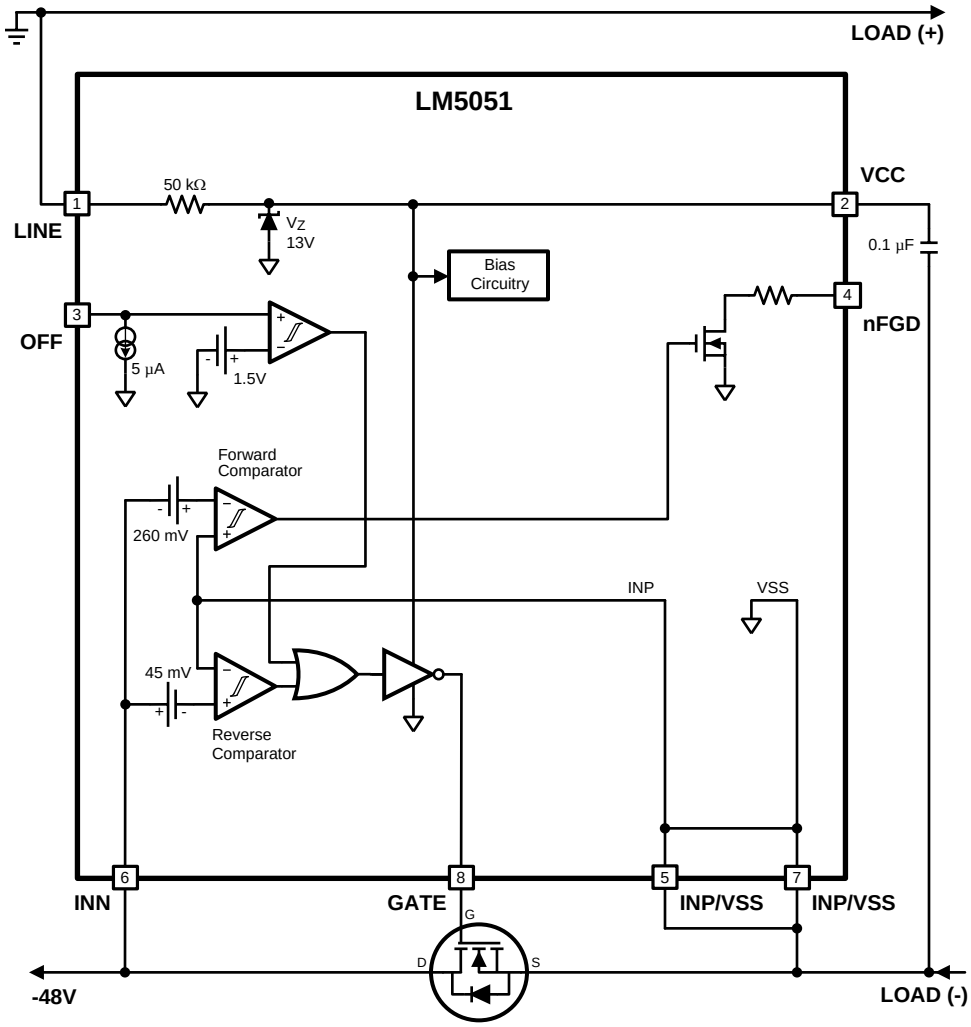


Figure 25.

BLOCK DIAGRAM



APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage, and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.

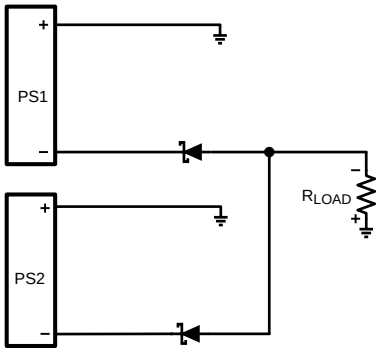


Figure 26. Traditional OR-ing with Diodes

The LM5051 is a negative voltage (i.e. low-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the LM5051 at the IN and OUT pins, while the GATE pin drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.

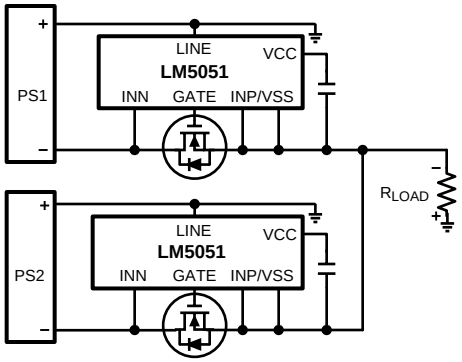


Figure 27. OR-ing with MOSFETs

INP/VSS PINS

The INP input is internally connected to the both device pin 5 and 7. Typical applications will use device pin 7 only, with a single common connection to the source connection of the N-Channel MOSFET array.

If pins 5 and 7 are both used, it is recommended that the two pins be externally connected together at the package, with a single common connection routed to the source connection of the N-Channel MOSFET array. Current should not be allowed flow through the internal connection between pin 5 and pin 7.

INN and GATE PINS

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. The resulting voltage across the body diode will be detected across the LM5051 INN and INP/VSS pins which then begins charging the MOSFET gate through a 0.66 mA (typical) current source.

The LM5051 is designed to regulate the MOSFET gate to source voltage if the voltage across the MOSFET source and drain pins falls below the $V_{SD(REG)}$ voltage of 20 mV (typical). If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 12 mV (typical), the GATE pin voltage will be decreased until the voltage across the MOSFET is regulated at 12 mV (typical). If the drain to source voltage is greater than$V_{SD(REG)}$ voltage the gate voltage will increase.

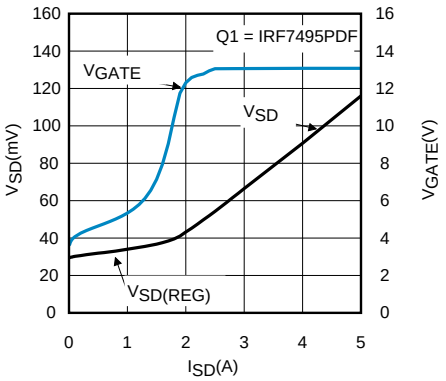


Figure 28. V_{SD} and V_{GATE} vs I_{LOAD} with IRF7495PDF

When the power supply voltages are within a few milli-volts of each other, this regulation method ensures that the load current transitions between them without any abrupt on and off oscillations. The current flowing through the MOSFET in each OR-ing circuit depends on the $R_{DS(ON)}$ of the MOSFETs, how close the power supply voltages are set, and the load regulation of the supplies.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the LM5051 INN pin is 5 mV (typical) more positive than INP/VSS pin ($V_{SD(REV)}$ + $\Delta V_{SD(REV)}$) the LM5051 will quickly discharge the MOSFET gate through a strong GATE pin to INP/VSS pin discharge path. A reverse current though the MOSFET is required to turn the gate drive off. If a single operating supply is removed from the OR-ing array, the gate drive will not be discharged since there is no reverse current through the MOSFET to trip the reverse comparator.

If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The LM5051 responds to a voltage reversal condition typically within 34 ns. The actual time required to turn off the MOSFET will depend on the charge held by gate capacitance of the MOSFET being used. A MOSFET with 47 nF of effective gate capacitance can be turned off in typically 90 ns. This fast turn-off time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

OFF PIN

The OFF pin is used to disable the active OR-ing control circuitry, and to discharge the MOSFET Gate. The OFF pin has an internal pull-down (4.6 µA typical) which will, by default, keep the active OR-ing control circuitry enabled. If the OFF pin function is not needed, this pin can be left open or connected to the INP/VSS pin. Pulling the OFF pin above the $V_{OFF(IH)}$ threshold of 1.50V (typical) will disable the active OR-ing control circuitry and discharge the MOSFET Gate. The V_{OFF} threshold has a typical hysteresis of 20mV. It is recommended that the OFF pin be pulled cleanly, and promptly, through the $V_{OFF(IH)}$ threshold region to prevent any aberrant behavior. The OFF pin must not be pulled higher than 5.5V above the INP/VSS pin.

nFGD PIN

The nFGD pin is an open Drain output pin and is controlled by status of the Forward comparator. When the voltage on INN pin is more negative than the $V_{SD(TST)}$ threshold voltage (285 mV typical) the nFGD pin will conduct current to the INP/VSS pin. During normal Active OR-ing, when the MOSFET is ON, the INN pin voltage should be less than approximately -100mV and the nFGD pin will be logic high. When the MOSFET is OFF and current is flowing through the body diode of the MOSFET, the INN pin voltage will be approximately -600 mV and the nFGD pin will be logic low.

Several factors can prevent the nFGD pin from indicating that the external MOSFET is operating normally. If the LM5051 is used to connect parallel, redundant power supplies, one of the connected supplies may hold the INP/VSS pin voltage close enough to the LM5051 INN pin voltage that the $V_{SD(TST)}$ threshold is not exceeded. Additionally, operating with a high output capacitance value and low output load current may require a significant amount of time before the output load capacitance is discharged to the point where the $V_{SD(TST)}$ threshold is crossed and the nFGD pin switches.

The status of the nFGD pin does not depend on the status of the OFF pin. The status of the nFGD pin depends only on the voltage at the INN pin relative to the INP/VSS pin being above, or below, the $V_{SD(TST)}$ threshold voltage.

The nFGD output pin requires pull-up to an external voltage source, and must not be pulled higher than 5.5V above the INP/VSS pin. It is recommended that the nFGD pin is not required to sink more than 2mA.

VCC PIN

The VCC pin is connected to the cathode of the internal shunt (zener) voltage regulator. The anode of the shunt regulator is connected to the INP/VSS pin. The VCC pin provides bias for internal circuitry, as well as gate drive to the external MOSFET. The VCC pin should always be bypassed with a 0.1 µF ceramic capacitor to the INP/VSS pin.

Typically, the VCC pin is biased from the LINE pin, through the internal 50 kΩ series resistor, when the available V_{LINE} voltage is not less than the 36V minimum operating voltage.

If the available LINE voltage is less than less than the 36V minimum operating voltage the VCC pin can be biased through the use of an external resistor to an appropriate bias supply that is referenced to the INP/VSS pin.

A minimum VCC pin bias current of 1 mA is recommended, with a recommended 10 mA maximum.

A design example for calculating the external resistor where the VCC pin will be biased from an 18V to 36V supply (relative to the INP/VSS pin):

$$R_{BIAS} = (V_{BIAS(MIN)} - V_Z) / I_{BIAS(MIN)} \quad (1)$$

$$R_{BIAS} = (18V - 13V) / 1\ mA \quad (2)$$

$$R_{BIAS} = 5.0\ k\Omega \quad (3)$$

Next, using the calculated R_{BIAS} resistor value, verify that the VCC pin current will be no more than 10mA at the maximum V_{BIAS} voltage:

$$ICC = (V_{BIAS(MAX)} - 13V) / R_{BIAS} \quad (4)$$

$$ICC = (36V - 13V) / 5.0\ k\Omega \quad (5)$$

$$ICC = 4.6\ mA \quad (6)$$

Since the calculated 4.6 mA is less than the 10 mA maximum, the 5 kΩ value for R_{BIAS} is acceptable.

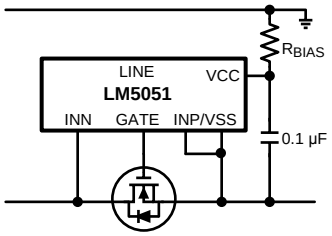


Figure 29. Using an External Resistor to Bias the VCC Pin

Alternately, an external bias supply can be connected directly to the VCC pin, as long as the applied voltage is below the minimum V_Z breakdown voltage (11.9V) and above the minimum VCC operating voltage (4.50V). In this case, it is important to pay close attention to the $_{VGS}$ rating of the external MOSFET as the gate drive voltage will be affected by the lower voltage on the VCC pin.

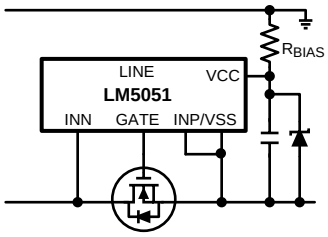


Figure 30. Using an External Zener to Bias the VCC Pin

In the case where the OFF pin is high (i.e. OR-ing is disabled, and the Gate is discharged) and the voltage at the INN pin is more negative than the $V_{SD(REV)}$ threshold voltage the internal current increases, and the voltage on the VCC pin may drop.. Since the LM5051 is in the OFF state, this voltage drop does not affect any operation. However, when the OFF pin is taken low to resume normal operation, the initial Gate charge time may be extended slightly if the capacitor on the VCC pin has not had adequate time to fully recharge through either the external R_{BIAS} resistor, or through the internal 50 kΩ resistor.

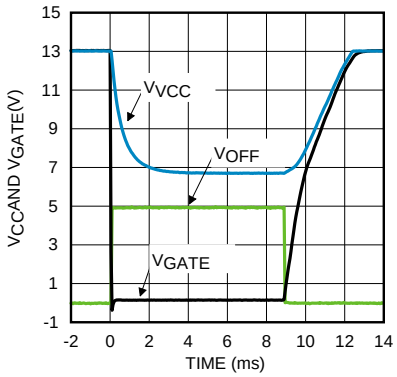


Figure 31. V_{CC} and V_{GATE} vs V_{OFF}, V_{INN} = –100 mV

HIGH SIDE OR-ing

Because the INP and VSS functions are internally connected, the LM5051 cannot be configured as a High-Side (i.e. Positive) OR-ing controller. Please refer to the LM5050-1 and LM5050-2 High-Side OR-ing controllers.

MOSFET FAILURE

Typically, the INN pin maximum negative voltage will be defined by the body diode of the external MOSFET. In the even that the external MOSFET has a catastrophic failure that results in an open body diode, the voltage between the INP/VSS pin and the INN pin may cause current through the LM5051 substrate diode at the INN pin. The voltage at the INN pin must be limited to a safe level (-1V) to prevent damage to the LM5051. The voltage on the INN pin can be limited with the use of a Schottky diode and a current limiting resistor. Note that the power dissipation of the current limiting resistor should allow for any anticipated worst case condition. See Figure 32.

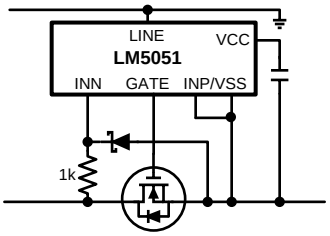


Figure 32. Protecting the INN Pin

SHORT CIRCUIT FAILURE OF AN INPUT SUPPLY

An abrupt zero ohm short circuit across the input supply will cause the highest possible reverse current to flow while the internal LM5051 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (7)$$

The internal Reverse Comparator will react, and will start the process of discharging the Gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (8)$$

When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit.

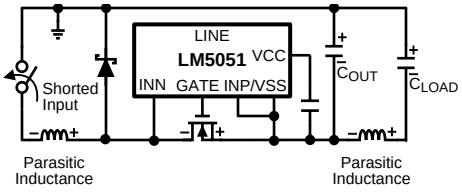


Figure 33. Input Supply Fault Transients

MOSFET SELECTION

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (i.e. body diode), the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source On resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must be exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$:

$$\text{Gate Charge Time} = Q_g / I_{GATE(ON)} \quad (9)$$

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.

The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.

The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the LM5051 gate drive capabilities. Logic level MOSFETs are recommended, but sub-Logic level MOSFETs can also be used.

The dominate MOSFET loss for the LM5051 active OR-ing controller is conduction loss due to source-to-drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

1) Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the LM5051 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turn-off condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.

2) Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (i.e. reverse) without activating the LM5051 Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.

3) Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.

Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation.

As a guideline, it is suggest that $R_{DS(ON)}$ be selected to provide at least 20 mV, and no more than 100 mV, at the nominal load current.

$$(20\ mV / I_D) \le R_{DS(ON)} \le (100mV / I_D) \quad (10)$$

The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET in order to ensure that the junction temperature (T_J) is reasonably well controlled, since the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

$$P_{DISS} = I_D^2 \times (R_{DS(ON)}) \quad (11)$$

Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10A, and an $R_{DS(ON)}$ of 10 mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating (θ_{JA}) would need to be:

$$\theta_{JA} \le (T_{J(MAX)} - T_{A(MAX)})/(I_D^2 \times R_{DS(ON)}) \quad (12)$$

$$\theta_{JA} \le (100°C - 35°C)/(10A \times 10A \times 0.01\Omega) \quad (13)$$

$$\theta_{JA} \le 65°C/W \quad (14)$$

TYPICAL APPLICATIONS

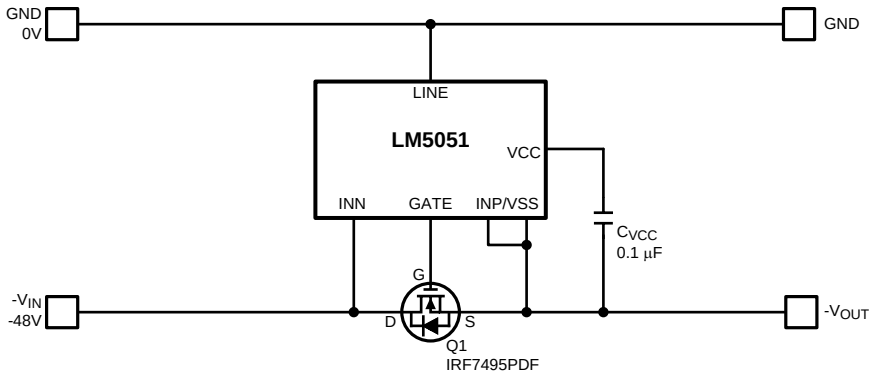
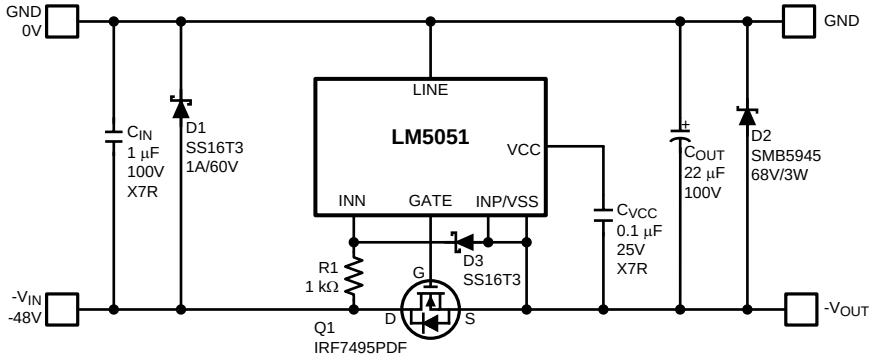


Figure 34. Basic Application



Typical –48V Application with Input and Output Transient Protection and Open MOSFET Protection

Figure 35. Typical –48V Application

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5051MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L5051 MA	Samples
LM5051MAE/NOPB	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L5051 MA	Samples
LM5051MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L5051 MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

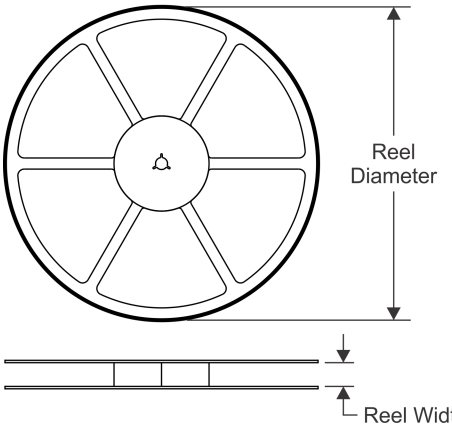
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

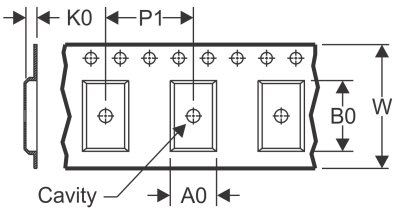
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

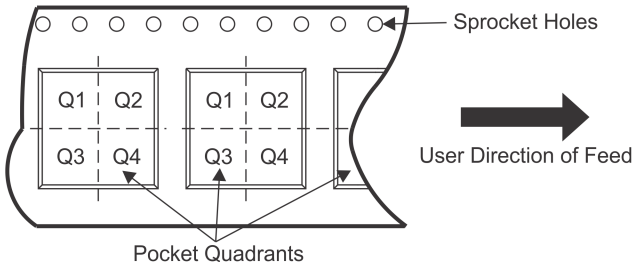


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

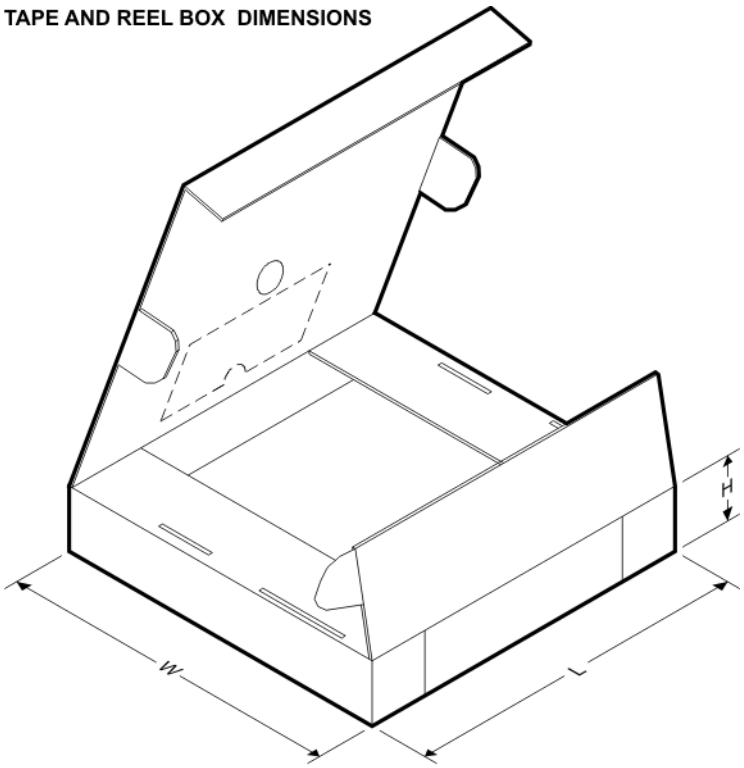
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

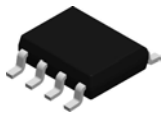
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5051MAE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5051MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5051MAE/NOPB	SOIC	D	8	250	210.0	185.0	35.0
LM5051MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

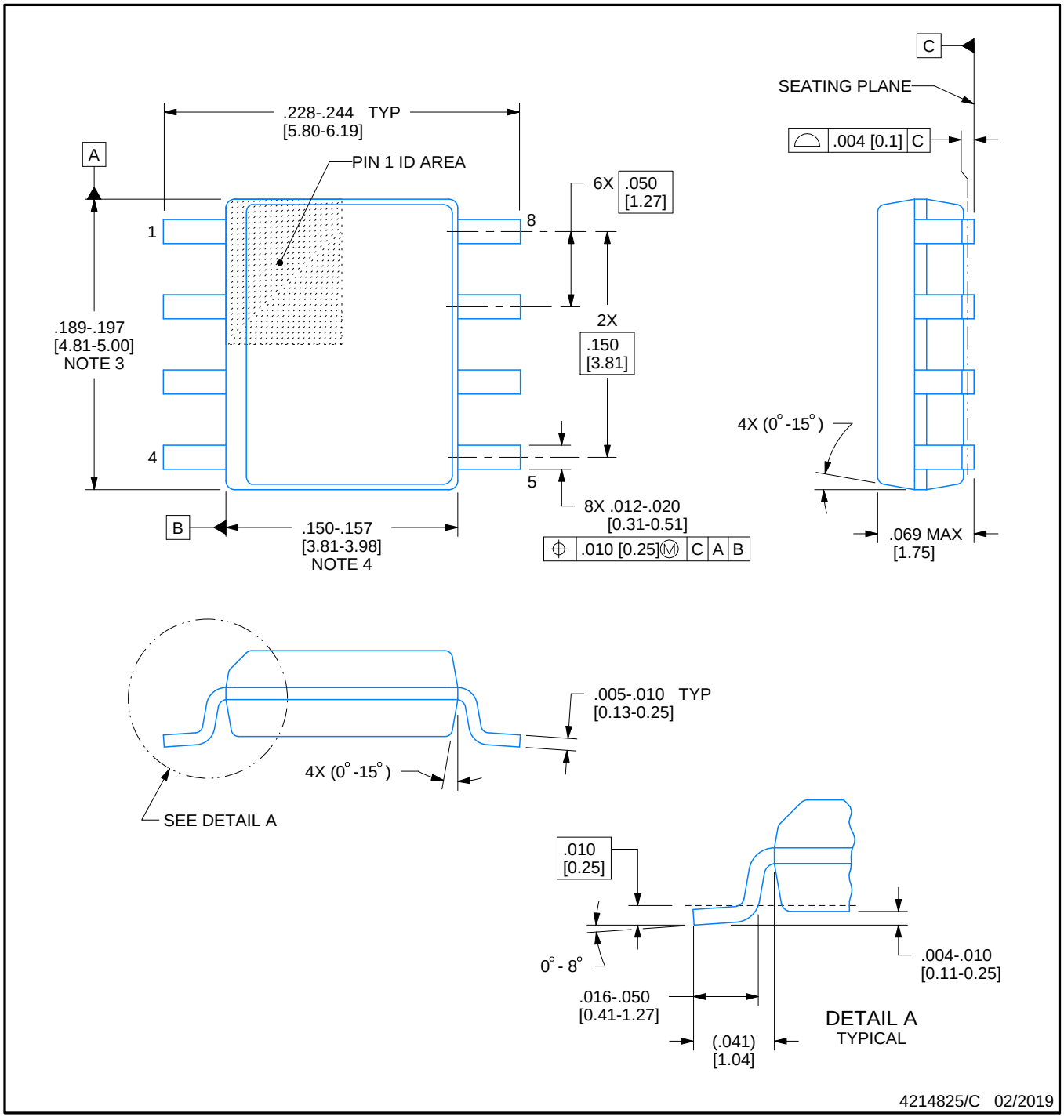


PACKAGE OUTLINE

D0008A

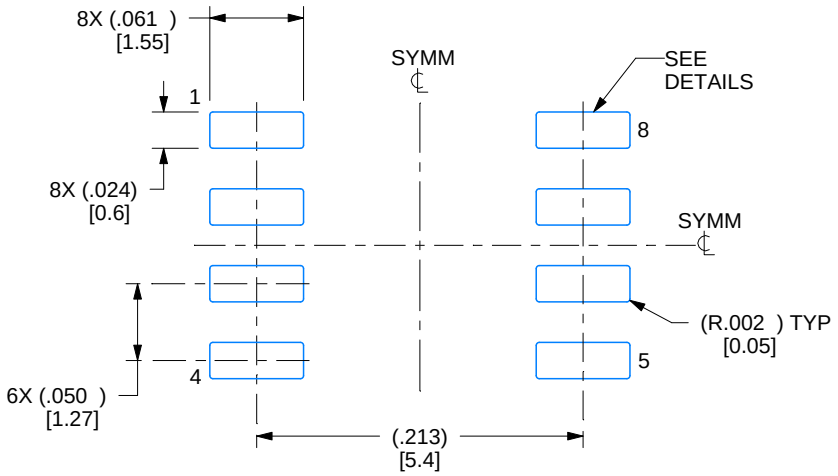
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

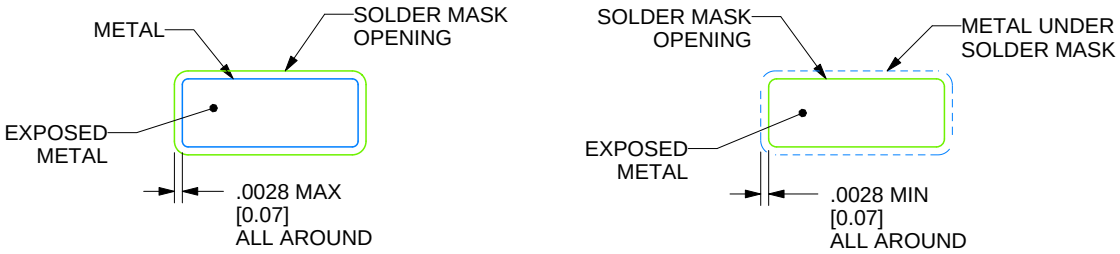


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

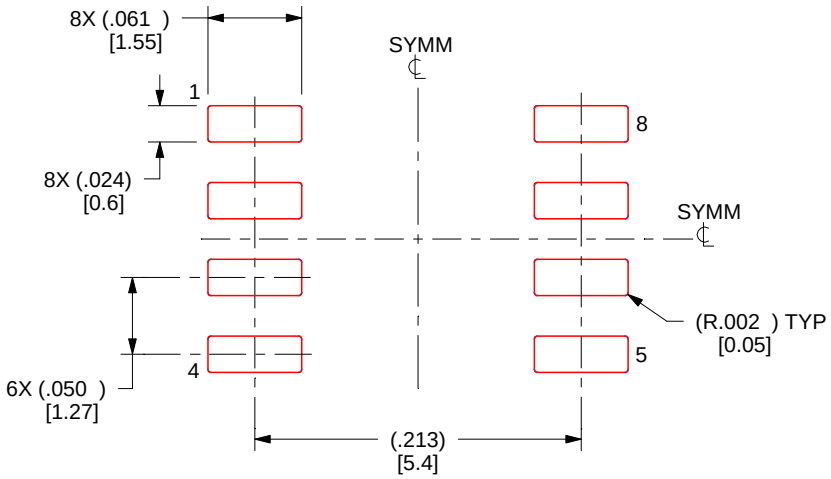
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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