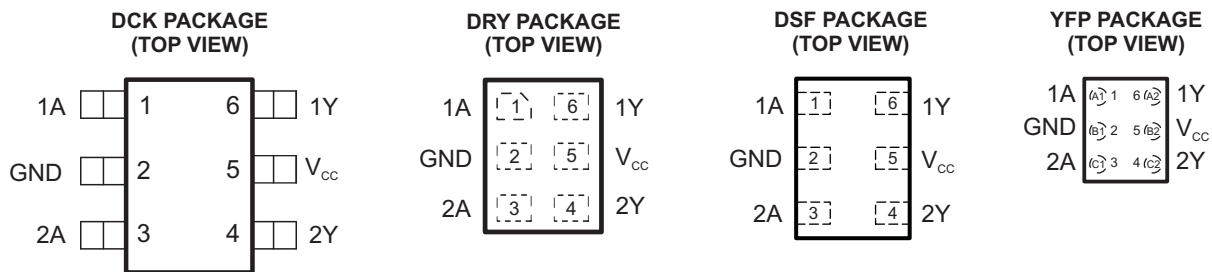# LOW-POWER DUAL SCHMITT-TRIGGER INVERTER

Check for Samples: **SN74AUP2G14**

FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 µA Maximum)**
- **Low Dynamic-Power Consumption (C_{pd} = 4.3 pF Typical at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typical)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**

- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 4.3 ns Maximum at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

DCK PACKAGE (TOP VIEW) | DRY PACKAGE (TOP VIEW) | DSF PACKAGE (TOP VIEW) | YFP PACKAGE (TOP VIEW)

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).

(A)Single, dual, and triple gates
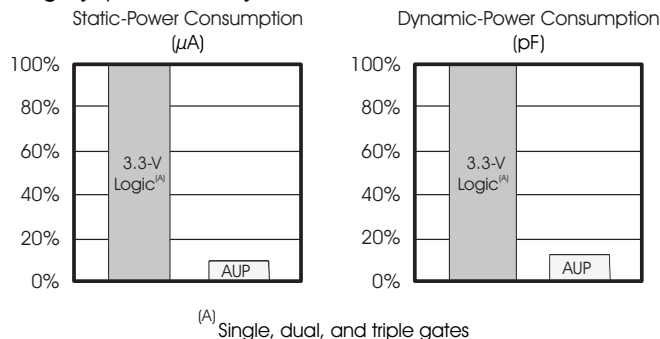
Figure 1. AUP – The Lowest-Power Family
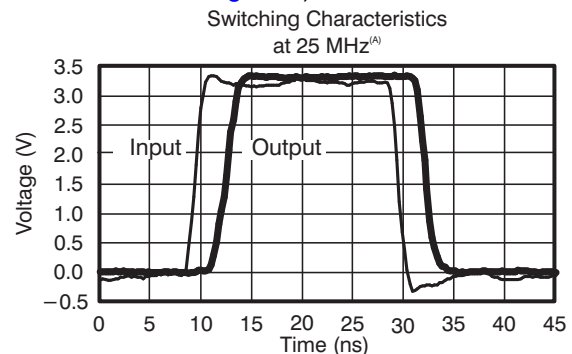
(A) SN74AUP2Gxx data at C_L = 15 pF.

Figure 2. Excellent Signal Integrity

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
NanoStar is a trademark of Texas Instruments.

The SN74AUP2G14 contains two inverters and performs the Boolean function $Y = \overline{A}$. The device functions as two independent inverters, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION [1] [2] [3]

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING[4]
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G14YFPR	_ _ _ H F _
	QFN – DSF	Reel of 5000	SN74AUP2G14DSFR	H6
			SN74AUP2G14DSF2[3]	
	uQFN – DRY	Reel of 5000	SN74AUP2G14DRYR	H6
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP2G14DCKR	H6_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) Pin 1 orientation at quadrant 3 in Tape.
(4) DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE
(Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM (POSITIVE LOGIC)
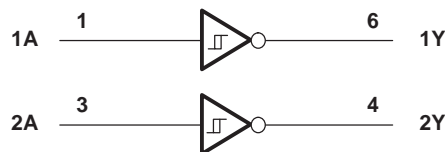
ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[2]		−0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	4.6	V
V_O	Output voltage range in the high or low state[2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance[3]	DCK package		252	°C/W
		DSF package		300	
		DRY package		234	
		YFP package		132	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[(1)]

				MIN	**MAX**	**UNIT**
V_{CC}	Supply voltage			0.8	3.6	V
V_I	Input voltage			0	3.6	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V			−20	µA
		V_{CC} = 1.1 V			−1.1	mA
		V_{CC} = 1.4 V			−1.7	
		V_{CC} = 1.65			−1.9	
		V_{CC} = 2.3 V			−3.1	
		V_{CC} = 3 V			−4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V			20	µA
		V_{CC} = 1.1 V			1.1	mA
		V_{CC} = 1.4 V			1.7	
		V_{CC} = 1.65 V			1.9	
		V_{CC} = 2.3 V			3.1	
		V_{CC} = 3 V			4	
T_A	Operating free-air temperature			−40	85	°C

(1)   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			$T_A = -40°C$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage			0.8 V	0.3		0.6	0.3	0.6	V
			1.1 V	0.53		0.9	0.53	0.9	
			1.4 V	0.74		1.11	0.74	1.11	
			1.65 V	0.91		1.29	0.91	1.29	
			2.3 V	1.37		1.77	1.37	1.77	
			3 V	1.88		2.29	1.88	2.29	
V_{T-} Negative-going input threshold voltage			0.8 V	0.1		0.6	0.1	0.6	V
			1.1 V	0.26		0.65	0.26	0.65	
			1.4 V	0.39		0.75	0.39	0.75	
			1.65 V	0.47		0.84	0.47	0.84	
			2.3 V	0.69		1.04	0.69	1.04	
			3 V	0.88		1.24	0.88	1.24	
ΔV_T Hysteresis $(V_{T+} - V_{T-})$			0.8 V	0.07		0.5	0.07	0.5	V
			1.1 V	0.08		0.46	0.08	0.46	
			1.4 V	0.18		0.56	0.18	0.56	
			1.65 V	0.27		0.66	0.27	0.66	
			2.3 V	0.53		0.92	0.53	0.92	
			3 V	0.79		1.31	0.79	1.31	
V_{OH}		$I_{OH} = -20$ μA	0.8 V to 3.6 V	$V_{CC} - 0.1$			$V_{CC} - 0.1$		V
		$I_{OH} = -1.1$ mA	1.1 V	$0.75 \times V_{CC}$			$0.7 \times V_{CC}$		
		$I_{OH} = -1.7$ mA	1.4 V	1.11			1.03		
		$I_{OH} = -1.9$ mA	1.65 V	1.32			1.3		
		$I_{OH} = -2.3$ mA	2.3 V	2.05			1.97		
		$I_{OH} = -3.1$ mA		1.9			1.85		
		$I_{OH} = -2.7$ mA	3 V	2.72			2.67		
		$I_{OH} = -4$ mA		2.6			2.55		
V_{OL}		$I_{OL} = 20$ μA	0.8 V to 3.6 V			0.1		0.1	V
		$I_{OL} = 1.1$ mA	1.1 V			$0.3 \times V_{CC}$		$0.3 \times V_{CC}$	
		$I_{OL} = 1.7$ mA	1.4 V			0.31		0.37	
		$I_{OL} = 1.9$ mA	1.65 V			0.31		0.35	
		$I_{OL} = 2.3$ mA	2.3 V			0.31		0.33	
		$I_{OL} = 3.1$ mA				0.44		0.45	
		$I_{OL} = 2.7$ mA	3 V			0.31		0.33	
		$I_{OL} = 4$ mA				0.44		0.45	
I_I	A or B input	$V_I = $ GND to 3.6 V	0 V to 3.6 V			0.1		0.5	μA
I_{off}		V_I or $V_O = 0$ V to 3.6 V	0 V			0.2		0.6	μA
ΔI_{off}		V_I or $V_O = 0$ V to 3.6 V	0 V to 0.2 V			0.2		0.6	μA
I_{CC}		$V_I = $ GND or (V_{CC} to 3.6 V), $I_O = 0$	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}		$V_I = V_{CC} - 0.6$ V [(1)], $I_O = 0$	3.3 V			40		50	μA
C_i		$V_I = V_{CC}$ or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		$V_O = $ GND	0 V		3				pF

(1)   One input at $V_{CC} - 0.6$ V, other input at V_{CC} or GND.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		18				ns
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	
			1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
			1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		18.4				ns
			1.2 V ± 0.1 V	4.6	7.9	13.4	1.3	16.7	
			1.5 V ± 0.1 V	4	6	9.6	2.2	11.8	
			1.8 V ± 0.15 V	3.6	5	7.9	2.4	9.5	
			2.5 V ± 0.2 V	3.2	4	5.5	2.3	6.8	
			3.3 V ± 0.3 V	2.9	3.5	4.6	2.1	5.6	

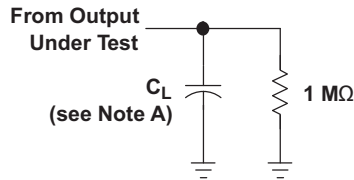## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		24				ns
			1.2 V ± 0.1 V	3.6	9.9	16.3	3.1	19.9	
			1.5 V ± 0.1 V	2.3	7.2	11.1	1.8	13.2	
			1.8 V ± 0.15 V	1.6	5.8	8.7	1.1	10.6	
			2.5 V ± 0.2 V	1	4.3	5.9	0.5	7.3	
			3.3 V ± 0.3 V	1	3.4	4.8	0.5	5.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		32.8				ns
			1.2 V ± 0.1 V	4.9	13.1	20.9	4.4	25.5	
			1.5 V ± 0.1 V	3.4	9.5	14.2	2.9	16.9	
			1.8 V ± 0.15 V	2.5	7.7	11	2	13.5	
			2.5 V ± 0.2 V	1.8	5.7	7.6	1.3	9.4	
			3.3 V ± 0.3 V	1.5	4.7	6.2	1	7.5	

Product Folder Link(s): *SN74AUP2G14*

OPERATING CHARACTERISTICS

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

From Output Under Test

C_L (see Note A)

1 MΩ

LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{CC}/2
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
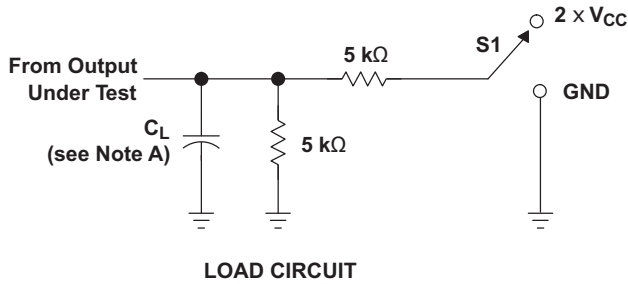**PULSE DURATION**

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, for propagation delays t_r/t_f = 3 ns, for setup and hold times and pulse width t_r/t_f = 1.2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

F. All parameters and waveforms are not applicable to all devices.
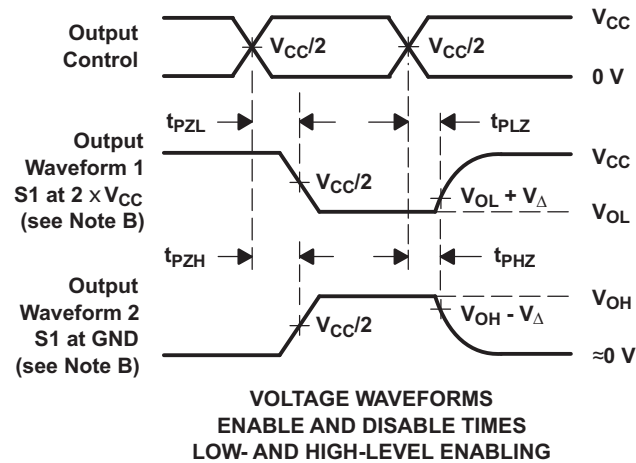
Figure 3. Load Circuit and Voltage Waveforms

Product Folder Link(s): *SN74AUP2G14*

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)

TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PLH} and t_{PHL} are the same as t_{pd}.

G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP2G14DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H65, H6F)	Samples
SN74AUP2G14DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6	Samples
SN74AUP2G14DSF2	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6	Samples
SN74AUP2G14DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H6	Samples
SN74AUP2G14YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HFN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G14DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP2G14DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP2G14DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G14DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP2G14DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G14YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G14DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G14DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G14DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G14DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G14DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G14YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

B ← 1.05 / 0.95 → A

PIN 1 INDEX AREA

1.5 / 1.4

0.6 MAX

C

SEATING PLANE

0.05 / 0.00

⌒ 0.08 C

3X 0.6

SYMM ₵

(0.05) TYP

3

4X 0.5

4

2X 1

SYMM ₵

1

6

0.4 / 0.3

6X 0.25 / 0.15

⊕ 0.1 Ⓜ C A B
0.05 Ⓜ C

PIN 1 ID (OPTIONAL)

5X 0.35 / 0.25

(0.127) TYP

4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM
℄

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM
℄

4X (0.5)

3

4

(R0.05) TYP

(0.6)

LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

0.05 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.05 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED
(PREFERRED)**

SOLDER MASK DETAILS

4222894/A   01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)

SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A   01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCK (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE

2,15
1,85

6   5   4

1,40
1,10

2,40
1,80

Pin 1
Index Area

1   2   3

0,65

6X 0,30
     0,15

1,30

⊕ 0,10 Ⓜ

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
0,80

0,10

Seating Plane

0,10
0,00

4093553−4/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
          D.   Falls within JEDEC MO−203 variation AB.

DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

4x0,65

4x0,65

2x1,30

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

TEXAS INSTRUMENTS
www.ti.com

BALL A1
CORNER

B E A

D

0.5 MAX

0.19
0.13

BALL TYP

C

SEATING PLANE

⌒ 0.05 C

0.4
TYP

SYMM
₵

0.8
TYP

0.4 TYP

C

B

A

SYMM
₵

1 2

6X ⌀ 0.25
0.21

⊕ 0.015Ⓜ C A B

D: Max = 1.19 mm, Min = 1.13 mm

E: Max = 0.79 mm, Min = 0.73 mm

4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

6X ($\emptyset$ 0.23)

(0.4) TYP

(0.4) TYP

1   2

A

B   SYMM
           $\mathbb{C}$

C

SYMM
$\mathbb{C}$

LAND PATTERN EXAMPLE
SCALE:50X

($\emptyset$ 0.23)
METAL

0.05 MAX

SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

METAL UNDER
SOLDER MASK

($\emptyset$ 0.23)
SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223410/A   11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

TEXAS
INSTRUMENTS
www.ti.com
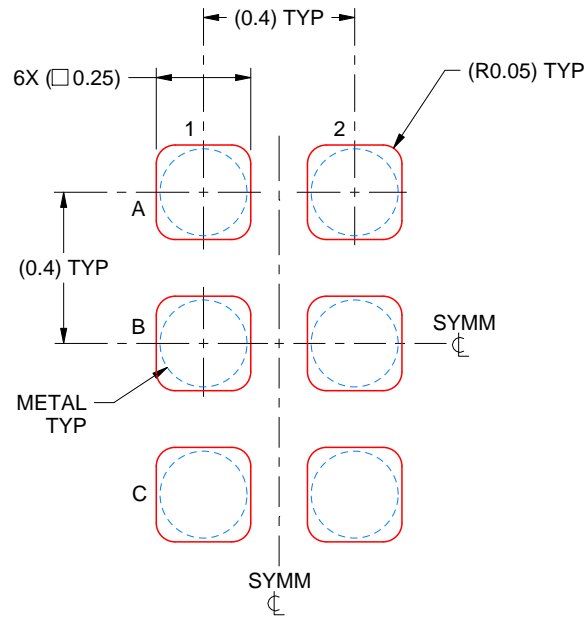
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A   11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

B | 1.05 / 0.95 | A

PIN 1 INDEX AREA

1.05 / 0.95

0.4 MAX

C

SEATING PLANE

0.05 | C

(0.11) TYP

0.05 / 0.00

SYMM

3

4

SYMM

2X [0.7]

4X [0.35]

1

6

(0.1)
PIN 1 ID

6X 0.45 / 0.35

6X 0.22 / 0.12

⊕ | 0.07Ⓜ | C | B | A
   | 0.05Ⓜ | C
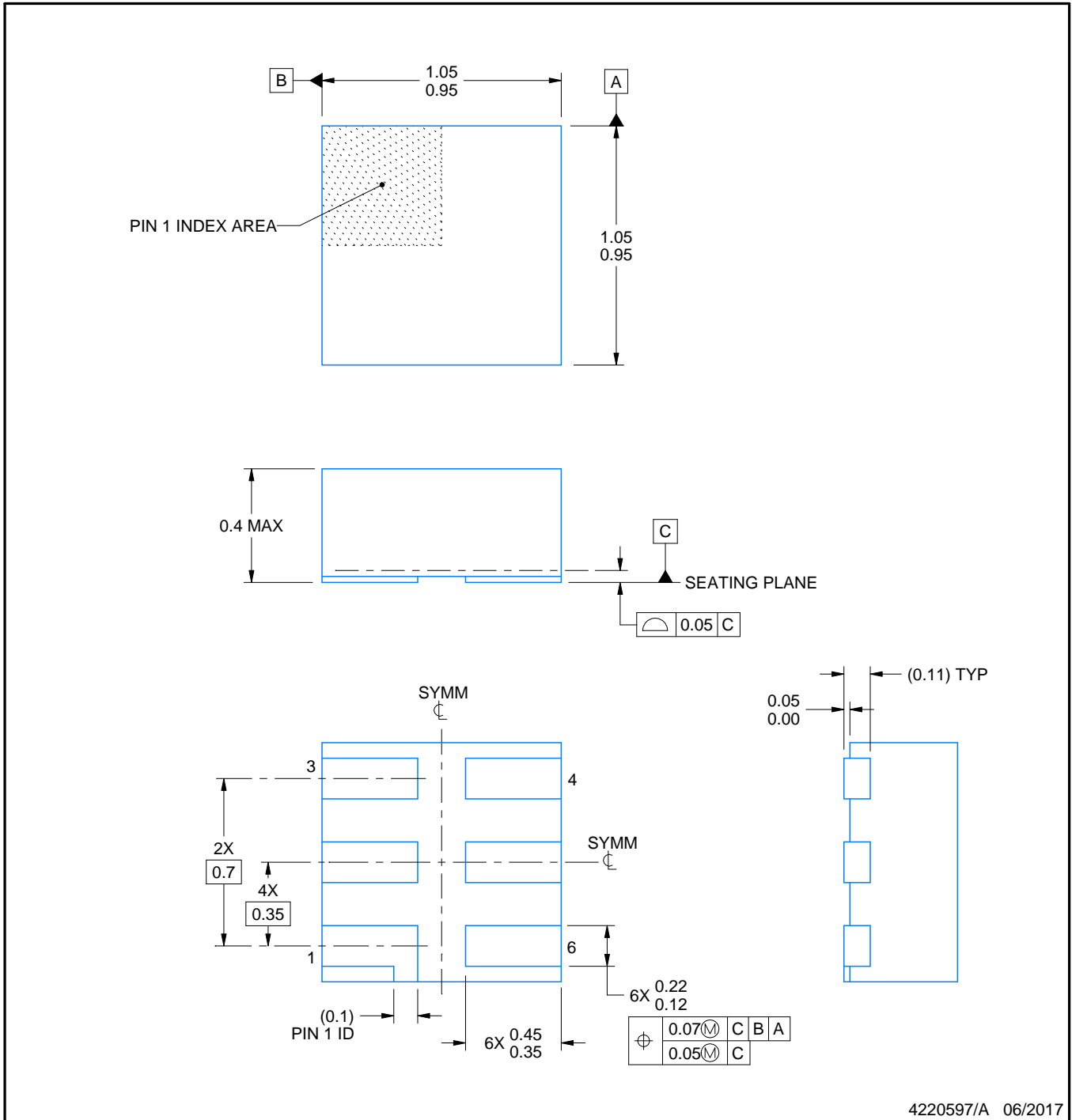
4220597/A   06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

6X (0.6)

1

6X (0.17)

(R0.05) TYP

6

SYMM
℄

4X (0.35)

3

4

SYMM
℄

(0.8)
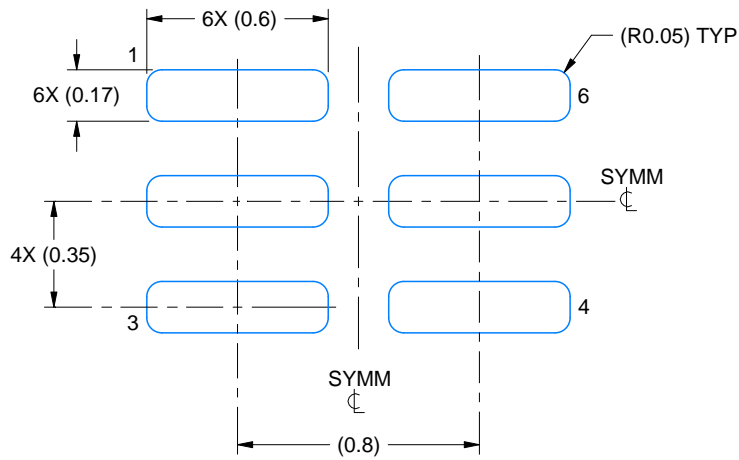
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**
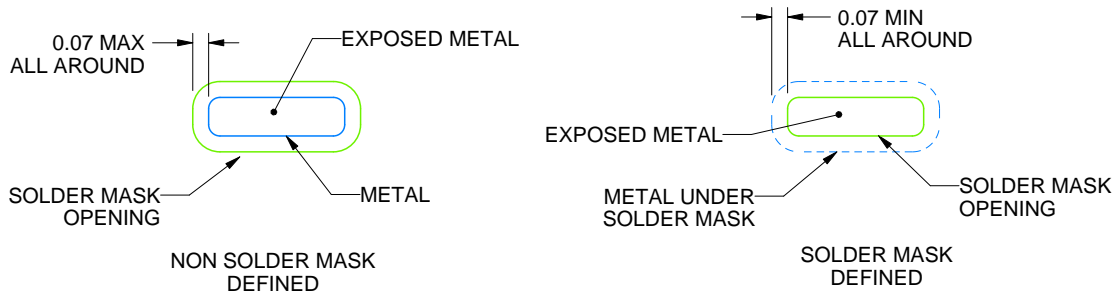
SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6X (0.6)

1

6X (0.17)

(R0.05) TYP

6

SYMM

4X (0.35)

3

4

SYMM

(0.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A   06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.