Product Specification

PE42510A

SPDT High Power UltraCMOS®
Reflective RF Switch 30 - 2000 MHz

Product Description

The following specification defines an SPDT (single pole double throw) switch for use in cellular and other wireless applications. The PE42510A uses Peregrine's UltraCMOS® process and it also features HaRP™ technology enhancements to deliver high linearity and exceptional harmonics performance. HaRP™ technology is an innovative feature of the UltraCMOS® process providing upgraded linearity performance.

The PE42510A is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- No blocking capacitors required
- 50 Watt P1dB compression point
- 10 Watts <8:1 VSWR (Normal Operation)
- 29 dB Isolation @ 800 MHz
- <0.3 dB Insertion Loss at 800 MHz
- $2f_o$ and $3f_o$ < -84 dBc @ 42.5 dBm
- ESD rugged to 2.0 kV HBM
- 32-lead 5x5x0.85 mm QFN package

Figure 1. Functional Diagram

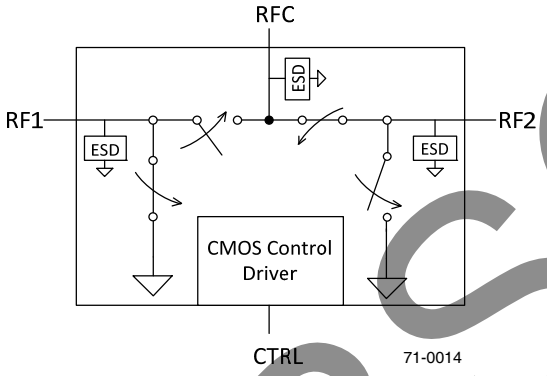

Figure 2. Package Type

32-lead 5x5x0.85 mm

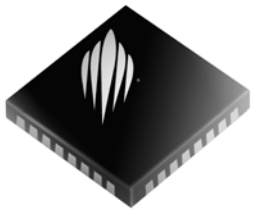

Table 1. Electrical Specifications @ 25°C, V_{DD} = 3.3V (Z_S = Z_L = 50 Ω) unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
RF Insertion Loss	30 MHz ≤ 1 GHz 1 GHz < 2 GHz		0.4 0.5	0.6 0.7	dB dB
0.1 dB Input Compression Point	800 MHz, 50% duty cycle		45.4		dBm
Isolation (Supply Biased): RF to RFC	800 MHz	25	29		dB
Unbiased Isolation: RF - RFC, V_{DD}, V1=0V	27 dBm, 800 MHz	5			dB
RF (Active Port) Return Loss		15	22		dB
2nd Harmonic 3rd Harmonic	800 MHz @ +42.5 dBm		-84	-81	dBc
Switching Time [2,3]	50% of CTRL to 10/90% of RF		25	31	µs

Notes: 1. The device was matched with 1.6 nH inductance per RF port
2. For high power applications, harmonics settling needs to be accounted for. Harmonics settling time is defined to be 50% of CTRL to 2fo/3fo within 3 dB of final value
3. For RF input power (50 Ω) ≥ 31 dBm, and operation above 30 MHz, the switching time and harmonics settling time is 100 µs Max

Figure 3. Pin Configuration (Top View)

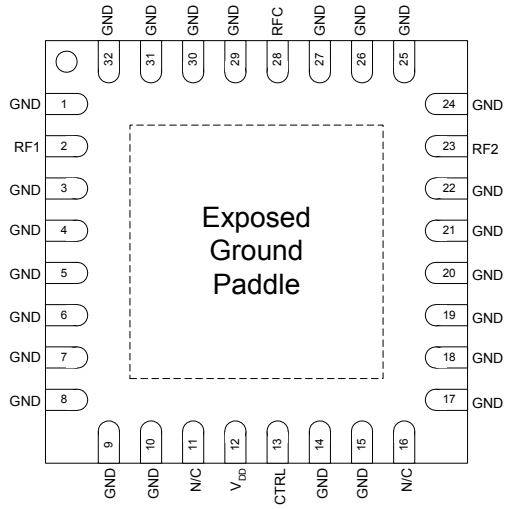

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	RF1	RF1 port
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	N/C	No Connect
12	V_{DD}	Nominal 3.3 V supply connection
13	CTRL	Control
14	GND	Ground
15	GND	Ground
16	N/C	Do Not Connect
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	RF2	RF2 port.
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	RFC	Common RF port for switch
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	GND	Ground
paddle	GND	Exposed ground paddle

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the 5x5x0.85 mm QFN package is MSL3.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
Frequency Range	30		2000	MHz
RF Input Power[1] (VSWR ≤8:1)			40	dBm
RF Input Power[2] (VSWR ≤8:1)			27	dBm
V_{DD} Power Supply Voltage	3.2	3.3	3.4	V
I_{DD} Power Supply Current		90	170	µA
Control Voltage High	1.4			V
Control Voltage Low			0.4	V
Operating Temperature Range (Case)	-40		85	°C
T_j Operating Junction Temperature			140	°C

Notes: 1. Supply biased
2. Supply unbiased

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power Supply Voltage	-0.3	4	V
V_I	Voltage on Any DC Input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage Temperature Range	-65	150	°C
T_{CASE}	Maximum Case Temperature		85	°C
T_j	Peak Maximum Junction Temperature (10 seconds max)		200	°C
P_{IN}	RF Input Power (VSWR 20:1, 10 seconds)		40	dBm
	RF Input Power (50 Ω)		45	dBm
	RF Input Power, Unbiased (VSWR 20:1)		27	dBm
P_D	Maximum Power Dissipation Due to RF Insertion Loss		2.2	W
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		2000	V

Absolute Maximum Ratings

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Table 5. Control Logic Truth Table

Path	CTRL
RFC – RF1	H
RFC – RF2	L

Evaluation Kit

The PE42510A Evaluation Kit board was designed to ease customer evaluation of the PE42510A RF switch.

DC power is supplied through J10, with V_{DD} on pin 9, and GND on the entire lower row of even numbered pins. To evaluate a switch path, add or remove jumpers on CTRL/V1 (pin 3) using *Table 5* (adding a jumper pulls the CMOS control pin low and removing it allows the on-board pull-up resistor to set the CMOS control pin high). J10 pins 1, 11, and 13 are N/C.

The RF common port (RFC) is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 paths are also connected through 50 Ω transmission lines via SMA connectors. A 50 Ω through transmission line is available via SMA connectors J8 and J9. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. An open-ended 50 Ω transmission line is also provided at J7 for calibration if needed.

Figure 4. Evaluation Board Layouts

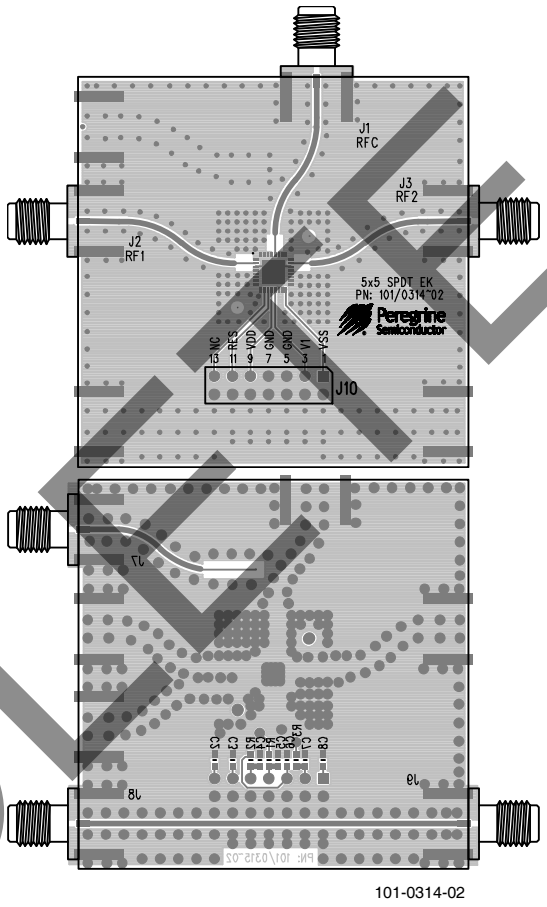

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Figure 5. Evaluation Board Schematic

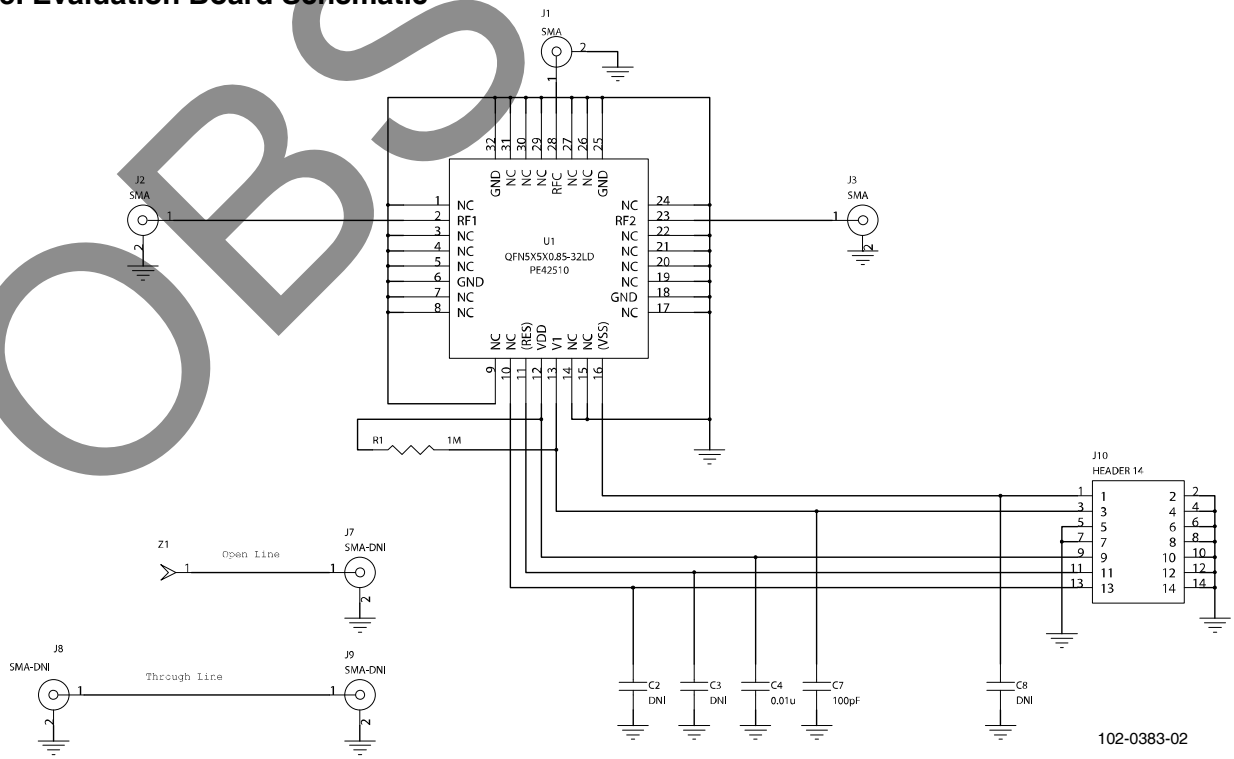

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Figure 6. RF-RFC Insertion Loss, V_{DD} = 3.3V

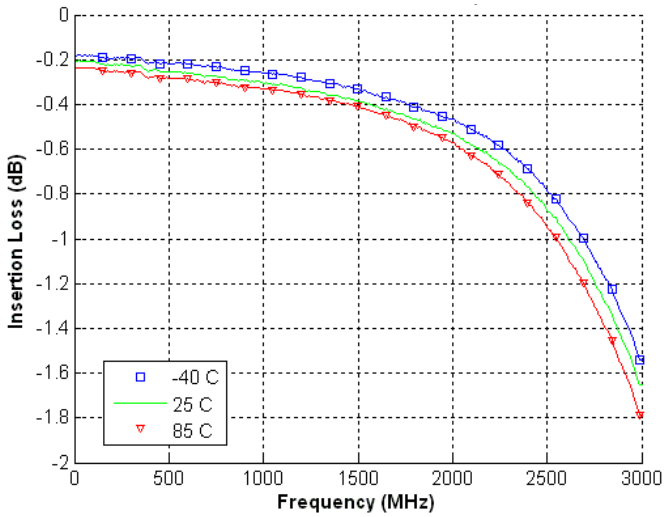


Figure 7. RF-RFC Insertion Loss, +25°C

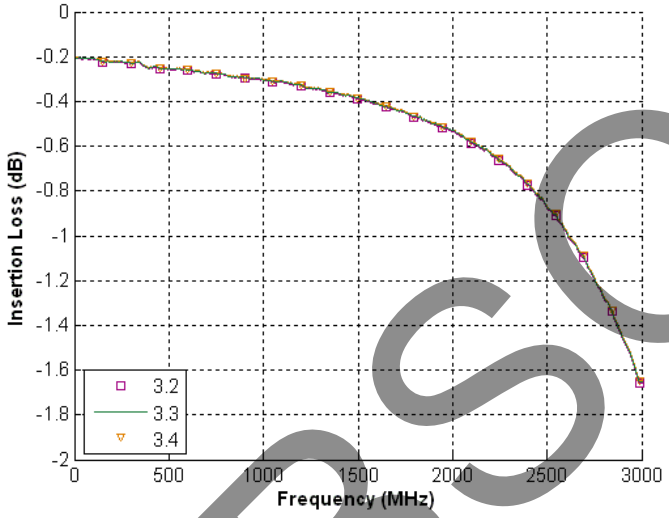


Figure 8. RFC-RF Isolation, V_{DD} = 3.3V

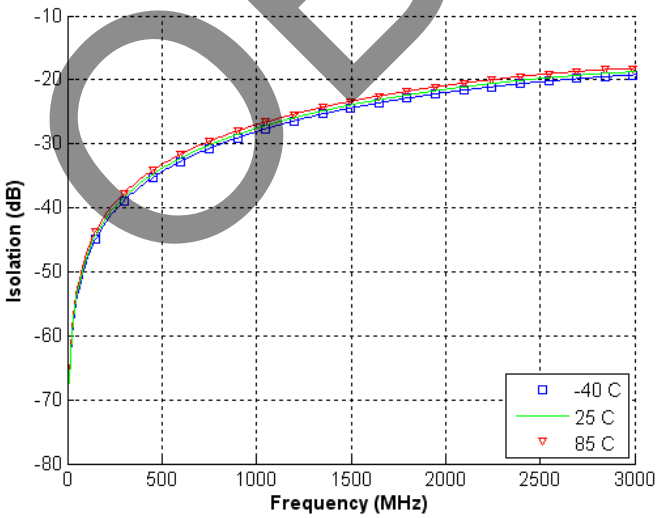


Figure 9. RFC-RF Isolation, +25°C

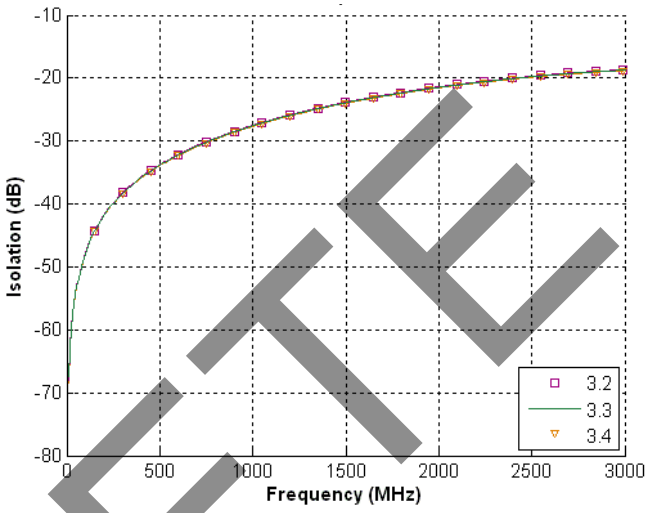


Figure 10. RF Return Loss, V_{DD} = 3.3V

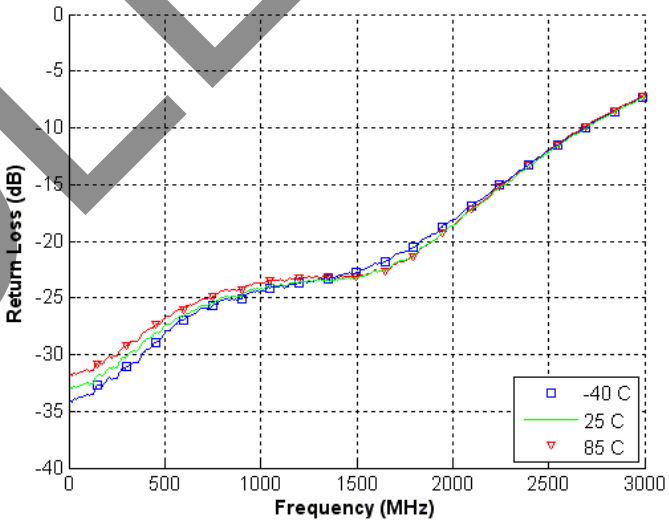
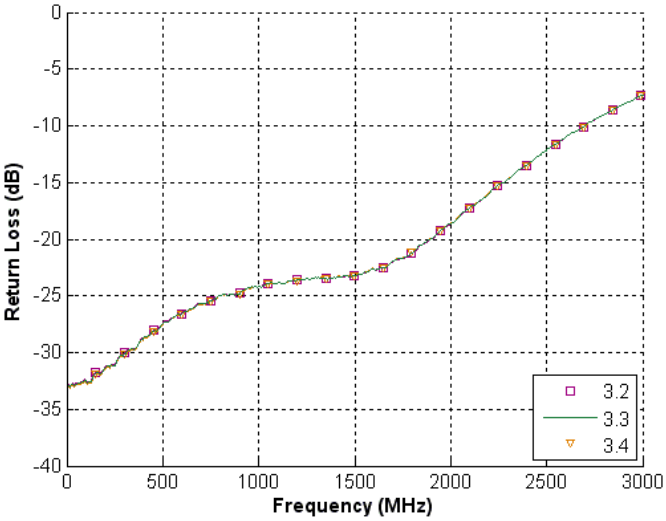


Figure 11. RF Return Loss, +25°C



Thermal Data

Though the insertion loss for this part is very low, when handling high power RF signals, the part can get quite hot.

Figure 12 shows the estimated power dissipation for a given incident RF power level. Multiple curves are presented to show the effect of poor VSWR conditions. VSWR conditions that present short circuit loads to the part can cause significantly more power dissipation than with proper matching.

Figure 13 shows the estimated maximum junction temperature of the part for similar conditions.

Note that both of these charts assume that the case (GND slug) temperature is held at 85°C. Special consideration needs to be made in the design of the PCB to properly dissipate the heat away from the part and maintain the 85°C maximum case temperature. It is recommended to use best design practices for high power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Special care also needs to be made to alleviate solder voiding under the part.

Table 6. Theta JC

Parameter	Min	Typ	Max	Units
Theta JC (+85°C)		24.0		C/W

Figure 12. Power Dissipation

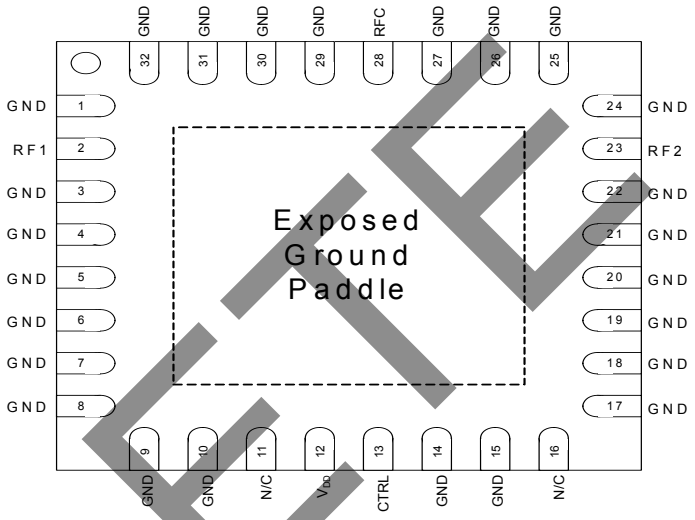
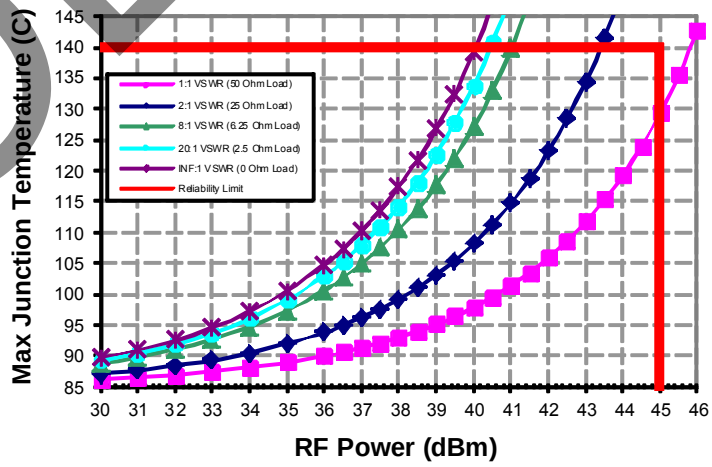
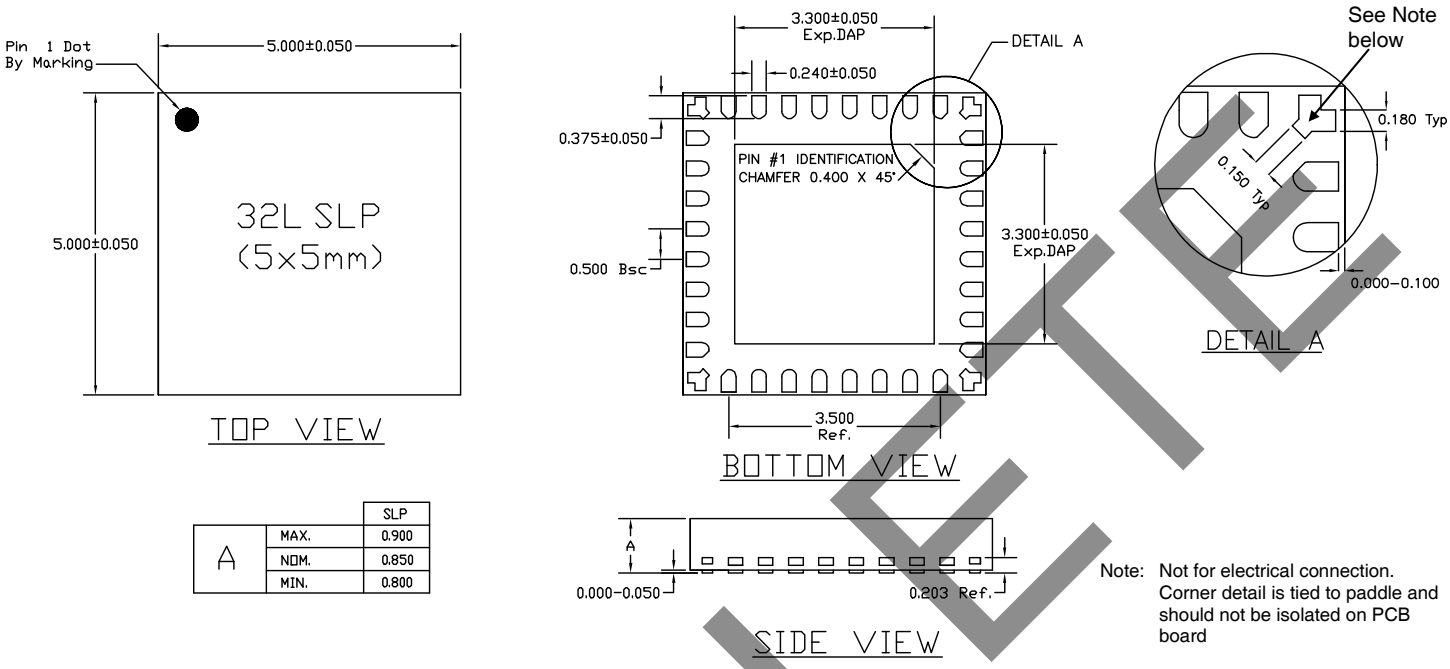


Figure 13. Maximum Junction Temperature



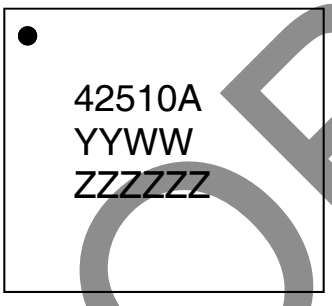
Note: Case temperature = 85°C

Figure 14. Package Drawing



		SLP
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

Figure 14. Top Marking Specification



● = Pin 1 designator

42510A = Six digit part number

YYWW = Date Code, last two digits of the year and work week

ZZZZZZ = Six digits of the lot number

Figure 15. Tape and Reel Specs

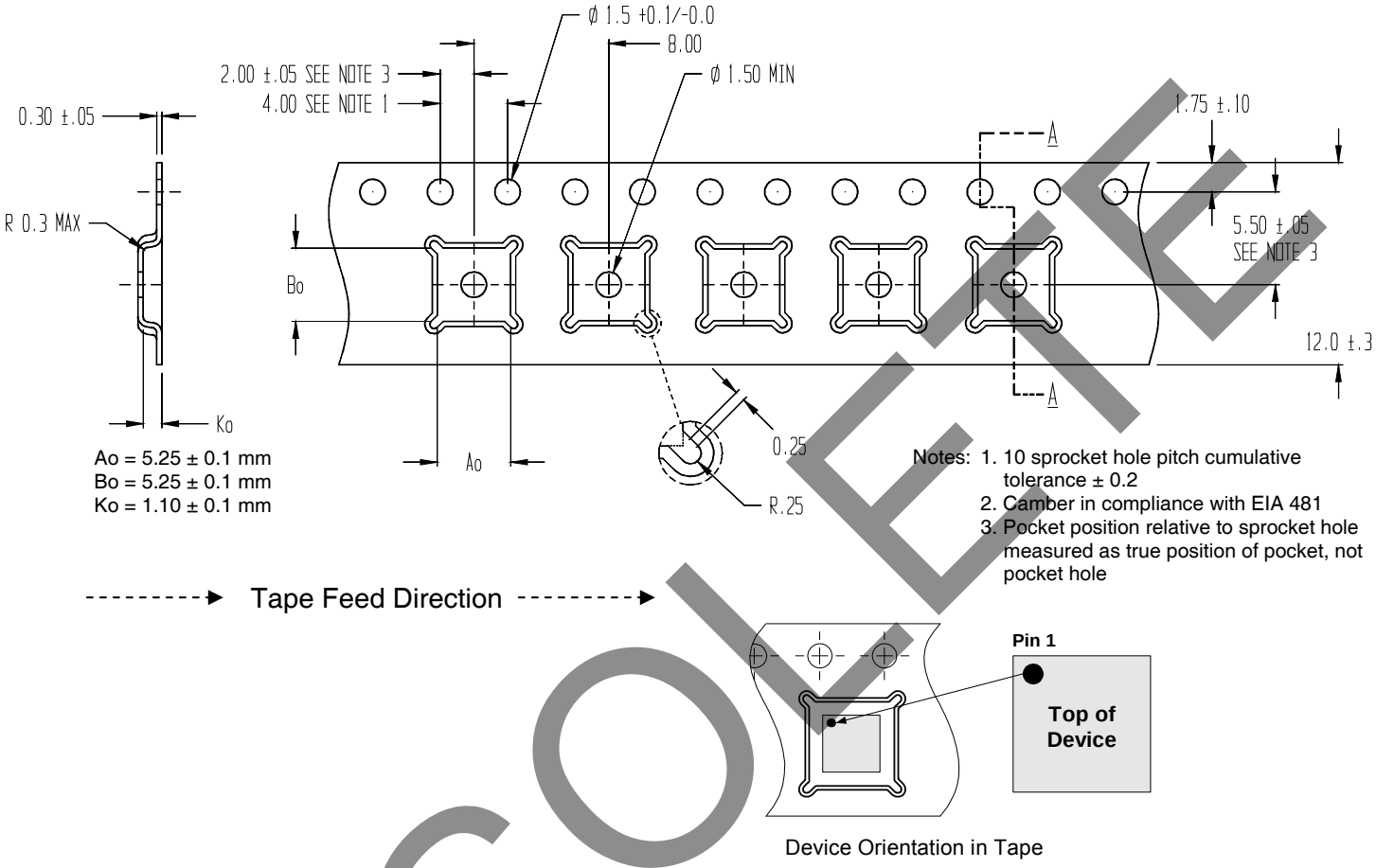


Table 7. Ordering Information

Order Code	Description	Package	Shipping Method
PE42510AMLI	Parts in Tubes or Cut Tape	Green 32-lead 5x5mm QFN	73 units/Tube
PE42510AMLI-X	Parts on Tape and Reel	Green 32-lead 5x5mm QFN	500 units/T&R
EK42510-01	Evaluation Kit	Evaluation Kit	1/Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.