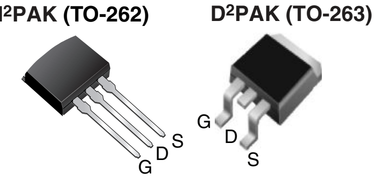
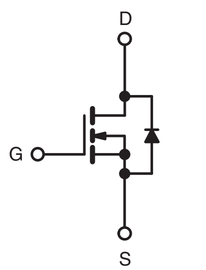
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 600 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 4.4 |
| $Q_g$ (Max.) (nC) | 18 | |
| $Q_{gs}$ (nC) | 3.0 | |
| $Q_{gd}$ (nC) | 8.9 | |
| Configuration | Single | |

I2PAK (TO-262) D2PAK (TO-263)




N-Channel MOSFET

## FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Surface Mount (IRFBC20S, SiHFBC20S)
- Low-Profile Through-Hole (IRFBC20L, SiHFBC20L)
- Available in Tape and Reel (IRFBC20, SiiHFBC20S)
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC

RoHS* COMPLIANT
HALOGEN FREE Available

## DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D2PAK is a surface mount power package capable of the accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D2PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRFBC20L, SiHFBC20L) is a available for low-profile applications.

| ORDERING INFORMATION | | | |
|---|---|---|---|
| Package | D2PAK (TO-263) | D2PAK (TO-263) | I2PAK (TO-262) |
| Lead (Pb)-free and Halogen-free | SiHFBC20S-GE3 | SiHFBC20STRL-GE3[a] | SiHFBC20L-GE3 |
| Lead (Pb)-free | IRFBC20SPbF | IRFBC20STRLPbF[a] | IRFBC20LPbF |
| | SiHFBC20S-E3 | SiHFBC20STL-E3[a] | SiHFBC20L-E3 |

**Note**
a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | 600 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current[e] | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 2.2 | A |
| | | $T_C$ = 100 °C | | 1.4 | |
| Pulsed Drain Current[a, e] | | | $I_{DM}$ | 8.0 | |
| Linear Derating Factor | | | | 0.40 | W/°C |
| Single Pulse Avalanche Energy[b, e] | | | $E_{AS}$ | 84 | mJ |
| Avalanche Current[a] | | | $I_{AR}$ | 2.2 | A |
| Repetiitive Avalanche Energy[a] | | | $E_{AR}$ | 5.0 | mJ |
| Maximum Power Dissipation | $T_A$ = 25 °C | | $P_D$ | 3.1 | W |
| | $T_C$ = 25 °C | | | 50 | |
| Peak Diode Recovery dV/dt[c, e] | | | dV/dt | 3.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |

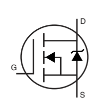
**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 31 mH, $R_g$ = 25 Ω, $I_{AS}$ = 2.2 A (see fig. 12).
c. $I_{SD} \leq$ 2.2 A, dI/dt ≤ 40 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.
e. Uses IRFBC20, SiHFBC20 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient (PCB Mounted, steady-state)[a] | $R_{thJA}$ | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 2.5 | |

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0, $I_D$ = 250 μA | | 600 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA[c] | | - | 0.88 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | | - | - | 100 | μA |
| | | $V_{DS}$ = 480 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 500 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 1.3 A[b] | - | - | 4.4 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 1.3 A[c] | | 1.4 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5[c] | | - | 350 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 48 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 8.6 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V | $I_D$ = 2.0 A, $V_{DS}$ = 360 V, see fig. 6 and 13[b, c] | - | - | 18 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 3.0 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 8.9 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 300 V, $I_D$ = 2.0 A, $R_g$ = 18 Ω, $R_D$ = 150 Ω, see fig. 10[b, c] | | - | 10 | - | ns |
| Rise Time | $t_r$ | | | - | 23 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 30 | - | |
| Fall Time | $t_f$ | | | - | 25 | - | |
| Internal Source Inductance | $L_S$ | Between lead, and center of die contact | | - | 7.5 | - | nH |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode |  | - | - | 2.2 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 8.0 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 2.2 A, $V_{GS}$ = 0 V[b] | | - | - | 1.6 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 2.0 A, dI/dt = 100 A/μs[b, c] | | - | 290 | 580 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | - | 0.67 | 1.3 | μC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
c. Uses IRFBC20, SiHFBC20 data and test conditions.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

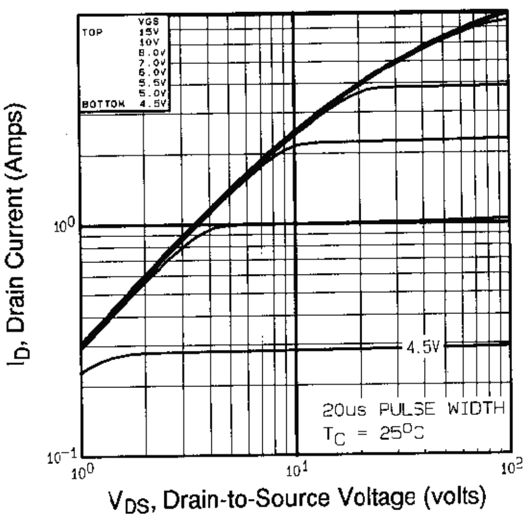



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

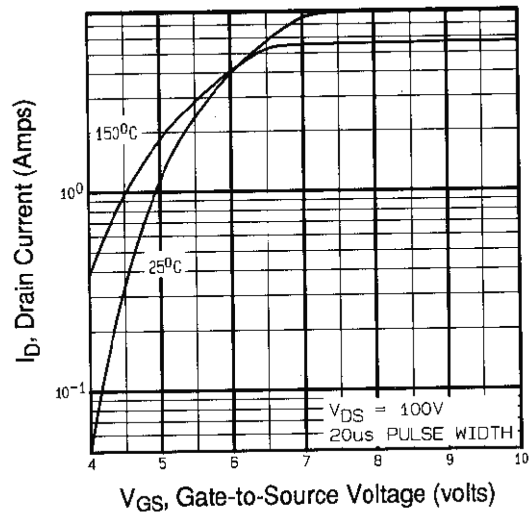



**Fig. 3 - Typical Transfer Characteristics**

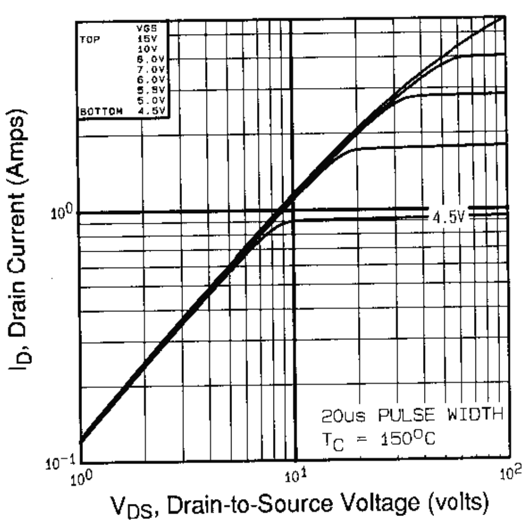



**Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C**

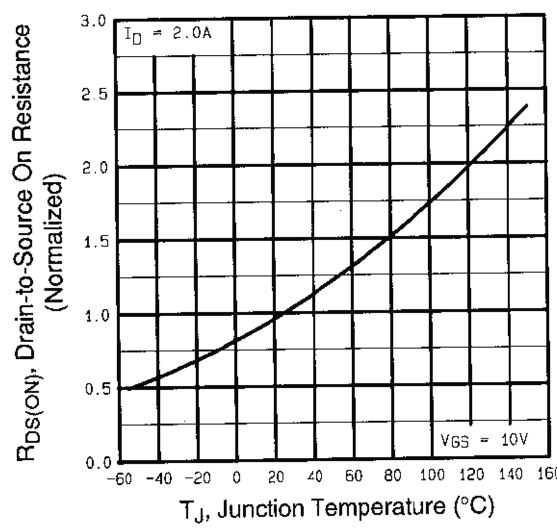



**Fig. 4 - Normalized On-Resistance vs. Temperature**

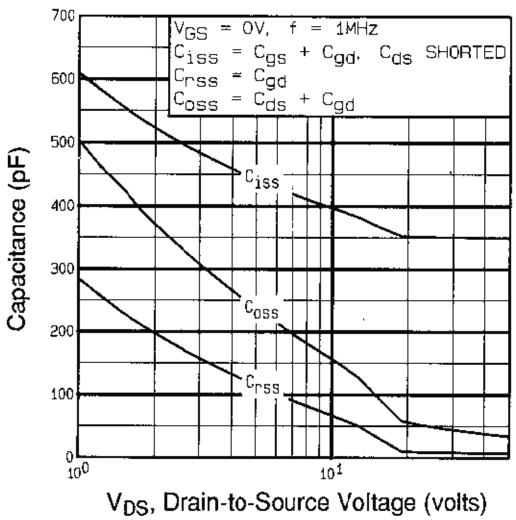



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

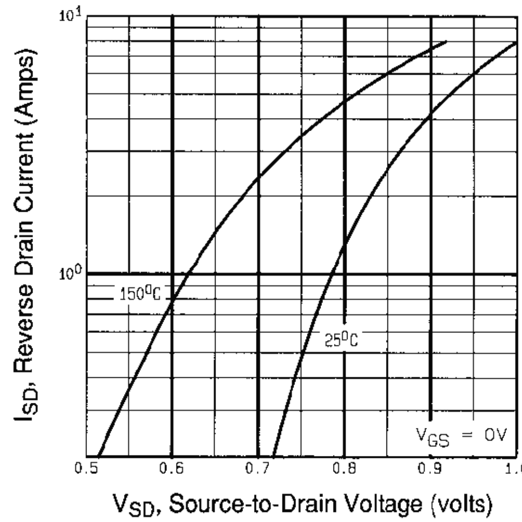



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

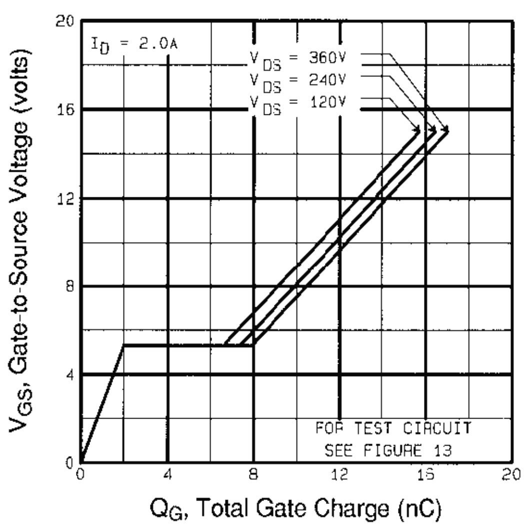



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

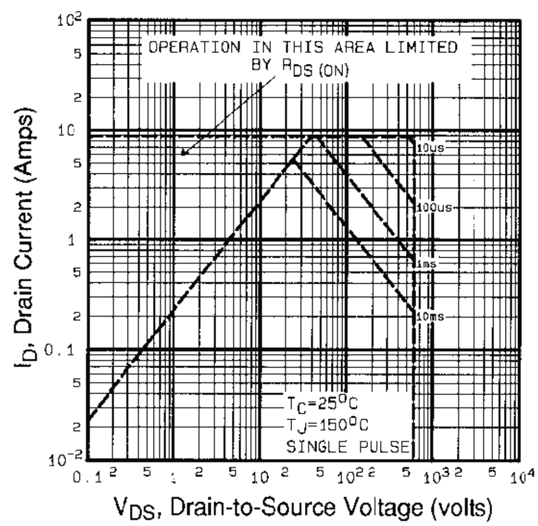



**Fig. 8 - Maximum Safe Operating Area**

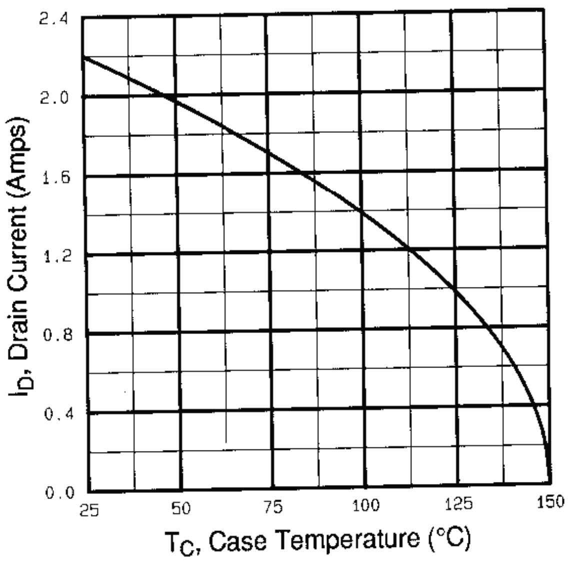



Fig. 9 - Maximum Drain Current vs. Case Temperature

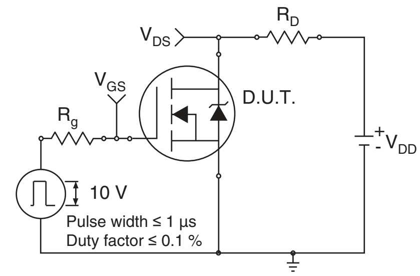



Fig. 10a - Switching Time Test Circuit

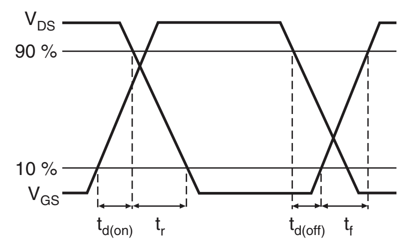



Fig. 10b - Switching Time Waveforms

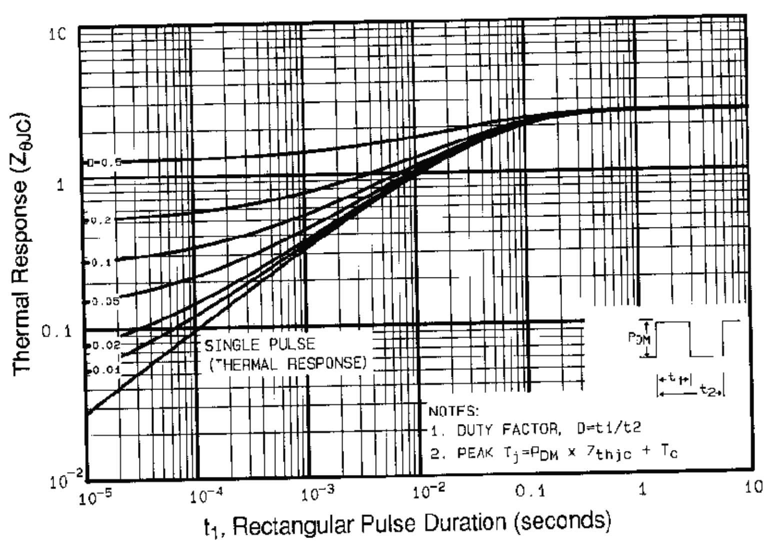



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

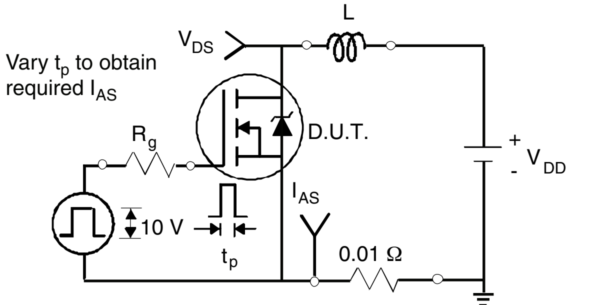



Fig. 12a - Unclamped Inductive Test Circuit

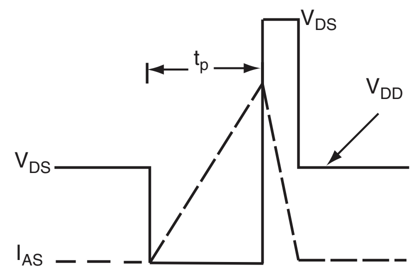



Fig. 12b - Unclamped Inductive Waveforms

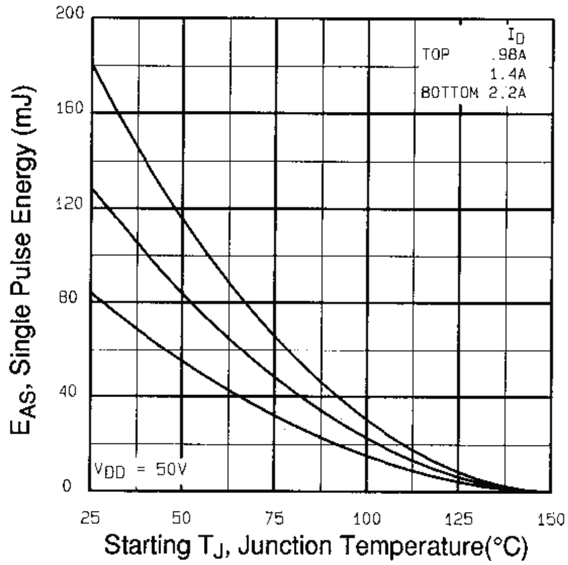



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

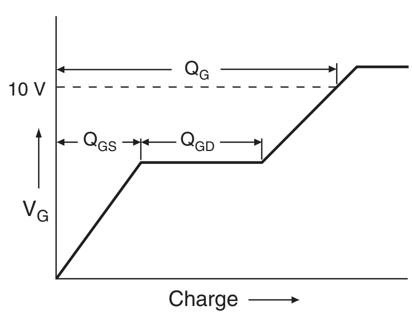



**Fig. 13a - Maximum Avalanche Energy vs. Drain Current**

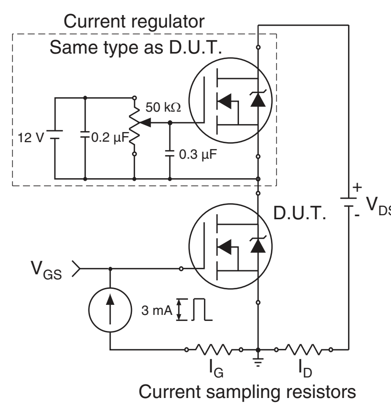
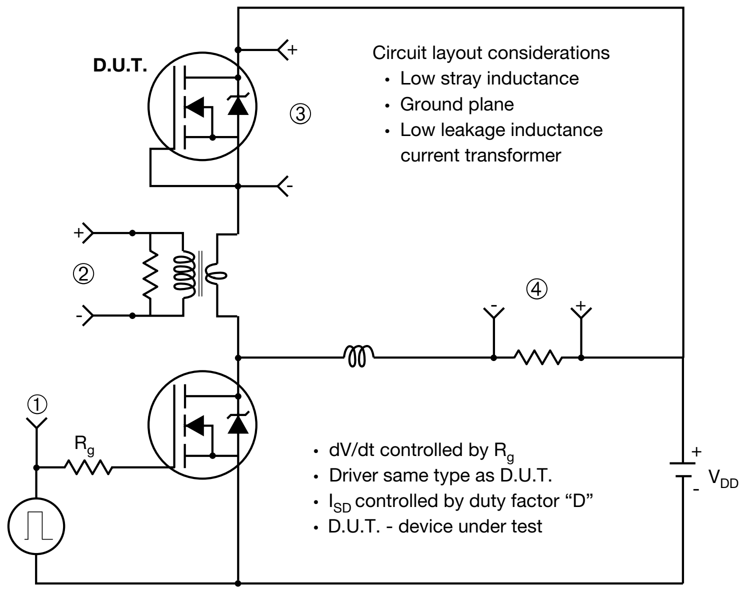
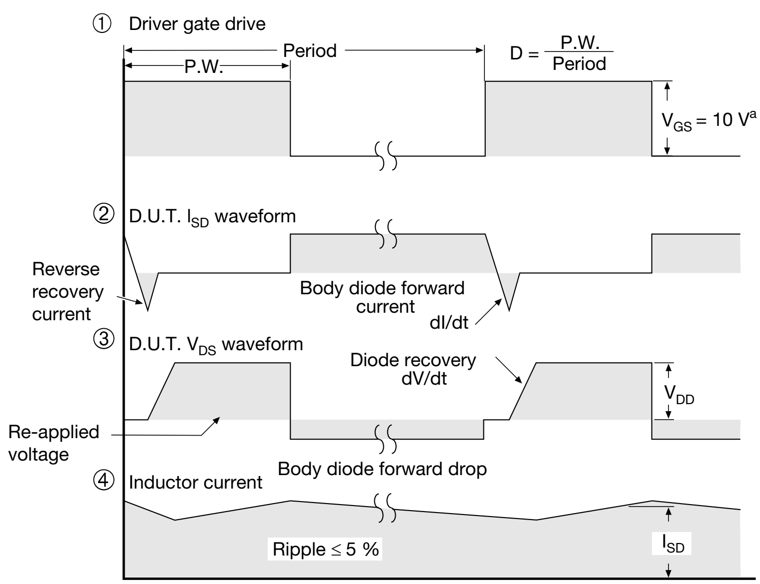



**Fig. 13b - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**



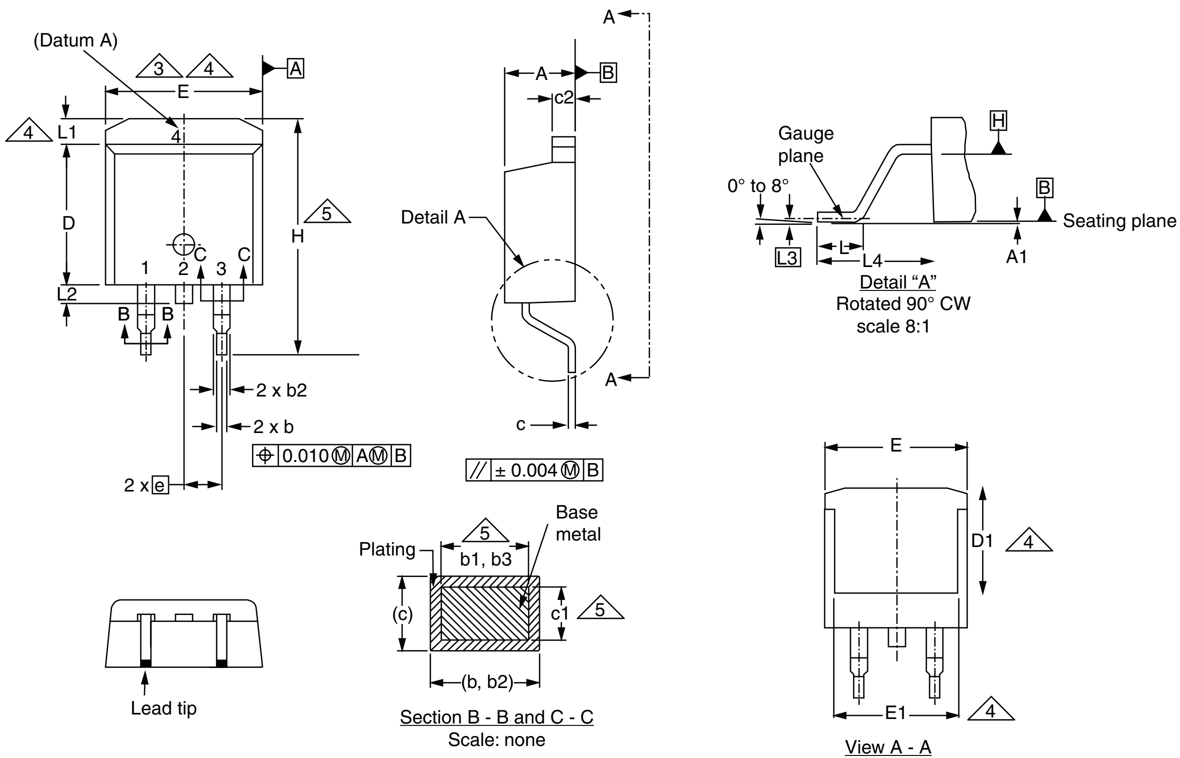

**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91107.*

## TO-263AB (HIGH VOLTAGE)



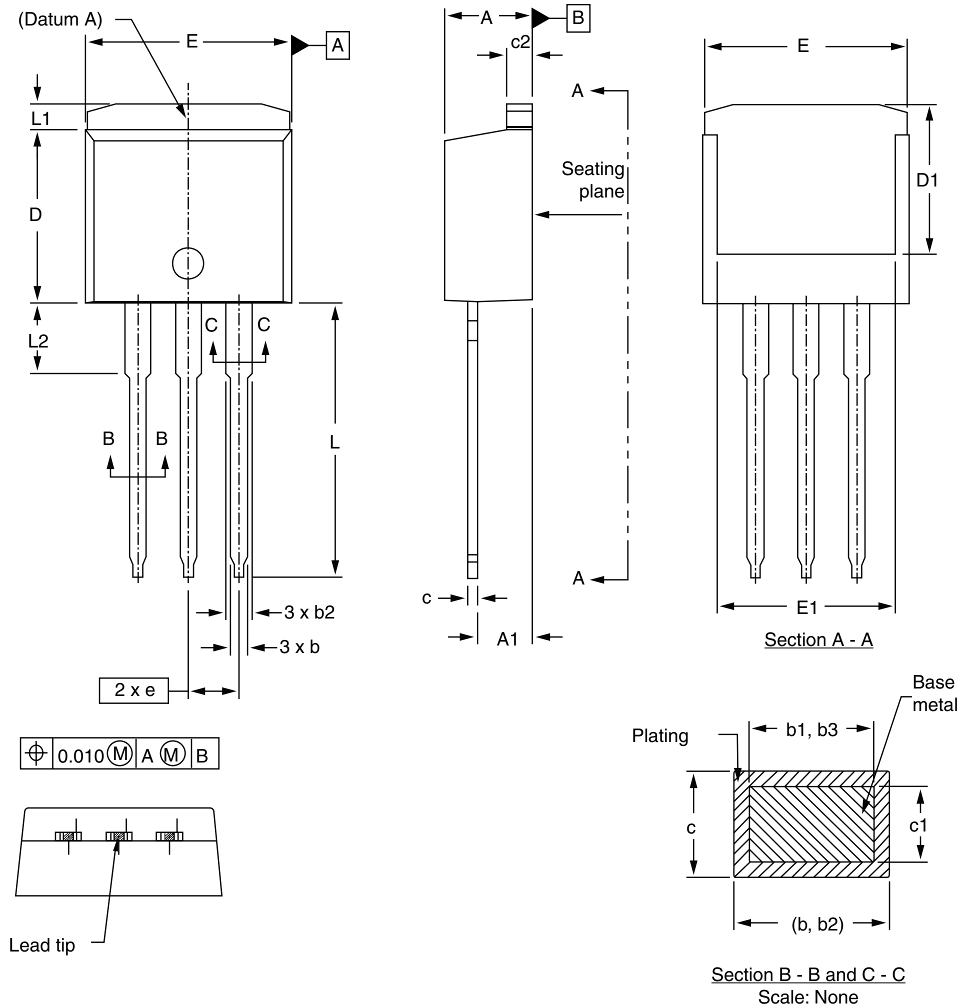

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

**Notes**
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

## I²PAK (TO-262) (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 2.03 | 3.02 | 0.080 | 0.119 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |

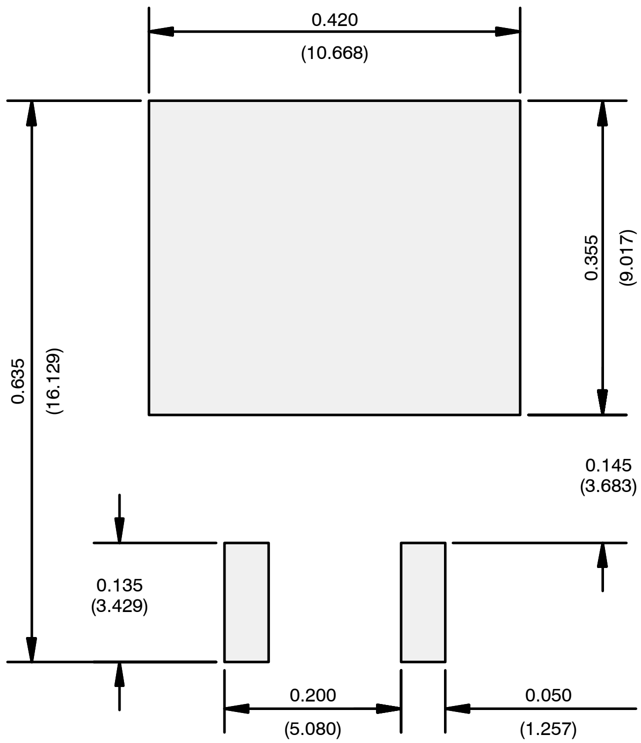
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D | 8.38 | 9.65 | 0.330 | 0.380 |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.46 | 14.10 | 0.530 | 0.555 |
| L1 | - | 1.65 | - | 0.065 |
| L2 | 3.56 | 3.71 | 0.140 | 0.146 |

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

## RECOMMENDED MINIMUM PADS FOR D$^2$PAK: 3-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

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