LP38512-1.8 1.5A Fast-Transient Response Low-Dropout Linear Voltage Regulator with Error Flag

Check for Samples: LP38512

FEATURES

- **2.25V to 5.5V Input Voltage Range**
- **1.8V Fixed Output Voltage**
- **1.5A Output Load Current**
- **±2.5% Accuracy Over Line, Load, and Full-Temperature Range from -40°C to +125°C**
- **Stable with Tiny 10 µF Ceramic Capacitors**
- **0.20% Output Voltage Load Regulation from 10 mA to 1.5A**
- **Enable Pin**
- **$\overline{\text{Error}}$ Flag Indicates Status of Output Voltage**
- **1uA of Quiescent Current in Shutdown**
- **40dB of PSRR at 100 kHz**
- **Over-Temperature and Over-Current Protection**
- **DDPAK/TO-263 and PFM Surface Mount Packages**

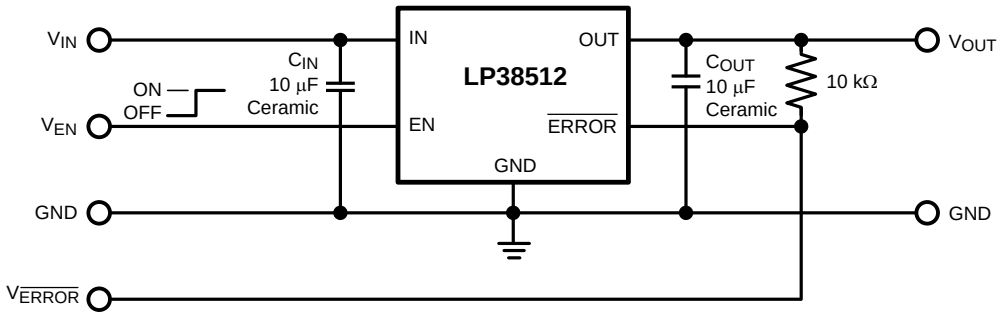
APPLICATIONS

- **Digital Core ASICs, FPGAs, and DSPs**
- **Servers**
- **Routers and Switches**
- **Base Stations**
- **Storage Area Networks**
- **DDR2 Memory**

DESCRIPTION

The LP38512-1.8 Fast-Transient Response Low-Dropout Voltage Regulator offers the highest-performance in meeting AC and DC accuracy requirements for powering Digital Cores. The LP38512-1.8 uses a proprietary control loop that enables extremely fast response to change in line conditions and load demands. Output Voltage DC accuracy is specified at 2.5% over line, load and full temperature range from -40°C to +125°C. The LP38512-1.8 is designed for inputs from the 2.5V, 3.3V, and 5.0V rail, is stable with 10 µF ceramic capacitors, and has a fixed 1.8V output. An Error Flag feature monitors the output voltage and notifies the system processor when the output voltage falls more than 15% below the nominal value. The LP38512-1.8 provides excellent transient performance to meet the demand of high performance digital core ASICs, DSPs, and FPGAs found in highly-intensive applications such as servers, routers/switches, and base stations.

Typical Application Circuit



Connection Diagram

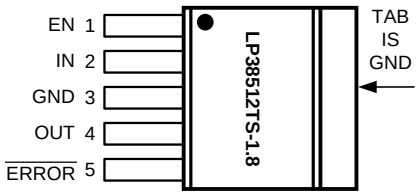


Figure 1. Top View
DDPAK/TO-263 5 Pin Package

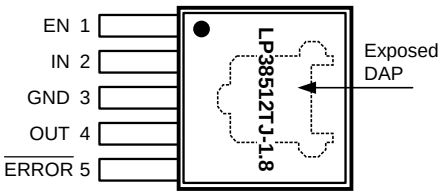


Figure 2. Top View
PFM 5 Pin Package

Table 1. Pin Descriptions for DDPAK/TO-263 and PFM Packages

Pin #	Pin Name	Function
1	EN	Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.
2	IN	Input Supply Pin
3	GND	Ground
4	OUT	Regulated Output Voltage Pin
5	$\overline{\text{ERROR}}$	$\overline{\text{ERROR}}$ Flag. A high level indicates that V_{OUT} is within typically 15% (V_{OUT} falling) of the nominal regulated voltage.
TAB/DAP	TAB/DAP	The DDPAK/TO-263 TAB, and the PFM DAP, is used as a thermal connection to remove heat from the device to an external heatsink. The TAB/DAP is internally connected to device pin 3, and is electrical ground connection.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Storage Temperature Range		−65°C to +150°C
Soldering Temperature [3]	DDPAK/TO-263	235°C, 30s
ESD Rating [4]		±2 kV
Power Dissipation[5]		Internally Limited
Input Pin Voltage (Survival)		−0.3V to +6.0V
Enable Pin Voltage (Survival)		−0.3V to +6.0V
Output Pin Voltage (Survival)		−0.3V to +6.0V
$\overline{\text{ERROR}}$ Pin Voltage (Survival)		0.3V to +6.0V
I_{OUT}(Survival)		Internally Limited

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperatures and times are for Sn-Pb (STD) only.
(4) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method is per JESD22-A114.
(5) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}).

Operating Ratings (1)

Input Supply Voltage, V_{IN}	2.25V to 5.5V
Enable Input Voltage, V_{EN}	0.0V to 5.5V
$\overline{\text{ERROR}}$ Pin Voltage	0.0V to V_{IN}
Output Current (DC)	0 mA to 1.5A
Junction Temperature (2)	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.

(2) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}).

Electrical Characteristics

Unless otherwise specified: V_{IN} = 2.5V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage Tolerance (1)	2.25V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 1.5A	-1.0 **−2.5**	0	+1.0 **+2.5**	%
$\Delta V_{OUT}/\Delta V_{IN}$	Output Voltage Line Regulation (2) (1)	2.25V ≤ V_{IN} ≤ 5.5V	-	0.02 **0.06**	-	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (3) (1)	10 mA ≤ I_{OUT} ≤ 1.5A	-	0.25 **0.40**	-	%/A
V_{DO}	Dropout Voltage (4)	I_{OUT} = 1.5A	-	250	340 **400**	mV
I_{GND}	Ground Pin Current, Output Enabled	I_{OUT} = 10 mA $\overline{\text{ERROR}}$ pin = GND	-	7.5	11 **12**	mA
		I_{OUT} = 1.5A $\overline{\text{ERROR}}$ pin = GND	-	9.5	13 **14**	
	Ground Pin Current, Output Disabled	V_{EN} = 0.50V $\overline{\text{ERROR}}$ pin = GND	-	0.1	3.5 **12**	µA
I_{SC}	Short Circuit Current	V_{OUT} = 0V	-	2.5	-	A
Enable Input						
$V_{EN(ON)}$	Enable ON Threshold	V_{EN} rising from 0.50V until V_{OUT} = ON	0.90 **0.80**	1.20	1.50 **1.60**	V
$V_{EN(OFF)}$	Enable OFF Threshold	V_{EN} falling from 1.60V until V_{OUT} = OFF	0.60 **0.50**	1.00	1.40 **1.50**	
$V_{EN(HYS)}$	Enable Hysteresis	$V_{EN(ON)}$ - $V_{EN(OFF)}$	-	200	-	mV
$t_{d(OFF)}$	Turn-off delay	Time from V_{EN} < $V_{EN(OFF)}$ to V_{OUT} = OFF, I_{LOAD} = 1.5A	-	1	-	µs
$t_{d(ON)}$	Turn-on delay	Time from V_{EN} >$V_{EN(ON)}$ to V_{OUT} = ON, I_{LOAD} = 1.5A	-	25	-	
I_{EN}	Enable Pin Current	V_{EN} = V_{IN}	-	1	-	nA
		V_{EN} = 0V	-	-1	-	
$\overline{\text{ERROR}}$ Flag						

(1) The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

(2) Output voltage line regulation is defined as the change in output voltage from the nominal value (ΔV_{OUT}) due to a change in the voltage at the input (ΔV_{IN}).

(3) Output voltage load regulation is defined as the change in output voltage from the nominal value (ΔV_{OUT}) due to a change in the load current at the output (ΔI_{OUT}).

(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. For the LP38512-1.8 the minimum V_{IN} operating voltage is the limiting factor.

Electrical Characteristics (continued)

Unless otherwise specified: V_{IN} = 2.5V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	$\overline{\text{Error}}$ Flag Threshold(5)	V_{OUT} rising threshold where $\overline{\text{ERROR}}$ Flag goes high	**78**	90	**98**	%
		V_{OUT} falling threshold where $\overline{\text{ERROR}}$ Flag goes low	**74**	85	**93**	
$V_{ERROR(SAT)}$	$\overline{\text{ERROR}}$ Flag Saturation Voltage	I_{SINK} = 100 µA	-	12.5	**45**	mV
I_{lk}	ERROR Flag Pin Leakage Current	$V_{\overline{ERROR}}$ = 5.5V	-	1	-	nA
t_d	$\overline{\text{ERROR}}$ Flag Delay time		-	1	-	µs
AC Parameters						
PSRR	Ripple Rejection	V_{IN} = 2.5V f = 120Hz	-	73	-	dB
		V_{IN} = 2.5V f = 1 kHz	-	73	-	
e_n	Output Noise Density	f = 120Hz	-	2	-	nV/$\sqrt{\text{Hz}}$
	Output Noise Voltage	BW = 100Hz – 100kHz	-	75	-	µV (RMS)
Thermal Characteristics						
T_{SD}	Thermal Shutdown	T_J rising	-	165	-	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	T_J falling from T_{SD}	-	10	-	
θ_{J-A}	Thermal Resistance Junction to Ambient(6)	DDPAK/TO-263 and PFM	-	60	-	°C/W
θ_{J-C}	Thermal Resistance Junction to Case	DDPAK/TO-263 and PFM	-	3	-	°C/W

(5) The $\overline{\text{ERROR}}$ Flag thresholds are specified as percentage of the nominal regulated output voltage. See Application Information.
(6) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}).

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

V_{OUT} vs Temperature

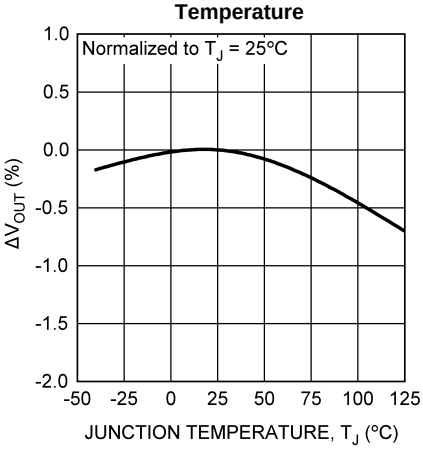


Figure 3.

V_{OUT} vs V_{IN}

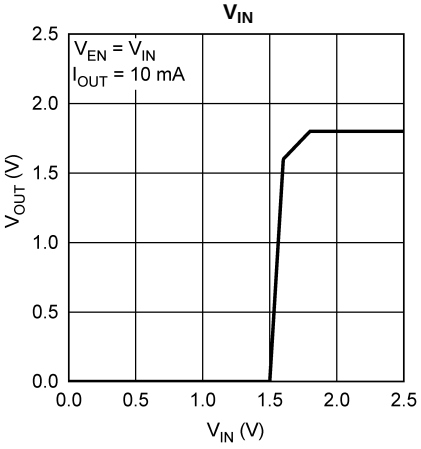


Figure 4.

Ground Pin Current (I_{GND}) vs V_{IN}

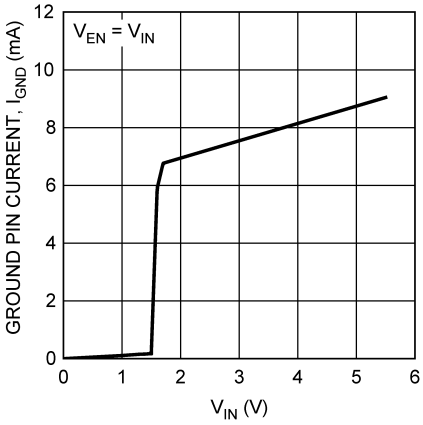


Figure 5.

Ground Pin Current (I_{GND}) vs Temperature

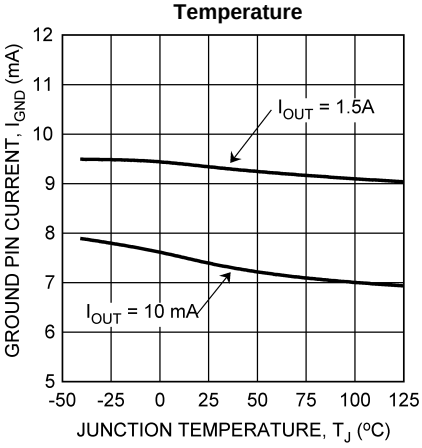


Figure 6.

Ground Pin Current(I_{GND}) vs Temperature, V_{EN} = 0.5V

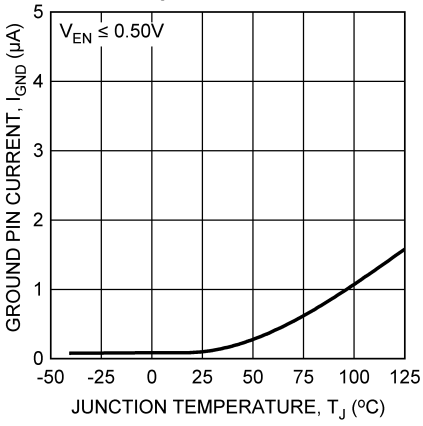


Figure 7.

Enable Thresholds vs Temperature

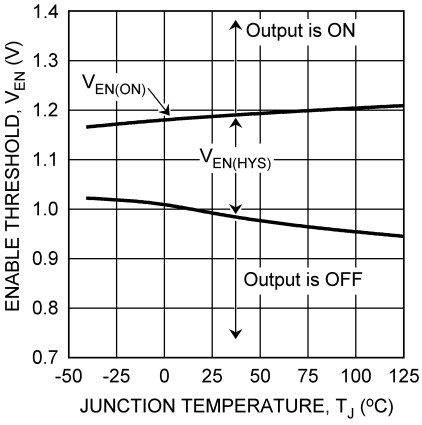


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

V_{OUT} vs V_{EN} ($t_{d(ON)}$)

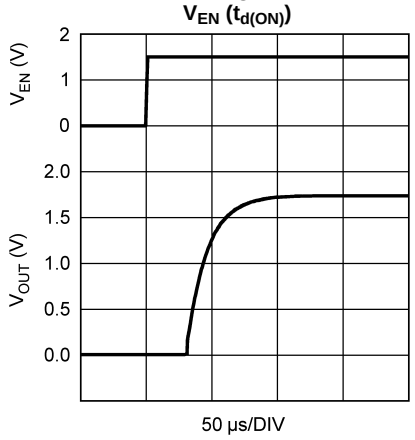


Figure 9.

V_{OUT} vs V_{EN} ($t_{d(OFF)}$)

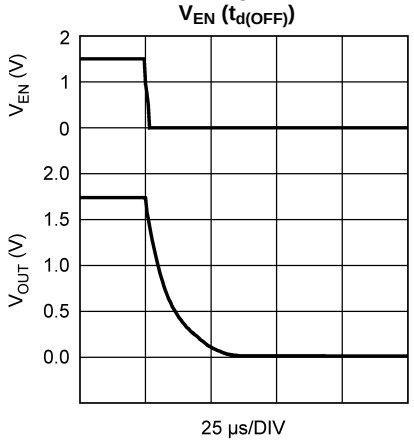


Figure 10.

V_{OUT} ERROR Flag Threshold vs Temperature

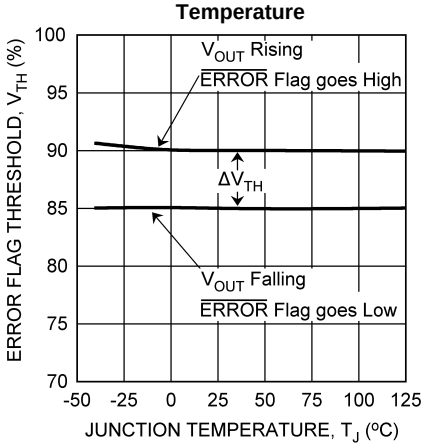


Figure 11.

ERROR Flag Low vs Temperature

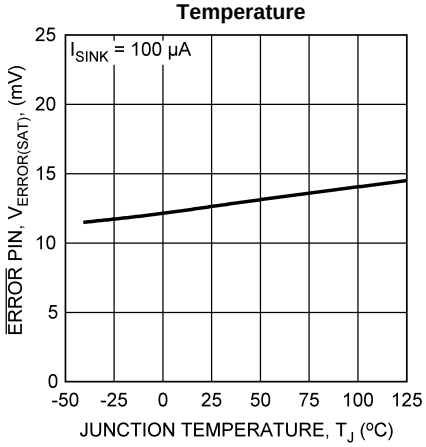


Figure 12.

Load regulation vs Temperature

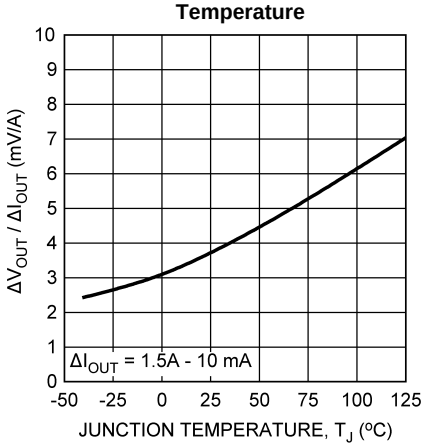


Figure 13.

Line Regulation vs Temperature

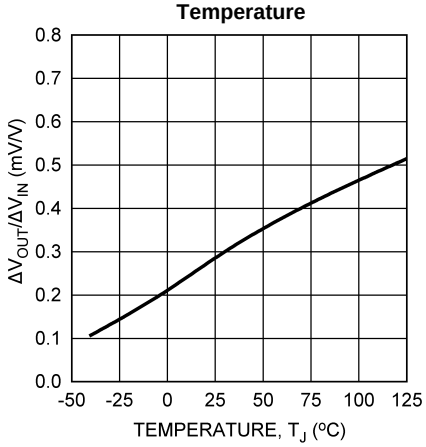


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

Current Limit vs Temperature

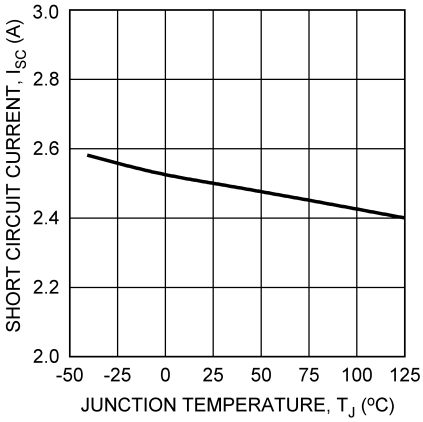


Figure 15.

Load Transient, 10 mA to 1.5A
C_{OUT} = 10 µF Ceramic

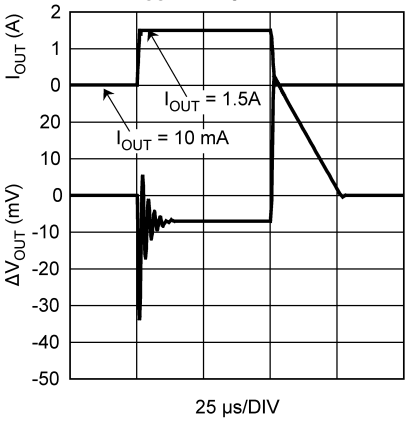


Figure 16.

Load Transient, 10 mA to 1.5A
C_{OUT} = 10 µF Ceramic + 100 µF Aluminum

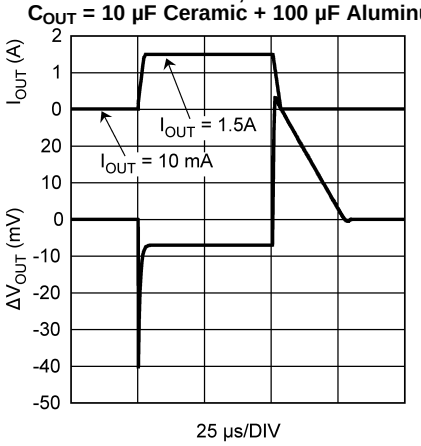


Figure 17.

Load Transient, 500 mA to 1.5A
C_{OUT} = 10 µF Ceramic

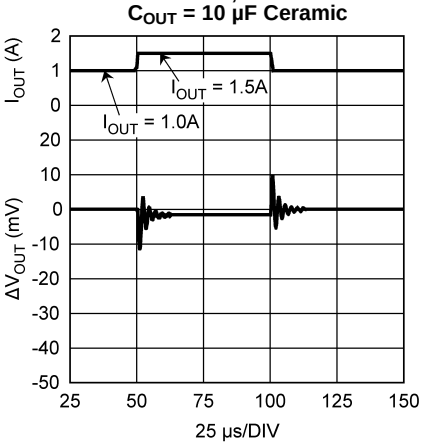


Figure 18.

Load Transient, 500 mA to 1.5A
C_{OUT} = 10 µF Ceramic + 100 µF Aluminum

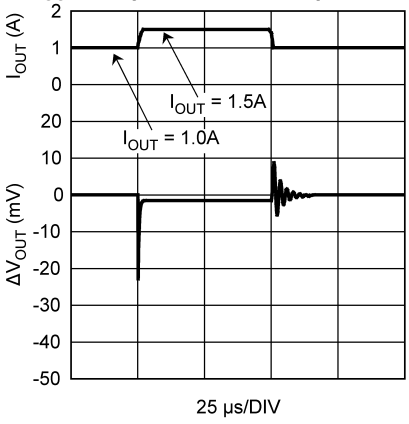


Figure 19.

Line Transient

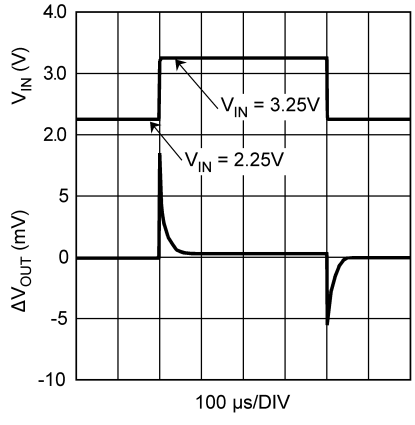


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

PSRR, 10Hz to 1MHz

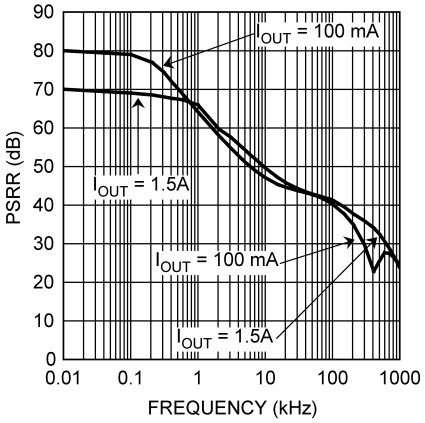


Figure 21.

Noise

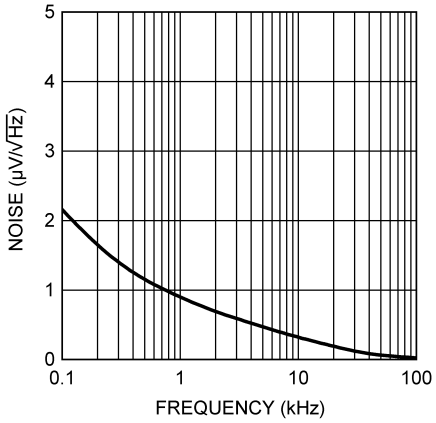
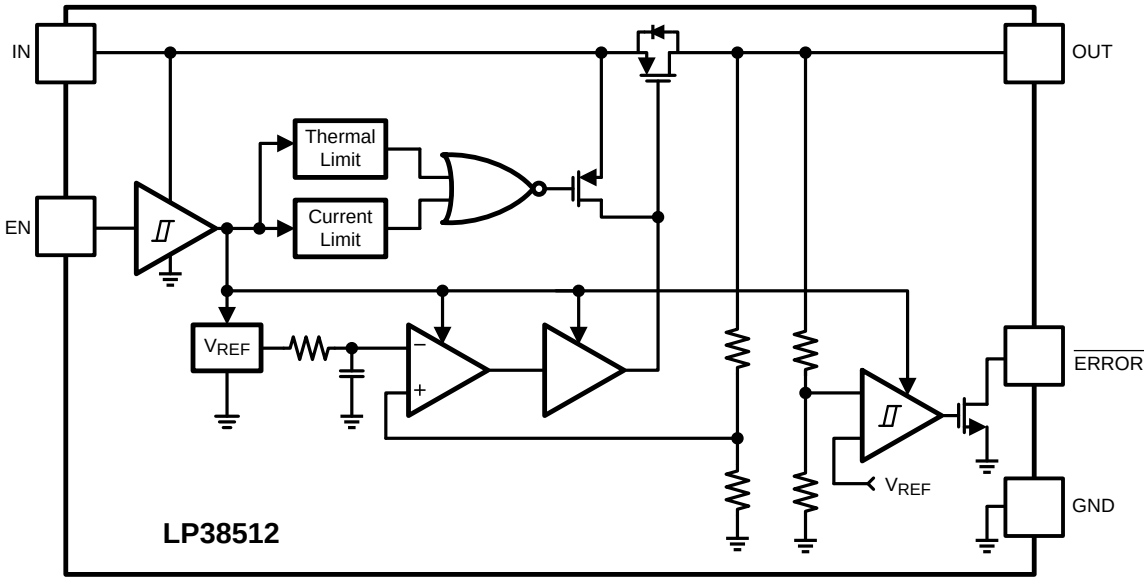


Figure 22.

Block Diagram



APPLICATION INFORMATION

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

Input Capacitor

A ceramic input capacitor of at least 10 µF is required. For general usage across all load currents and operating conditions, a 10 µF ceramic input capacitor will provide satisfactory performance.

Output Capacitor

A ceramic capacitor with a minimum value of 10 µF is required at the output pin for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pin using traces which have no other currents flowing through them. As long as the minimum of 10 µF ceramic is met, there is no limitation on any additional capacitance.

X7R and X5R dielectric ceramic capacitors are strongly recommended, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Z5U and Y5V dielectric ceramics are not recommended as the capacitance will drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

While V_{IN} is high enough to keep the control circuity alive, and the Enable pin is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full on condition when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided.

The internal PFET pass element in the LP38512 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output voltage to input voltage differential is more than 500 mV (typical) the parasitic diode becomes forward biased and current flows from the output pin to the input through the diode. The current in the parasitic diode should limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this protective clamp.

SHORT-CIRCUIT PROTECTION

The LP38512 is short circuit protected, and in the event of a peak over-current condition the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the POWER DISSIPATION/HEATSINKING section for power dissipation calculations.

ENABLE OPERATION

The Enable ON threshold is typically 1.2V, and the OFF threshold is typically 1.0V. To ensure reliable operation the Enable pin voltage must rise above the maximum $V_{EN(ON)}$ threshold and must fall below the minimum $V_{EN(OFF)}$ threshold. The Enable threshold has typically 200mV of hysteresis to improve noise immunity.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

If the Enable pin is driven from a single ended device (such as discrete transistor) a pull-up resistor to V_{IN}, or a pull-down resistor to ground, will be required for proper operation. A 1 kΩ to 100 kΩ resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the pin should be connected to directly to the adjacent V_{IN} pin.

The status of the Enable pin also affects the behavior of the $\overline{\text{ERROR}}$ Flag. While the Enable pin is high the regulator control loop will be active and the $\overline{\text{ERROR}}$ Flag will report the status of the output voltage. When the Enable pin is taken low the regulator control loop is shutdown, the output is turned off, and the $\overline{\text{ERROR}}$ Flag pin is immediately forced low.

$\overline{\text{ERROR}}$ FLAG OPERATION

When the LP38512 Enable pin is high, the $\overline{\text{ERROR}}$ Flag pin will produce a logic low signal when the output drops by more than 15% (typical) from the nominal output voltage. The drop in output voltage may be due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The output voltage will need to rise to within 10% (typical) of the nominal output voltage for the $\overline{\text{ERROR}}$ Flag to return to a logic high state. It should also be noted that when the Enable pin is pulled low, the $\overline{\text{ERROR}}$ Flag pin is forced to be low as well.

The internal $\overline{\text{ERROR}}$ flag comparator has an open drain output stage. Hence, the $\overline{\text{ERROR}}$ pin requires an external pull-up resistor. The value of the pull-up resistor should be in the range of 10 kΩ to 1 MΩ. The $\overline{\text{ERROR}}$ Flag pin should not be pulled-up to any voltage source higher than V_{IN} as current flow through an internal parasitic diode may cause unexpected behavior. The $\overline{\text{ERROR}}$ Flag must be connected to ground if this function is not used.

The timing diagram in Figure 23 shows the relationship between the $\overline{\text{ERROR}}$ flag and the output voltage.

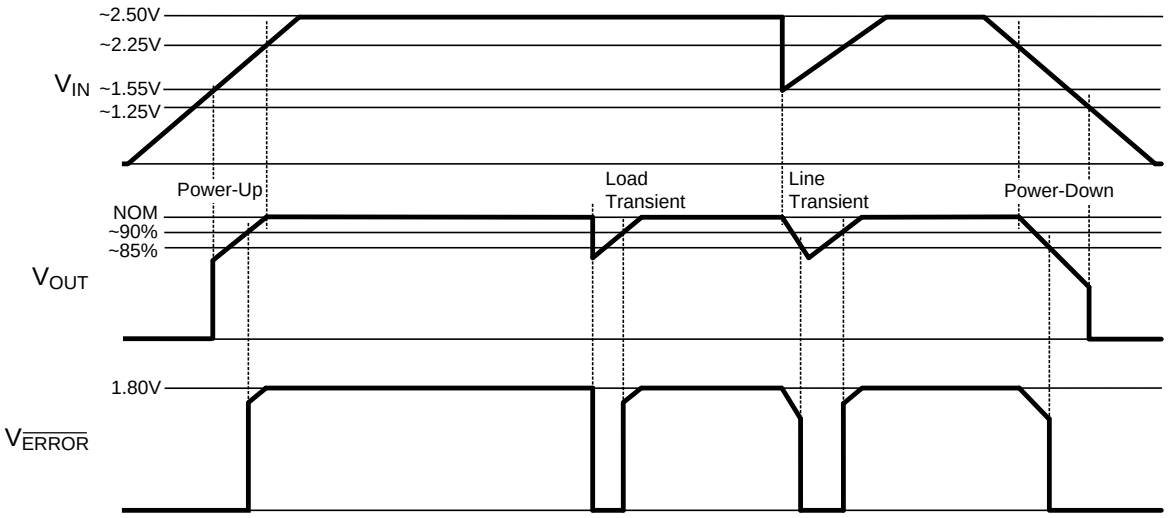


Figure 23. $\overline{\text{ERROR}}$ Flag Operation, see Typical Application

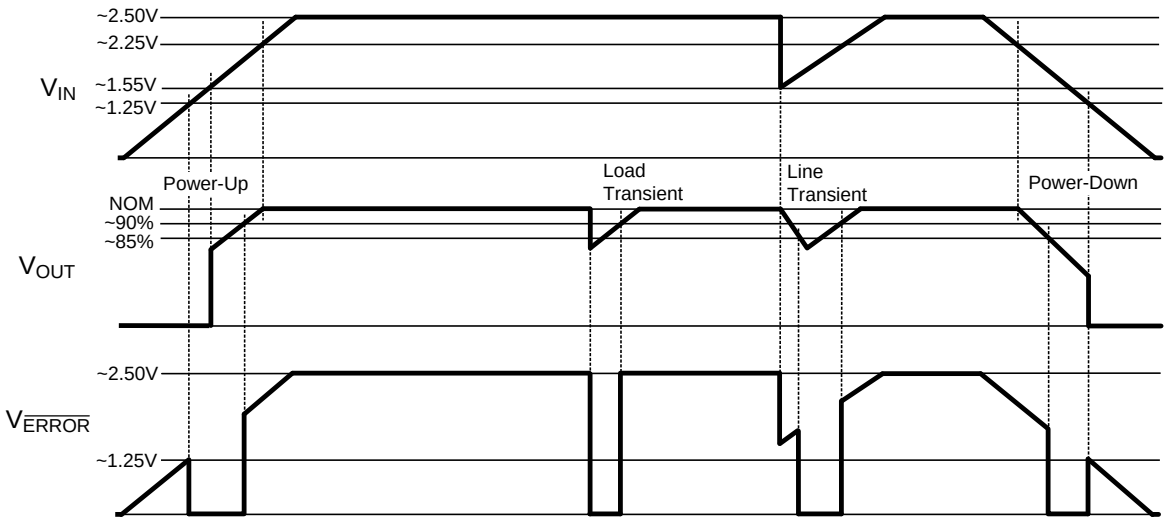


Figure 24. $\overline{\text{ERROR}}$ Flag Operation, biased from V_{IN}

POWER DISSIPATION/HEATSINKING

A heatsink may be required depending on the maximum power dissipation ($P_{D(MAX)}$), maximum ambient temperature ($T_{A(MAX)}$) of the application, and the thermal resistance (θ_{JA}) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND})$$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)}$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)}$$

HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 and the PFM packages use the copper plane on the PCB as a heatsink. The tab, or DAP, of these packages are soldered to the copper plane for heat sinking. Figure 25 shows a curve for the θ_{JA} of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

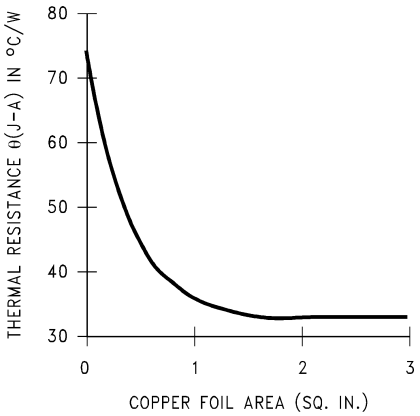


Figure 25. θ_{JA} vs Copper (1 Ounce) Area for DDPAK/TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK/TO-263 package mounted to a two-layer PCB is 32°C/W.

Figure 26 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

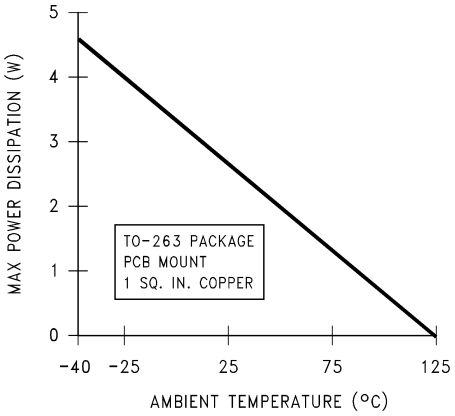


Figure 26. Maximum Power Dissipation vs Ambient Temperature for DDPAK/TO-263 Package

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38512TJ-1.8/NOPB	ACTIVE	TO-263	NDQ	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L38512TJ -1.8	Samples
LP38512TS-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38512 TS-1.8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

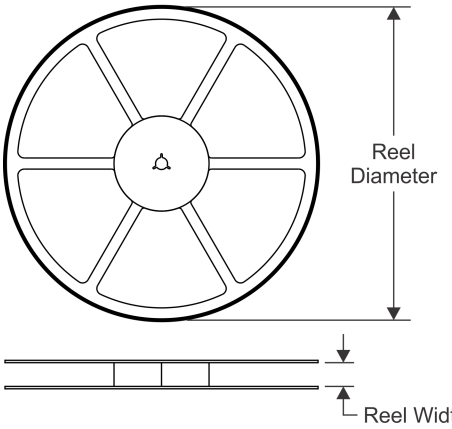
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

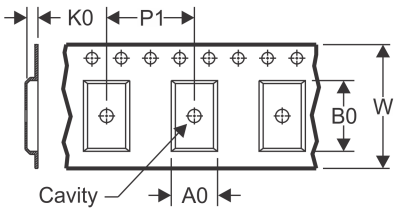
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

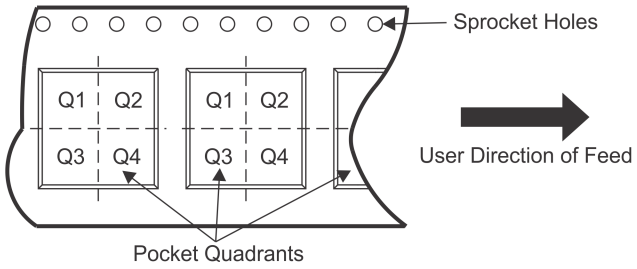


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

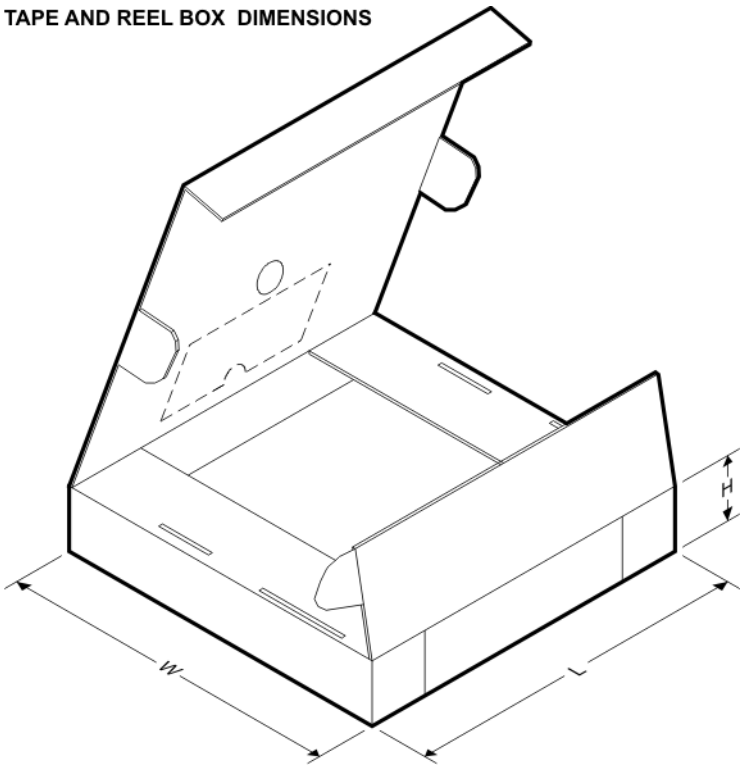
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38512TJ-1.8/NOPB	TO-263	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2

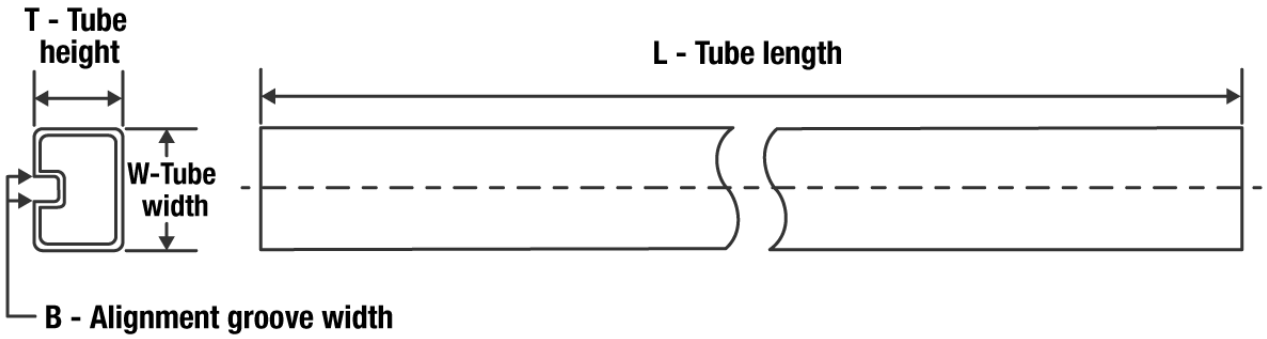
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38512TJ-1.8/NOPB	TO-263	NDQ	5	1000	367.0	367.0	35.0

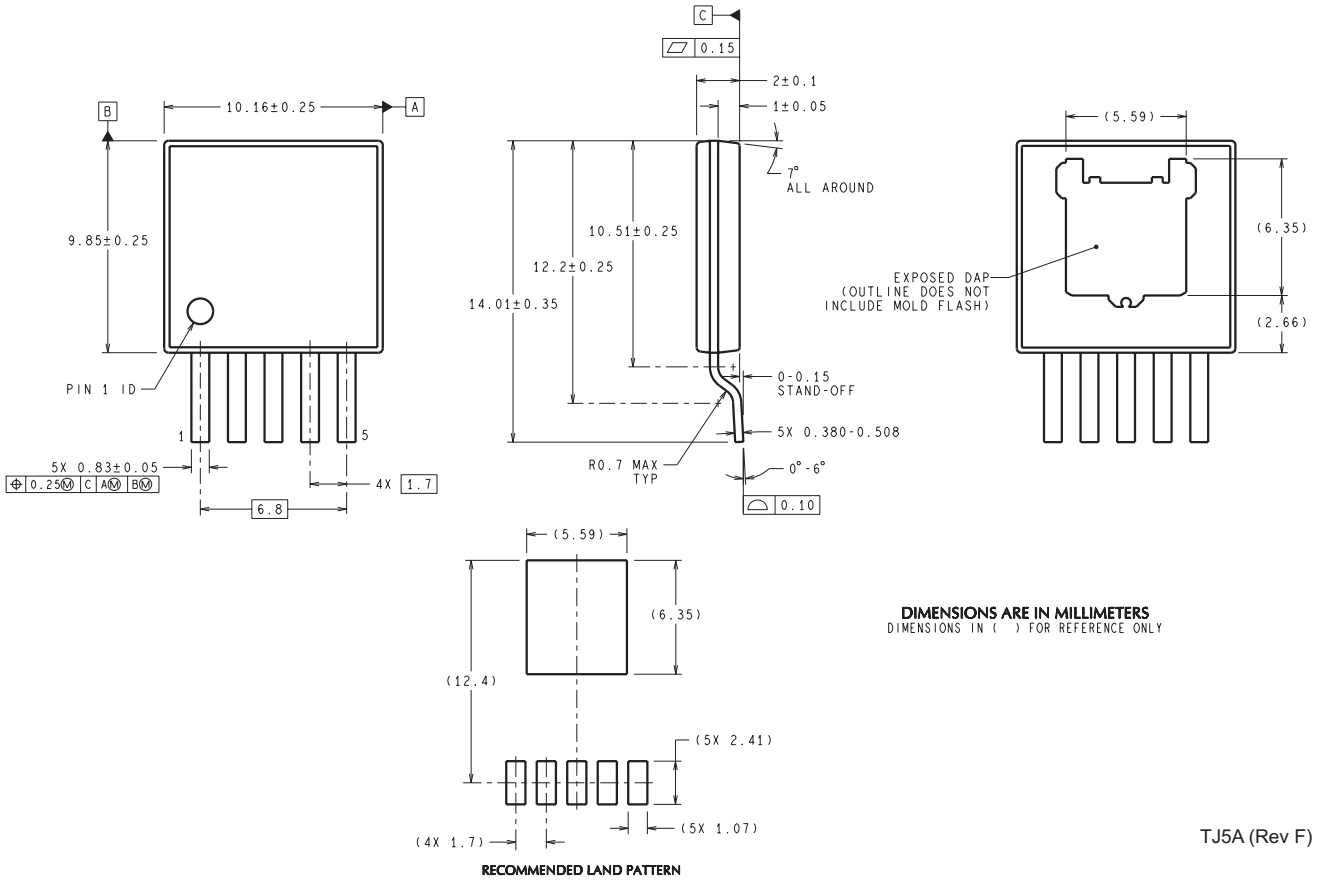
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38512TS-1.8/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19

NDQ0005A



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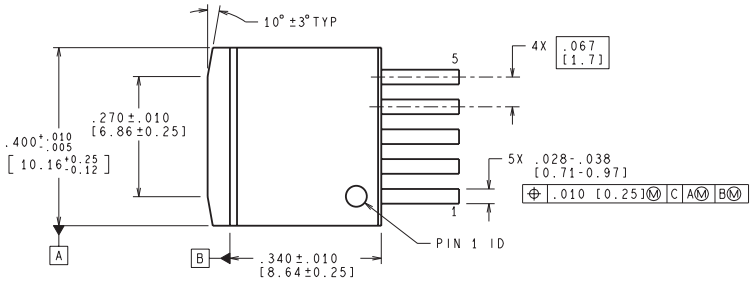
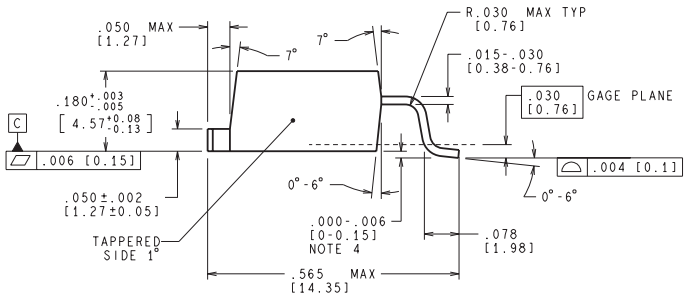
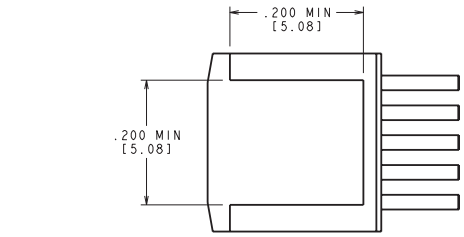
TJ5A (Rev F)

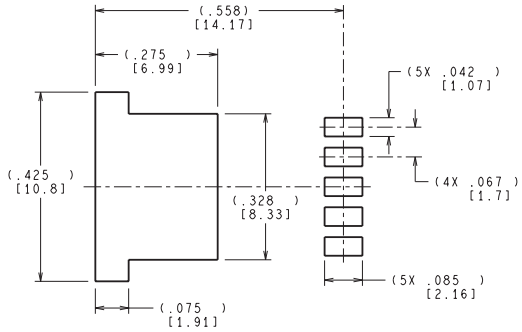
KTT0005B







BOTTOM SIDE OF PACKAGE



LAND PATTERN RECOMMENDATION

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