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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild <a href="general-regarding-numbers-n

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January 2014

FQD1N80 / FQU1N80

N-Channel QFET® MOSFET

800 V, 1.0 A, 20 Ω

Description

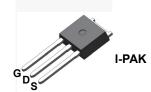
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state

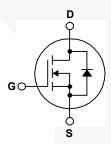
• Low Gate Charge (Typ. 5.5 nC) resistance, and to provide superior switching performance • Low Crss (Typ. 2.7 pF) and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power • 100% Avalanche Tested factor correction (PFC), and electronic lamp ballasts.

Features

- 1.0 A, 800 V, $R_{DS(on)} = 20 \Omega$ (Max.) @ $V_{GS} = 10 V$, $I_D = 0.5 A$







Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FQD1N80TM / FQU1N80TU	Unit
V _{DSS}	Drain-Source Voltage	800	V
I _D	Drain Current - Continuous (T _C = 25°C)	1.0	Α
	- Continuous (T _C = 100°C)	0.63	Α
I _{DM}	Drain Current - Pulsed (Note	1) 4.0	Α
V _{GSS}	Gate-Source Voltage	± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note	2) 90	mJ
I _{AR}	Avalanche Current (Note	1) 1.0	Α
E _{AR}	Repetitive Avalanche Energy (Note	1) 4.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note	3) 4.0	V/ns
P _D	Power Dissipation (T _A = 25°C) *	2.5	W
	Power Dissipation (T _C = 25°C)	45	W
- Derate above 25°C		0.36	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FQD1N80TM / FQU1N80TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max. 2.78		
Ъ	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max.	50	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD1N80TM	FQD1N80	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FQU1N80TU	FQU1N80	I-PAK	Tube	N/A	N/A	70 units

Parameter	Test Conditions	Min.	Тур.	Max.	Unit
aracteristics					
Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	800			V
Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		1.0		V/°C
Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V			10	μА
	V _{DS} = 640 V, T _C = 125°C			100	μA
Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	-		-100	nA
eracteristics					
	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.5 A		15.5	20	Ω
Forward Transconductance	V _{DS} = 50 V, I _D = 0.5 A	\	0.75		S
ic Characteristics					
Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		150	195	pF
Output Capacitance	f = 1.0 MHz		20	26	pF
Reverse Transfer Capacitance			2.7	3.5	pF
ing Characteristics					
ing Characteristics Turn-On Delay Time	V = 400 V L = 1 0 A		10	30	ns
	$V_{DD} = 400 \text{ V}, I_D = 1.0 \text{ A},$ $R_0 = 25 \Omega$		10 25	30	
Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 1.0 \text{ A},$ $R_G = 25 \Omega$				ns ns
Turn-On Delay Time Turn-On Rise Time			25	60	ns
Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time	R_G = 25 Ω (Note 4)		25 15	60	ns ns ns
Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time Turn-Off Fall Time	$R_G = 25 \Omega$		25 15 25	60 40 60	ns ns ns
Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time Turn-Off Fall Time Total Gate Charge Gate-Source Charge	$R_{G} = 25 \Omega$ (Note 4) $V_{DS} = 640 \text{ V}, I_{D} = 1.0 \text{ A}, V_{GS} = 10 \text{ V}$		25 15 25 5.5 1.1	60 40 60 7.2	ns ns ns n(
Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge	$R_{G} = 25~\Omega \label{eq:RG}$ (Note 4) $V_{DS} = 640~V, I_{D} = 1.0~A, \label{eq:VGS}$ (Note 4) $V_{GS} = 10~V \label{eq:KGS}$ (Note 4)		25 15 25 5.5 1.1 3.3	60 40 60 7.2 	ns ns ns nC nC
Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics ar Maximum Continuous Drain-Source Dio	$R_G = 25 \Omega$ (Note 4) $V_{DS} = 640 \text{ V}, I_D = 1.0 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 4) And Maximum Ratings and Forward Current		25 15 25 5.5 1.1 3.3	60 40 60 7.2 	ns ns ns nC nC
Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics ar Maximum Continuous Drain-Source Diode Fallows Turn-Onder Fallows Time Maximum Pulsed Drain-Source Diode Fallows Time Turn-On Delay Time Turn-On Rise Time Turn-O	$R_G = 25 \Omega$ (Note 4) $V_{DS} = 640 \text{ V}, I_D = 1.0 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 4) and Maximum Ratings of Forward Current Forward Current		25 15 25 5.5 1.1 3.3	60 40 60 7.2 1.0 4.0	ns ns nc nC nC
Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics ar Maximum Continuous Drain-Source Dio	$R_G = 25 \Omega$ (Note 4) $V_{DS} = 640 \text{ V}, I_D = 1.0 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 4) And Maximum Ratings and Forward Current		25 15 25 5.5 1.1 3.3	60 40 60 7.2 	ns ns ns nC nC
	Drain-Source Breakdown Voltage Breakdown Voltage Temperature Coefficient Zero Gate Voltage Drain Current Gate-Body Leakage Current, Forward Gate-Body Leakage Current, Reverse Aracteristics Gate Threshold Voltage Static Drain-Source On-Resistance Forward Transconductance ic Characteristics Input Capacitance	Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}$, $I_D = 250 \text{ μA}$ Breakdown Voltage Temperature Coefficient $I_D = 250 \text{ μA}$, Referenced to 25° CZero Gate Voltage Drain Current $V_{DS} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$ Gate-Body Leakage Current, Forward Gate-Body Leakage Current, Reverse $V_{GS} = 30 \text{ V}$, $V_{DS} = 0 \text{ V}$ Bracteristics $V_{DS} = V_{GS}$, $V_{DS} = 0 \text{ V}$ Gate Threshold Voltage $V_{DS} = V_{GS}$, $V_{DS} = 0 \text{ V}$ Static Drain-Source On-Resistance $V_{DS} = 10 \text{ V}$, $V_{DS} = 0.5 \text{ A}$ Forward Transconductance $V_{DS} = 50 \text{ V}$, $V_{DS} = 0.5 \text{ A}$ Input Capacitance $V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $V_{CS} = 0 $	Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}$, $I_D = 250 \text{ μA}$ 800Breakdown Voltage Temperature Coefficient $I_D = 250 \text{ μA}$, Referenced to 25°C Zero Gate Voltage Drain Current $V_{DS} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$ Gate-Body Leakage Current, Forward Gate-Body Leakage Current, Reverse $V_{GS} = 30 \text{ V}$, $V_{DS} = 0 \text{ V}$ Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250 \text{ μA}$ 3.0Static Drain-Source On-Resistance $V_{CS} = 10 \text{ V}$, $V_{CS} = 0.5 \text{ A}$ Forward Transconductance $V_{DS} = 50 \text{ V}$, $I_D = 0.5 \text{ A}$ ic Characteristics $V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $V_{CS} = 0 \text{ V}$, $V_$	Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}$, $I_D = 250 \text{ μA}$ 800Breakdown Voltage Temperature Coefficient $I_D = 250 \text{ μA}$, Referenced to 25°C 1.0Zero Gate Voltage Drain Current $V_{DS} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$ Gate-Body Leakage Current, Forward $V_{GS} = 30 \text{ V}$, $V_{DS} = 0 \text{ V}$ Gate-Body Leakage Current, Reverse $V_{GS} = -30 \text{ V}$, $V_{DS} = 0 \text{ V}$ aracteristicsStatic Drain-Source $V_{DS} = V_{GS}$, $I_D = 250 \text{ μA}$ 3.0Static Drain-Source On-Resistance $V_{DS} = 10 \text{ V}$, $I_D = 0.5 \text{ A}$ 15.5Forward Transconductance $V_{DS} = 50 \text{ V}$, $I_D = 0.5 \text{ A}$ 0.75ic CharacteristicsInput Capacitance $V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $V_{CS} = 0$	Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}$, $I_D = 250 \text{ μA}$ 800 Breakdown Voltage Temperature Coefficient $I_D = 250 \text{ μA}$, Referenced to 25°C 1.0 Zero Gate Voltage Drain Current $V_{DS} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$ 10 Gate-Body Leakage Current, Forward $V_{GS} = 30 \text{ V}$, $V_{DS} = 0 \text{ V}$ 100 Gate-Body Leakage Current, Forward $V_{GS} = 30 \text{ V}$, $V_{DS} = 0 \text{ V}$ 100 Gate-Body Leakage Current, Reverse $V_{GS} = -30 \text{ V}$, $V_{DS} = 0 \text{ V}$ -100 Aracteristics Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250 \text{ μA}$ 3.0 5.0 Static Drain-Source On-Resistance $V_{GS} = 10 \text{ V}$, $I_D = 0.5 \text{ A}$ 15.5 20 Forward Transconductance $V_{DS} = 50 \text{ V}$, $I_D = 0.5 \text{ A}$ 0.75 Input Capacitance $V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $V_{CS} = $

Notes: 1. Repetitive rating : pulse-width limited by maximum junction temperature. 2. L = 170 mH, I_{AS} = 1.0 A, V_{DD} = 50 V, R_{G} = 25 Ω , starting T_{J} = 25°C. 3. $I_{SD} \le$ 1.0 A, di/dt \le 200 A/ μ s, $V_{DD} \le$ BV $_{DSS}$, starting T_{J} = 25°C. 4. Essentially independent of operating temperature.

Typical Characteristics

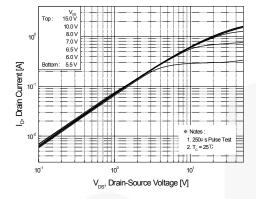


Figure 1. On-Region Characteristics

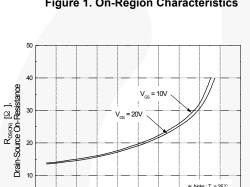


Figure 3. On-Resistance Variation vs. **Drain Current and Gate Voltage**

1.2 ${\rm I_{\scriptscriptstyle D}}$, Drain Current [A] 1.6 1.8

0.8 1.0

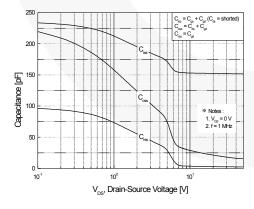


Figure 5. Capacitance Characteristics

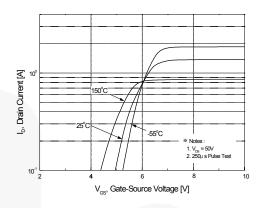


Figure 2. Transfer Characteristics

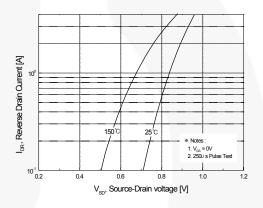


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

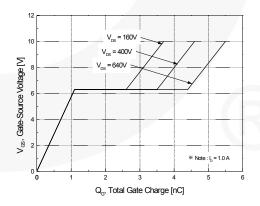


Figure 6. Gate Charge Characteristics

1.2 (Nomelized) BV LSS (Momelized) 1.0 (Nomelized) 1.0 (Notes: 1.1 (Notes: 1.2 (Notes: 2.2 (Notes:

Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

T_,, Junction Temperature [°C]

150

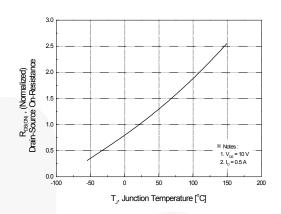


Figure 8. On-Resistance Variation vs. Temperature

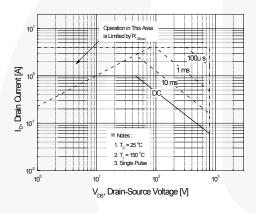


Figure 9. Maximum Safe Operating Area

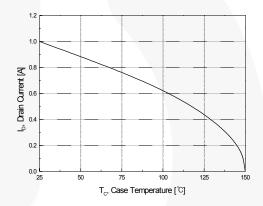


Figure 10. Maximum Drain Current vs. Case Temperature

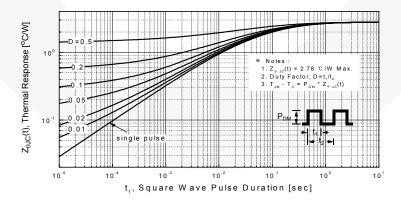


Figure 11. Transient Thermal Response Curve

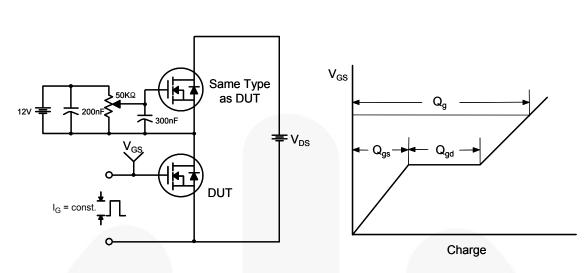


Figure 12. Gate Charge Test Circuit & Waveform

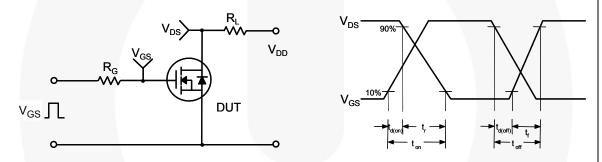


Figure 13. Resistive Switching Test Circuit & Waveforms

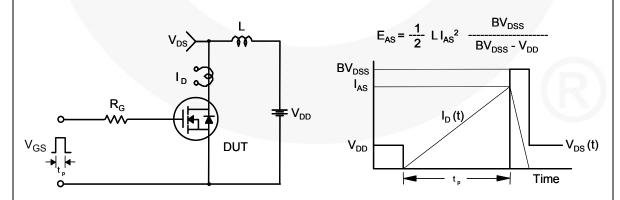
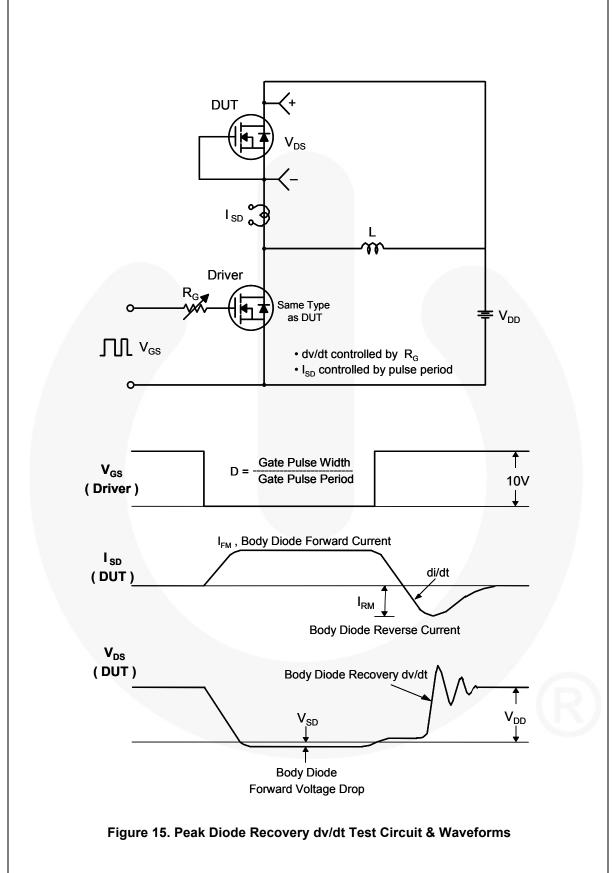


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions -5.55 MIN→ 1.27 6.22 5.97 6.50 MIN -1.02 MAX Ċ 2 (0.59)0.89 2.29 2.28 ⊕ 0.25 A A C 4.57 LAND PATTERN RECOMMENDATION 2.39 SEE 2.18 4.32 MIN NOTE D 0.58 0.45 5.21 MIN 10.41 9.40 SEE DETAIL A △ 0.10 B 0.51 GAGE PLANE NOTES: UNLESS OTHERWISE SPECIFIED THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA. ALL DIMENSIONS ARE IN MILLIMETERS. 10 (1.54)DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009. SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION. PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL. .78 0.127 MAX DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS. SEATING PLANE (2.90)LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD DETAIL TO228P991X239-3N. (ROTATED -90°) SCALE: 12X DRAWING NUMBER AND REVISION: MKT-T0252A03REV9. FAIRCHILD SEMICONDUCTOR.

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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Mechanical Dimensions C 9.65 8.90 (0.60) -2.29 ◆ 0.25M AM C 3 PLCS NOTES: UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN MILLIMETERS. THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988. B) DIMENSIONING AND TOLERANCING PER TO251A03REVA ASME Y14.5M-1994.

Figure 17. TO251 (I-PAK), Molded, 3-Lead

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Advance Information Formative / In Design		Datasheet contains the design specifications for product development. Specificati may change in any manner without notice.	
Preliminary First Production		Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.	
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