

## SN74LVC245A Octal Bus Transceiver With 3-State Outputs

### 1 Features

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode and Back Drive protection
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

### 2 Applications

- Cable Modem Termination Systems
- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

### 3 Description

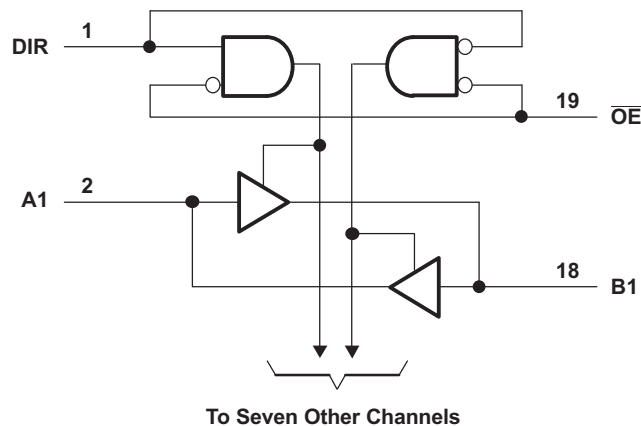
These octal bus transceivers are designed for 1.65-V to 3.6-V  $V_{CC}$  operation. The 'LVC245A devices are designed for asynchronous communication between data buses.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE (PIN) | BODY SIZE          |
|-------------|---------------|--------------------|
| SN74LVC245A | VQFN (20)     | 4.50 mm x 3.50 mm  |
|             | SSOP (20)     | 7.50 mm x 5.30 mm  |
|             | TSSOP (20)    | 6.50 mm x 4.40 mm  |
|             | TVSOP (20)    | 5.00 mm x 4.40 mm  |
|             | SOIC (20)     | 12.80 mm x 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.



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## 5 Revision History

### Changes from Revision W (May 2013) to Revision X

**Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**
- Deleted *Ordering Information* table. .... **1**

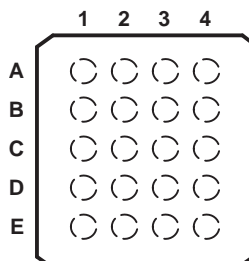
### Changes from Revision V (September 2010) to Revision W

**Page**

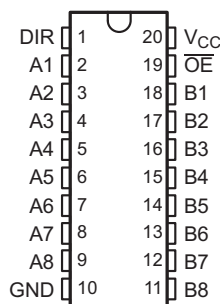
- Added –40°C to 125°C temperature specification to *Recommended Operating Conditions* table. .... **5**

## 6 Pin Configuration and Functions

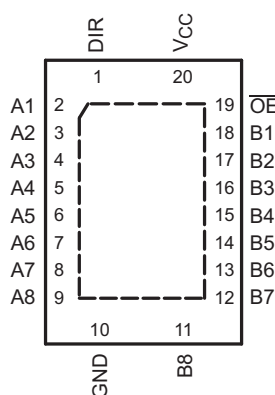
**GQN OR ZQN PACKAGE  
(TOP VIEW)**



**DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)**



**RGY PACKAGE  
(TOP VIEW)**



### Pin Functions

| NAME            | PIN                          |            | TYPE | DESCRIPTION                                                                                                   |
|-----------------|------------------------------|------------|------|---------------------------------------------------------------------------------------------------------------|
|                 | DB, DGV, DW, NS, PW, and RGY | GQN or ZQN |      |                                                                                                               |
| A1              | 2                            | A1         | I/O  | Transceiver I/O pin                                                                                           |
| A2              | 3                            | B3         | I/O  | Transceiver I/O pin                                                                                           |
| A3              | 4                            | B1         | I/O  | Transceiver I/O pin                                                                                           |
| A4              | 5                            | C2         | I/O  | Transceiver I/O pin                                                                                           |
| A5              | 6                            | C1         | I/O  | Transceiver I/O pin                                                                                           |
| A6              | 7                            | D3         | I/O  | Transceiver I/O pin                                                                                           |
| A7              | 8                            | D1         | I/O  | Transceiver I/O pin                                                                                           |
| A8              | 9                            | E2         | I/O  | Transceiver I/O pin                                                                                           |
| B1              | 18                           | B4         | I/O  | Transceiver I/O pin                                                                                           |
| B2              | 17                           | B2         | I/O  | Transceiver I/O pin                                                                                           |
| B3              | 16                           | C4         | I/O  | Transceiver I/O pin                                                                                           |
| B4              | 15                           | C3         | I/O  | Transceiver I/O pin                                                                                           |
| B5              | 14                           | D4         | I/O  | Transceiver I/O pin                                                                                           |
| B6              | 13                           | D2         | I/O  | Transceiver I/O pin                                                                                           |
| B7              | 12                           | E4         | I/O  | Transceiver I/O pin                                                                                           |
| B8              | 11                           | E3         | I/O  | Transceiver I/O pin                                                                                           |
| DIR             | 1                            | A2         | I    | Direction control. When high, the signal propagates from A to B. When low, the signal propagates from B to A. |
| $\overline{OE}$ | 19                           | A4         | I    | Output enable                                                                                                 |
| GND             | 10                           | E1         | —    | Ground                                                                                                        |
| V <sub>CC</sub> | 20                           | A3         | —    | Power pin                                                                                                     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                                                             | MIN                | MAX                   | UNIT    |
|------------------|---------------------------------------------------------------------------------------------|--------------------|-----------------------|---------|
| V <sub>CC</sub>  | Supply voltage range                                                                        | -0.5               | 6.5                   | V       |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                                                          | -0.5               | 6.5                   | V       |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5               | 6.5                   | V       |
| V <sub>O</sub>   | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              | -0.5               | V <sub>CC</sub> + 0.5 | V       |
| I <sub>IK</sub>  | Input clamp current                                                                         | V <sub>I</sub> < 0 |                       | -50 mA  |
| I <sub>OK</sub>  | Output clamp current                                                                        | V <sub>O</sub> < 0 |                       | -50 mA  |
| I <sub>O</sub>   | Continuous output current                                                                   |                    |                       | ±50 mA  |
|                  | Continuous current through V <sub>CC</sub> or GND                                           |                    |                       | ±100 mA |
| T <sub>stg</sub> | Storage temperature range                                                                   | -65                | 150                   | °C      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 7.2 ESD Ratings

| PARAMETER          | DEFINITION              | VALUE                                                                                    | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 2000 |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    |                                    | T <sub>A</sub> = 25°C  |     | –40°C TO 85°C          |     | –40°C TO 125°C         |      | UNIT |
|-----------------|------------------------------------|------------------------------------|------------------------|-----|------------------------|-----|------------------------|------|------|
|                 |                                    |                                    | MIN                    | MAX | MIN                    | MAX | MIN                    | MAX  |      |
| V <sub>CC</sub> | Supply voltage                     | Operating                          | 1.65                   | 3.6 | 1.65                   | 3.6 | 1.65                   | 3.6  | V    |
|                 |                                    | Data retention only                | 1.5                    |     | 1.5                    |     | 1.5                    |      |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> |     | 0.65 × V <sub>CC</sub> |     | 0.65 × V <sub>CC</sub> |      | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |     | 1.7                    |     | 1.7                    |      |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2                      |     | 2                      |     | 2                      |      |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.35 × V <sub>CC</sub> |     | 0.35 × V <sub>CC</sub> |     | 0.35 × V <sub>CC</sub> |      | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 0.7                    |     | 0.7                    |     | 0.7                    |      |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 0.8                    |     | 0.8                    |     | 0.8                    |      |      |
| V <sub>I</sub>  | Input voltage                      | 0                                  | 5.5                    | 0   | 5.5                    | 0   | 5.5                    | V    |      |
| V <sub>O</sub>  | Output voltage                     | 0                                  | V <sub>CC</sub>        | 0   | V <sub>CC</sub>        | 0   | V <sub>CC</sub>        | V    |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V           | –4                     |     | –4                     |     | –4                     |      | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | –8                     |     | –8                     |     | –8                     |      |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | –12                    |     | –12                    |     | –12                    |      |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | –24                    |     | –24                    |     | –24                    |      |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V           | 4                      |     | 4                      |     | 4                      |      | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | 8                      |     | 8                      |     | 8                      |      |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | 12                     |     | 12                     |     | 12                     |      |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | 24                     |     | 24                     |     | 24                     |      |      |
| Δt/Δv           | Input transition rise or fall rate |                                    | 10                     |     | 10                     |     | 10                     | ns/V |      |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | SN74LVC245A                                  |                    |                   |                           |                  |                   |                   |                    | UNIT |          |
|-------------------------------|----------------------------------------------|--------------------|-------------------|---------------------------|------------------|-------------------|-------------------|--------------------|------|----------|
|                               | DB <sup>(2)</sup>                            | DGV <sup>(2)</sup> | DW <sup>(2)</sup> | GQN or ZQN <sup>(2)</sup> | N <sup>(2)</sup> | NS <sup>(2)</sup> | PW <sup>(2)</sup> | RGY <sup>(3)</sup> |      |          |
|                               | 20 PINS                                      |                    |                   |                           |                  |                   |                   |                    |      |          |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 106.5              | 124.1             | 92.9                      | 78               | 59.2              | 83.6              | 108.1              | 44.0 | °C/<br>W |
| R <sub>θJC(top)</sub>         | Junction-to-case(top) thermal resistance     | 68.1               | 39.5              | 60.6                      |                  | 44.9              | 49.4              | 43.0               | 53.0 |          |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 61.7               | 65.5              | 60.4                      |                  | 40.1              | 51.2              | 59.1               | 22.1 |          |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 28.5               | 2.1               | 28.2                      |                  | 29.9              | 21.9              | 4.7                | 3.0  |          |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 61.2               | 64.9              | 60.0                      |                  | 39.9              | 50.8              | 58.6               | 22.2 |          |
| R <sub>θJC(bottom)</sub>      | Junction-to-case(bottom) thermal resistance  | —                  | —                 | —                         |                  | —                 | —                 | —                  | 16.6 |          |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

(3) The package thermal impedance is calculated in accordance with JESD 51-5.

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      | TEST CONDITIONS                                                                 | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | –40°C TO 85°C         |     | –40°C TO 125°C        |     | UNIT |
|--------------------------------|---------------------------------------------------------------------------------|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|-----|------|
|                                |                                                                                 |                 | MIN                   | TYP | MAX | MIN                   | MAX | MIN                   | MAX |      |
| V <sub>OH</sub>                | I <sub>OH</sub> = –100 μA                                                       | 1.65 V to 3.6 V | V <sub>CC</sub> – 0.2 |     |     | V <sub>CC</sub> – 0.2 |     | V <sub>CC</sub> – 0.2 |     | V    |
|                                | I <sub>OH</sub> = –4 mA                                                         | 1.65 V          | 1.29                  |     |     | 1.2                   |     | 1.1                   |     |      |
|                                | I <sub>OH</sub> = –8 mA                                                         | 2.3 V           | 1.9                   |     |     | 1.7                   |     | 1.6                   |     |      |
|                                | I <sub>OH</sub> = –12 mA                                                        | 2.7 V           | 2.2                   |     |     | 2.2                   |     | 2.1                   |     |      |
|                                |                                                                                 | 3 V             | 2.4                   |     |     | 2.4                   |     | 2.3                   |     |      |
| I <sub>OH</sub> = –24 mA       | 3 V                                                                             | 2.3             |                       |     | 2.2 |                       | 2.1 |                       |     |      |
| V <sub>OL</sub>                | I <sub>OL</sub> = 100 μA                                                        | 1.65 V to 3.6 V | 0.1                   |     |     | 0.2                   |     | 0.2                   |     | V    |
|                                | I <sub>OL</sub> = 4 mA                                                          | 1.65 V          | 0.24                  |     |     | 0.45                  |     | 0.60                  |     |      |
|                                | I <sub>OL</sub> = 8 mA                                                          | 2.3 V           | 0.3                   |     |     | 0.7                   |     | 0.75                  |     |      |
|                                | I <sub>OL</sub> = 12 mA                                                         | 2.7 V           | 0.4                   |     |     | 0.4                   |     | 0.6                   |     |      |
|                                | I <sub>OL</sub> = 24 mA                                                         | 3 V             | 0.55                  |     |     | 0.55                  |     | 0.75                  |     |      |
| I <sub>I</sub>                 | Control inputs<br>V <sub>I</sub> = 0 to 5.5 V                                   | 3.6 V           | ±1                    |     |     | ±5                    |     | ±10                   |     | μA   |
| I <sub>off</sub>               | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                        | 0               | ±1                    |     |     | ±10                   |     | ±20                   |     | μA   |
| I <sub>OZ</sub> <sup>(1)</sup> | V <sub>O</sub> = 0 to 5.5 V                                                     | 3.6 V           | ±1                    |     |     | ±10                   |     | ±20                   |     | μA   |
| I <sub>CC</sub>                | V <sub>I</sub> = V <sub>CC</sub> or GND                                         | 3.6 V           | 1                     |     |     | 10                    |     | 30                    |     | μA   |
|                                | 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>                                   |                 | 1                     |     |     | 10                    |     | 30                    |     |      |
| ΔI <sub>CC</sub>               | One input at V <sub>CC</sub> – 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  | 500                   |     |     | 500                   |     | 5000                  |     | μA   |
| C <sub>i</sub>                 | Control inputs<br>V <sub>I</sub> = V <sub>CC</sub> or GND                       | 3.3 V           | 4                     |     |     |                       |     |                       |     | pF   |
| C <sub>io</sub>                | A or B ports <sup>(3)</sup><br>V <sub>I</sub> = V <sub>CC</sub> or GND          | 3.3 V           | 5.5                   |     |     |                       |     |                       |     | pF   |

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25 C.

(2) This applies in the disabled state only.

 (3) For I/O ports, the parameter I<sub>oz</sub> includes the input leakage current.

## 7.6 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

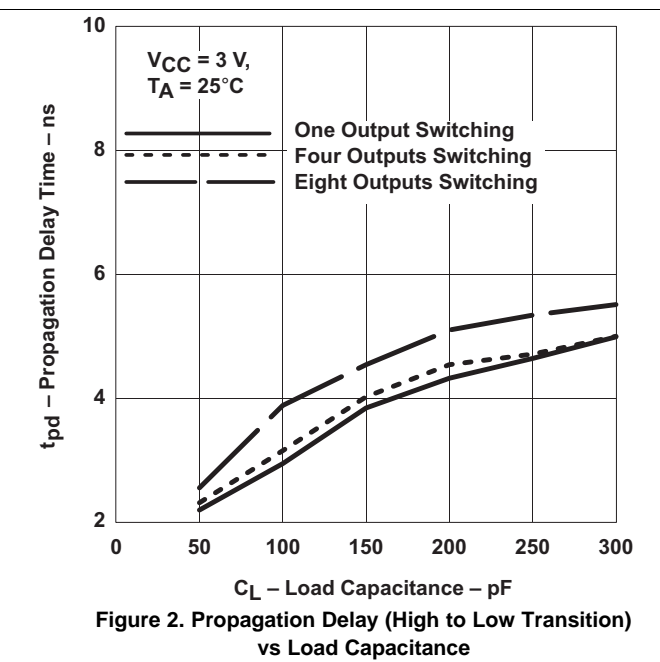
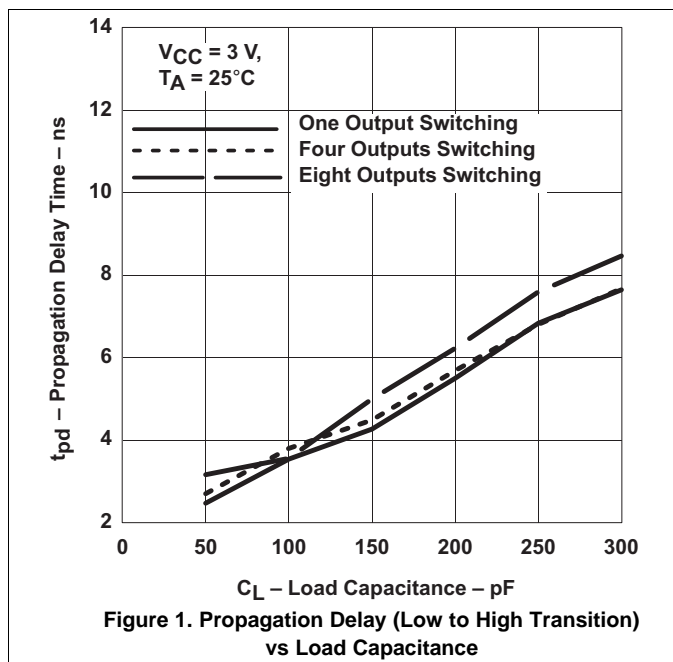
| PARAMETER          | FROM (INPUT)    | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | –40°C TO 85°C |      | –40°C TO 125°C |      | UNIT |
|--------------------|-----------------|-------------|-----------------|-----------------------|-----|------|---------------|------|----------------|------|------|
|                    |                 |             |                 | MIN                   | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |      |
| t <sub>pd</sub>    | A or B          | B or A      | 1.8 V ± 0.15 V  | 1                     | 6   | 12.2 | 1             | 12.7 | 1              | 13.7 | ns   |
|                    |                 |             | 2.5 V ± 0.2 V   | 1                     | 3.9 | 7.8  | 1             | 8.3  | 1              | 9.1  |      |
|                    |                 |             | 2.7 V           | 1                     | 4.2 | 7.1  | 1             | 7.3  | 1              | 8.3  |      |
|                    |                 |             | 3.3 V ± 0.3 V   | 1.5                   | 3.8 | 6.1  | 1.5           | 6.3  | 1.5            | 7.3  |      |
| t <sub>en</sub>    | $\overline{OE}$ | A or B      | 1.8 V ± 0.15 V  | 1                     | 7   | 14.8 | 1             | 15.3 | 1              | 16.8 | ns   |
|                    |                 |             | 2.5 V ± 0.2 V   | 1                     | 4.5 | 10   | 1             | 10.5 | 1              | 12   |      |
|                    |                 |             | 2.7 V           | 1                     | 5.4 | 9.3  | 1             | 9.5  | 1              | 11   |      |
|                    |                 |             | 3.3 V ± 0.3 V   | 1.5                   | 4.4 | 8.3  | 1.5           | 8.5  | 1.5            | 10   |      |
| t <sub>dis</sub>   | $\overline{OE}$ | A or B      | 1.8 V ± 0.15 V  | 1                     | 7.8 | 16.5 | 1             | 17   | 1              | 18   | ns   |
|                    |                 |             | 2.5 V ± 0.2 V   | 1                     | 4   | 9    | 1             | 9.5  | 1              | 10.5 |      |
|                    |                 |             | 2.7 V           | 1                     | 4.4 | 8.3  | 1             | 8.5  | 1              | 9.5  |      |
|                    |                 |             | 3.3 V ± 0.3 V   | 1.7                   | 4.1 | 7.3  | 1.7           | 7.5  | 1.7            | 8.5  |      |
| t <sub>sk(o)</sub> |                 |             | 3.3 V ± 0.3 V   |                       |     |      | 1             |      | 1.5            | ns   |      |

### 7.7 Operating Characteristics

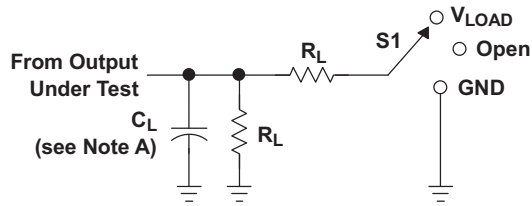
T<sub>A</sub> = 25°C

| PARAMETER       |                                               | TEST CONDITIONS | V <sub>CC</sub>  | TYP   | UNIT |    |
|-----------------|-----------------------------------------------|-----------------|------------------|-------|------|----|
| C <sub>pd</sub> | Power dissipation capacitance per transceiver | f = 10 MHz      | Outputs enabled  | 1.8 V | 42   | pF |
|                 |                                               |                 |                  | 2.5 V | 43   |    |
|                 |                                               |                 | 3.3 V            | 45    |      |    |
|                 |                                               |                 | Outputs disabled | 1.8 V | 1    |    |
|                 |                                               |                 |                  | 2.5 V | 1    |    |
|                 |                                               |                 |                  | 3.3 V | 2    |    |

### 7.8 Typical Characteristics

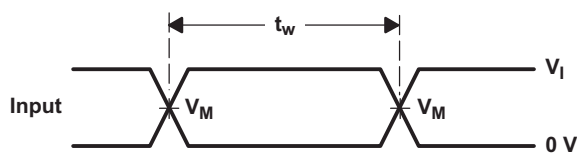
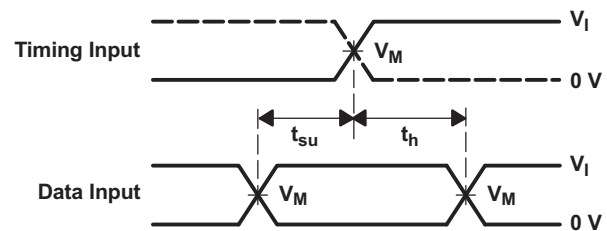
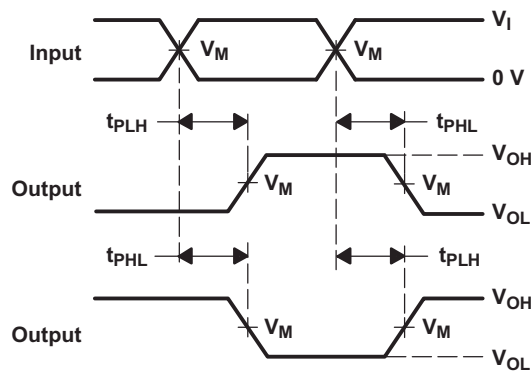
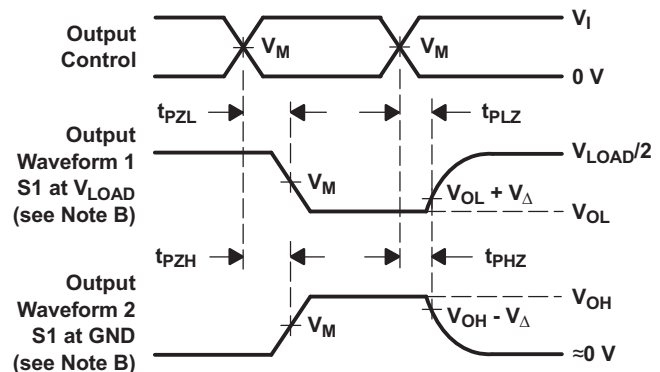


## 8 Parameter Measurement Information


**LOAD CIRCUIT**

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |


**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**



## 9 Detailed Description

### 9.1 Overview

This octal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

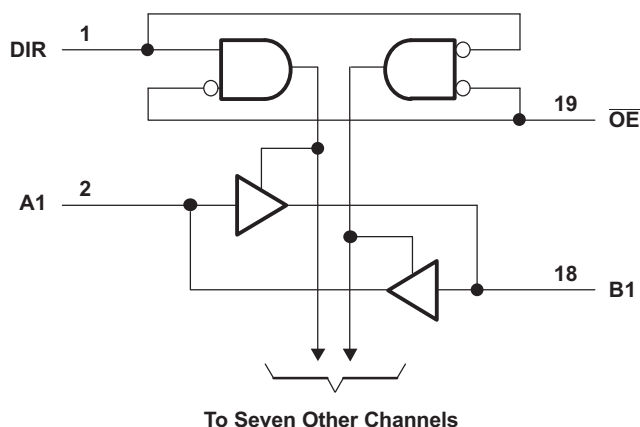
The SN74LVC245A device is designed for asynchronous communication between data buses. This device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses effectively are isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 9.2 Functional Block Diagram



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

### 9.3 Feature Description

- Allows down voltage translation
  - 5 V to 3.3 V
  - 5 V or 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V

### 9.4 Device Functional Modes

Table 1. Function Table

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |

## 10 Application and Implementation

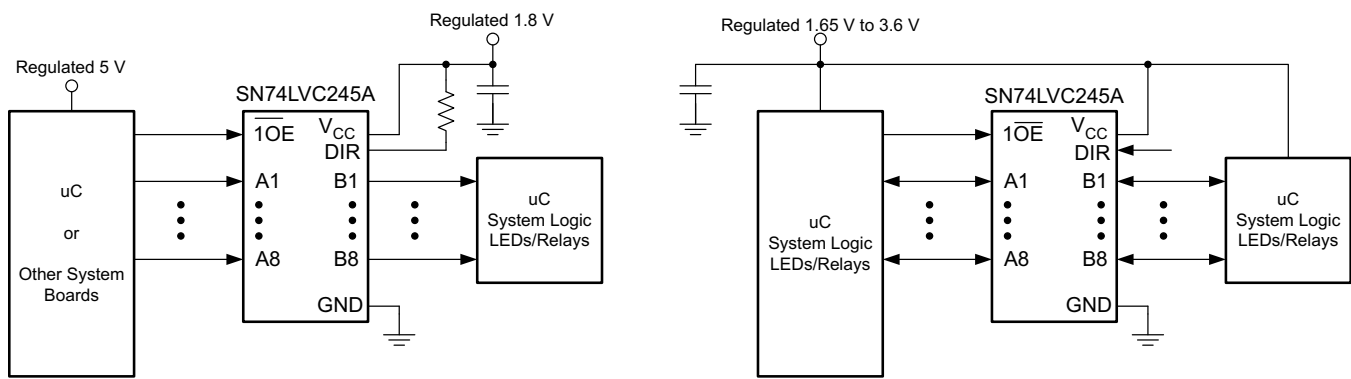
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

SN74LVC245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making it ideal for down translation.

### 10.2 Typical Application



**Figure 4. Typical Application Schematic**

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

##### 1. Recommended Input Conditions

- For rise time and fall time specifications, see  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
- For specified high and low levels, see  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .

##### 2. Recommend Output Conditions

- Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves

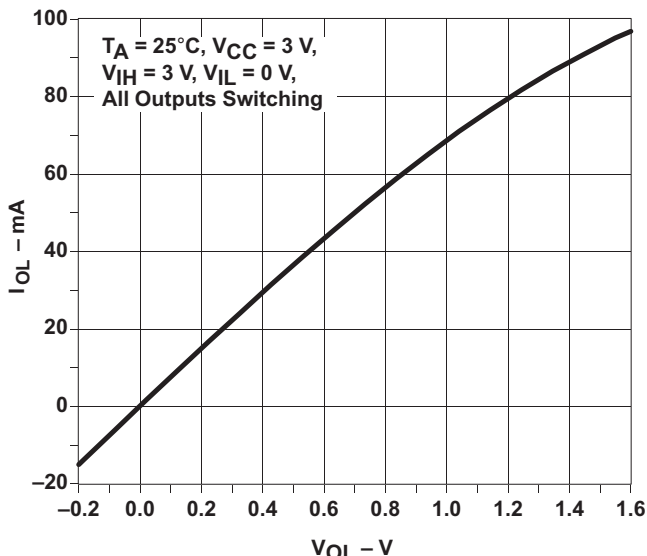


Figure 5. Output Drive Current ( $I_{OL}$ ) vs LOW-level Output Voltage ( $V_{OL}$ )

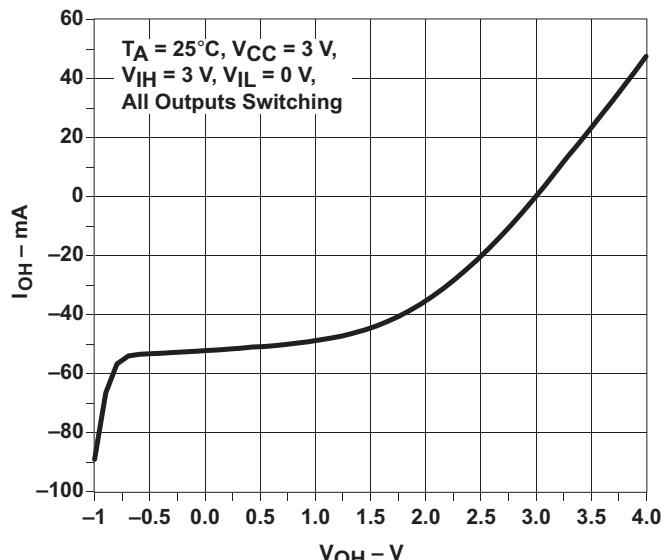


Figure 6. Output Drive Current ( $I_{OH}$ ) vs HIGH-level Output Voltage ( $V_{OH}$ )

## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1  $\mu\text{F}$  capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

### 12.2 Layout Example

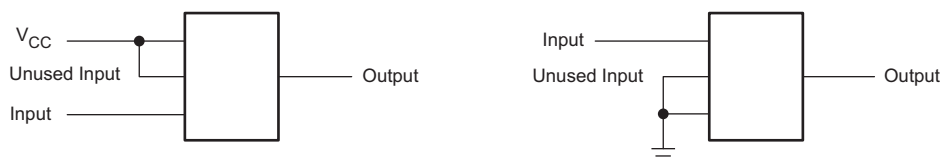


Figure 7. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Trademarks

All trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.



This glossary lists and explains terms, acronyms and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC245ADBR   | ACTIVE        | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245ADBRE4 | ACTIVE        | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245ADBRG4 | ACTIVE        | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245ADGVR  | ACTIVE        | TVSOP        | DGV             | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245ADW    | ACTIVE        | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LVC245A                 | <a href="#">Samples</a> |
| SN74LVC245ADWR   | ACTIVE        | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LVC245A                 | <a href="#">Samples</a> |
| SN74LVC245ADWRG4 | ACTIVE        | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LVC245A                 | <a href="#">Samples</a> |
| SN74LVC245AN     | ACTIVE        | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | NIPDAU                  | N / A for Pkg Type   | -40 to 125   | SN74LVC245AN            | <a href="#">Samples</a> |
| SN74LVC245ANE4   | ACTIVE        | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | NIPDAU                  | N / A for Pkg Type   | -40 to 125   | SN74LVC245AN            | <a href="#">Samples</a> |
| SN74LVC245ANSR   | ACTIVE        | SO           | NS              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LVC245A                 | <a href="#">Samples</a> |
| SN74LVC245APW    | ACTIVE        | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245APWE4  | ACTIVE        | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245APWG4  | ACTIVE        | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245APWR   | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU   SN             | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245APWRE4 | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245APWRG3 | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | SN                      | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |
| SN74LVC245APWRG4 | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type               | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                                                                             |
|------------------|---------------|----------------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------------------------------------------------------------------|
| SN74LVC245APWT   | ACTIVE        | TSSOP                      | PW              | 20   | 250         | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  |  |
| SN74LVC245ARGYR  | ACTIVE        | VQFN                       | RGY             | 20   | 3000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | LC245A                  |  |
| SN74LVC245AZQNR  | LIFEBUY       | BGA<br>MICROSTAR<br>JUNIOR | ZQN             | 20   | 1000        | Green (RoHS & no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | LC245A                  |                                                                                     |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC245A :**

- Enhanced Product: [SN74LVC245A-EP](#)

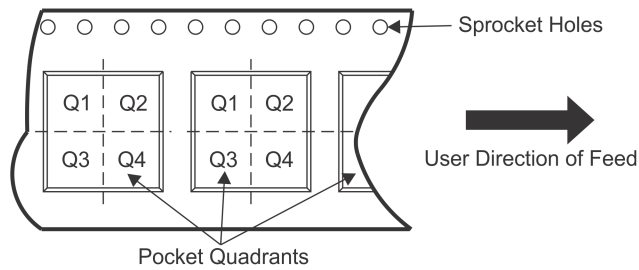
## NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device           | Package Type         | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC245ADBR   | SSOP                 | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC245ADGVR  | TVSOP                | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC245ADWR   | SOIC                 | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVC245ANSR   | SO                   | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LVC245APWR   | TSSOP                | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVC245APWRG3 | TSSOP                | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVC245APWRG4 | TSSOP                | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LVC245APWT   | TSSOP                | PW              | 20   | 250  | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVC245ARGYR  | VQFN                 | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC245AZQNR  | BGA MICROSTAR JUNIOR | ZQN             | 20   | 1000 | 330.0              | 12.4               | 3.3     | 4.3     | 1.6     | 8.0     | 12.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type         | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC245ADBR   | SSOP                 | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVC245ADGVR  | TVSOP                | DGV             | 20   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LVC245ADWR   | SOIC                 | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVC245ANSR   | SO                   | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVC245APWR   | TSSOP                | PW              | 20   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC245APWRG3 | TSSOP                | PW              | 20   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC245APWRG4 | TSSOP                | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVC245APWT   | TSSOP                | PW              | 20   | 250  | 367.0       | 367.0      | 38.0        |
| SN74LVC245ARGYR  | VQFN                 | RGY             | 20   | 3000 | 367.0       | 367.0      | 35.0        |
| SN74LVC245AZQNR  | BGA MICROSTAR JUNIOR | ZQN             | 20   | 1000 | 350.0       | 350.0      | 43.0        |

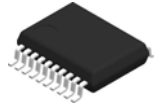
ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BC-2.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## GENERIC PACKAGE VIEW

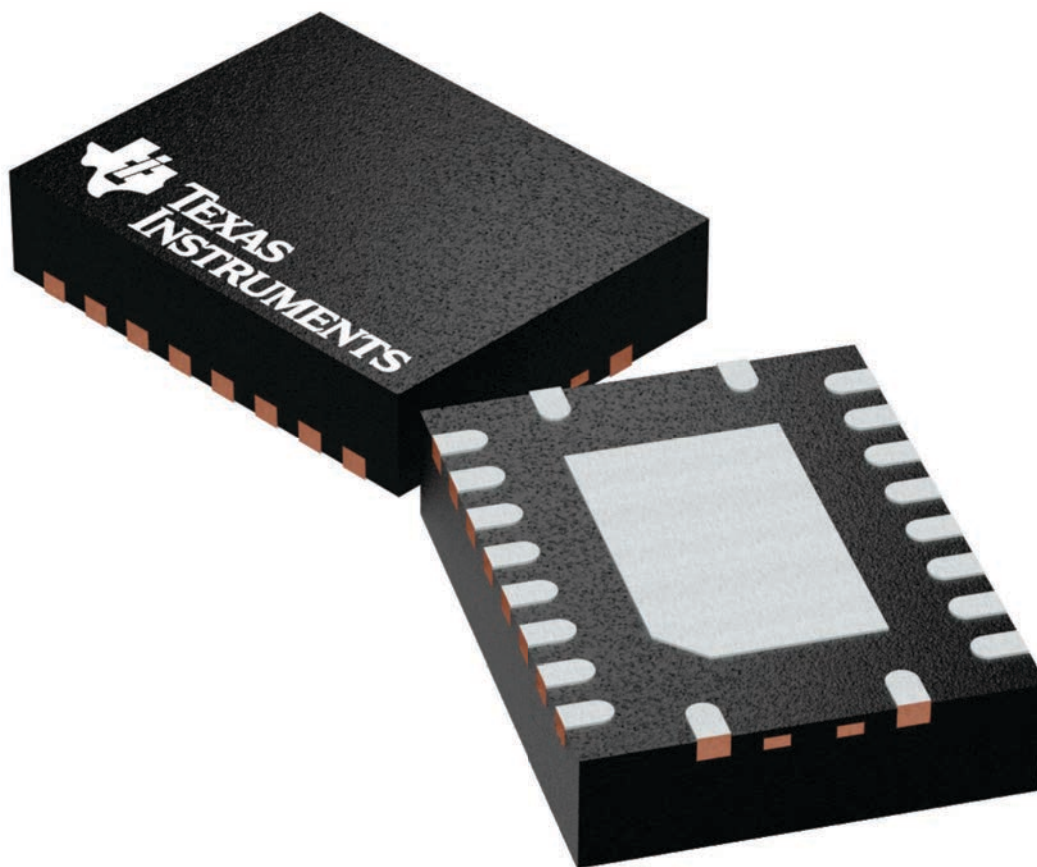
**RGY 20**

**VQFN - 1 mm max height**

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.





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