

SN54AS760, SN74ALS760, SN74AS760 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS141A – DECEMBER 1983 – REVISED JANUARY 1995

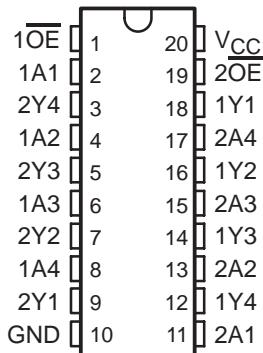
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Eliminates the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of 'ALS244 and 'AS244
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

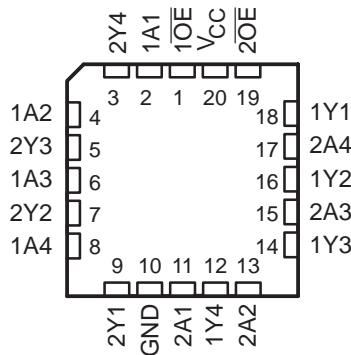
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. With the 'AS756 and SN74AS757, these devices provide the choice of selected combinations of inverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs.

The SN54AS760 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS760 and SN74AS760 are characterized for operation from 0°C to 70°C .

SN54AS760 . . . J PACKAGE
SN74ALS760, SN74AS760 . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS760 . . . FK PACKAGE
(TOP VIEW)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

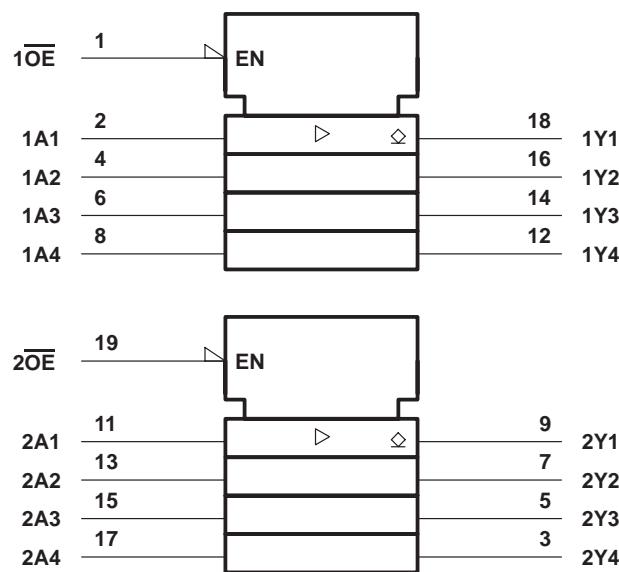
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SN54AS760, SN74ALS760, SN74AS760 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

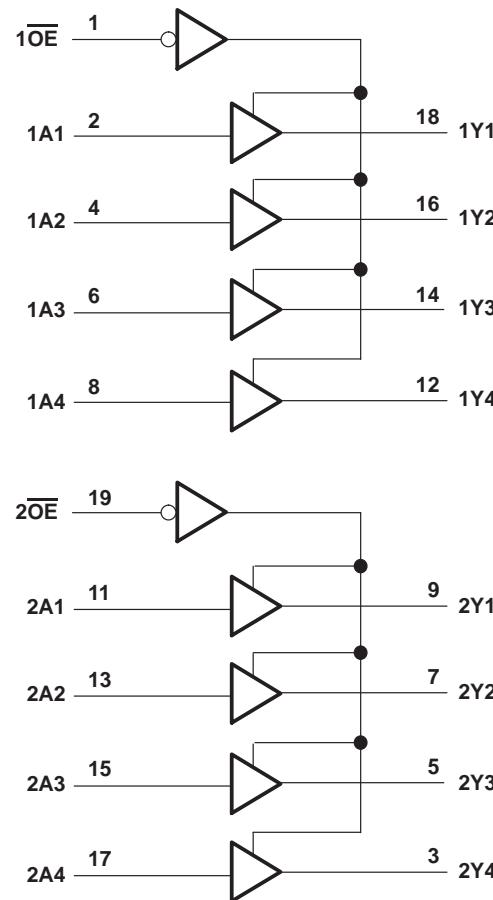
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|--|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Off-state output voltage | 7 V |
| Operating free-air temperature range, T_A : SN74ALS760 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN74ALS760 | | | UNIT |
|----------|--------------------------------|------------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | V |
| V_{OH} | High-level output voltage | | 5.5 | | V |
| I_{OL} | Low-level output current | | 24 | | mA |
| T_A | Operating free-air temperature | 0 | 70 | | °C |



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN74ALS760 | | | UNIT |
|-----------|---|--------------------------|------|------|---------------|
| | | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$ | | | -1.5 | V |
| I_{OH} | $V_{CC} = 4.5 \text{ V}$, $V_{OH} = 5.5 \text{ V}$ | | | 0.1 | mA |
| I_{OL} | $V_{CC} = 4.5 \text{ V}$ | $I_{OL} = 12 \text{ mA}$ | 0.25 | 0.4 | V |
| | | $I_{OL} = 24 \text{ mA}$ | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$ | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$ | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$ | | | -0.1 | mA |
| I_{CC} | $V_{CC} = 5.5 \text{ V}$ | Outputs high | 9 | 15 | mA |
| | | Outputs low | 15 | 19 | |

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\ddagger$ | UNIT | |
|-----------|-----------------|----------------|---|------|----|
| | | | SN74ALS760 | | |
| | | | MIN | MAX | |
| t_{PLH} | A | Y | 5 | 15 | ns |
| | | | 5 | 12 | |
| t_{PHL} | \overline{OE} | Y | 5 | 16 | ns |
| | | | 5 | 13 | |

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Off-state output voltage | 7 V |
| Operating free-air temperature range, T_A : SN54AS760 | -55°C to 125°C |
| SN74AS760 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54AS760, SN74ALS760, SN74AS760
OCTAL BUFFERS AND LINE DRIVERS
WITH OPEN-COLLECTOR OUTPUTS

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recommended operating conditions

| | | SN54AS760 | | | SN74AS760 | | | UNIT |
|-----------------|--------------------------------|-----------|-----|-----|-----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| V _{OH} | High-level output voltage | | | 5.5 | | | 5.5 | V |
| I _{OL} | Low-level output current | | | 48 | | | 64 | mA |
| T _A | Operating free-air temperature | -55 | 125 | 0 | 0 | 70 | °C | |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS760 | | | SN74AS760 | | | UNIT |
|-----------------|--|-------------------------|------|------|-----------|------|------|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | | -1.2 | V |
| I _{OH} | V _{CC} = 4.5 V, V _{OH} = 5.5 V | | | 0.1 | | | 0.1 | mA |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = 48 mA | | 0.55 | | | | V |
| | | I _{OL} = 64 mA | | | | | 0.55 | |
| I _I | V _{CC} = 5.5 V, V _I = 7 V | | | 0.1 | | | 0.1 | mA |
| I _{IH} | V _{CC} = 5.5 V, V _I = 2.7 V | | | 20 | | | 20 | µA |
| I _{IL} | V _{CC} = 5.5 V, V _I = 0.4 V | | | -0.5 | | | -0.5 | mA |
| | | | | -1 | | | -1 | |
| I _{CC} | V _{CC} = 5.5 V | Outputs high | 20 | 32 | 20 | 32 | | mA |
| | | Outputs low | 60 | 94 | 60 | 94 | | |

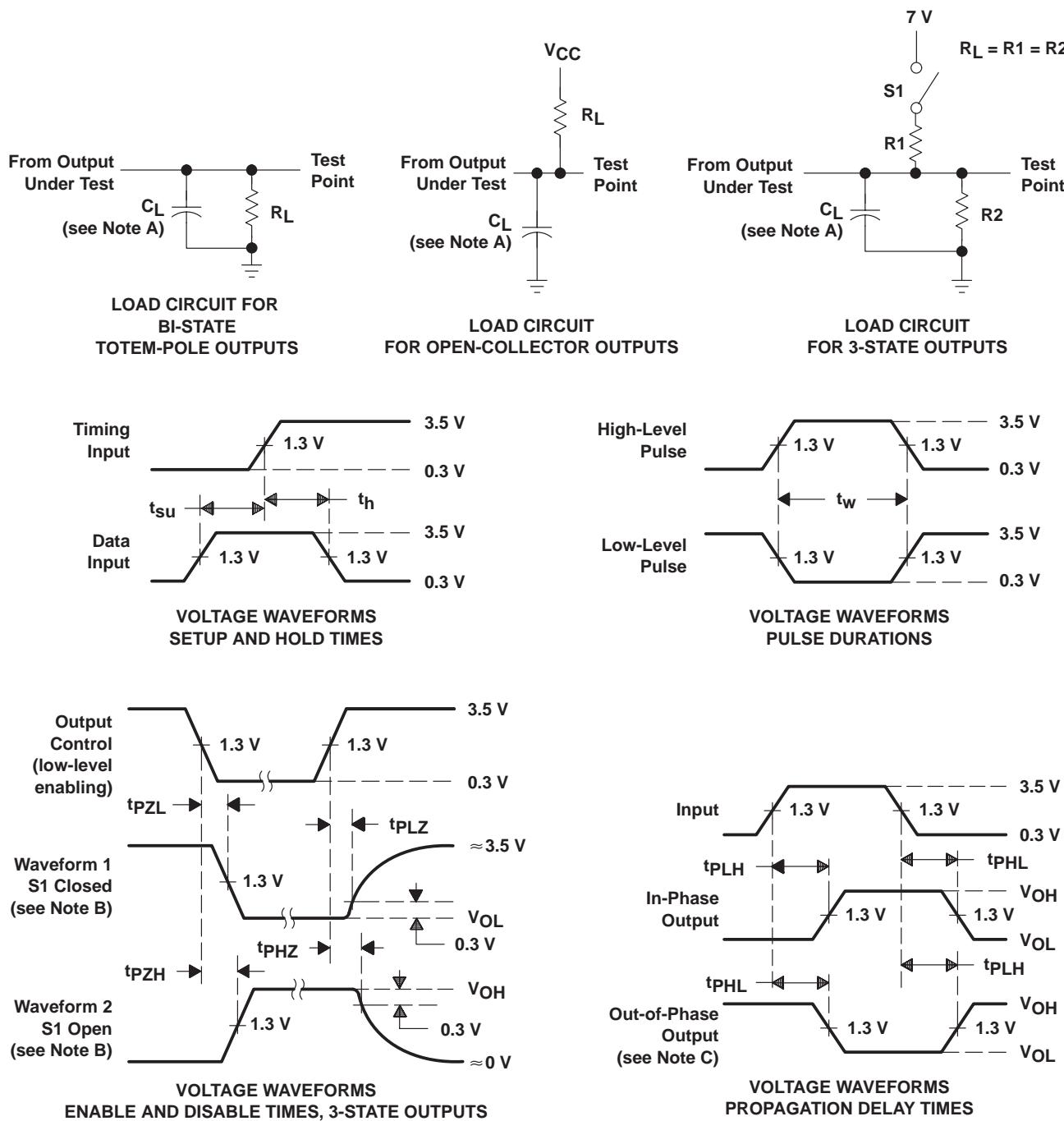
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX‡ | | | | UNIT | |
|------------------|--------------|-------------|--|------|-----------|------|------|--|
| | | | SN54AS760 | | SN74AS760 | | | |
| | | | MIN | MAX | MIN | MAX | | |
| t _{PLH} | A | Y | 3 | 19.5 | 3 | 18.5 | ns | |
| t _{PHL} | | | 1 | 7 | 1 | 6 | | |
| t _{PLH} | OE | Y | 3 | 19.5 | 3 | 18.5 | ns | |
| t _{PHL} | | | 1 | 8 | 1 | 7 | | |

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-87767012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-87767012A SNJ54AS 760FK | Samples |
| 5962-8776701RA | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776701RA SNJ54AS760J | Samples |
| SN74ALS760DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS760 | Samples |
| SN74ALS760DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS760 | Samples |
| SN74ALS760N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS760N | Samples |
| SN74AS760DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS760 | Samples |
| SN74AS760DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS760 | Samples |
| SN74AS760N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS760N | Samples |
| SN74AS760NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS760 | Samples |
| SNJ54AS760FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-87767012A SNJ54AS 760FK | Samples |
| SNJ54AS760J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776701RA SNJ54AS760J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AS760, SN74AS760 :

- Catalog: [SN74AS760](#)
- Military: [SN54AS760](#)

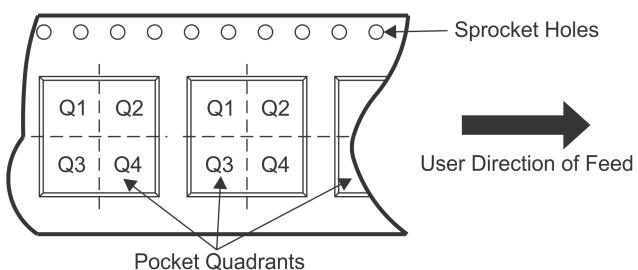
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AS760DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AS760NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

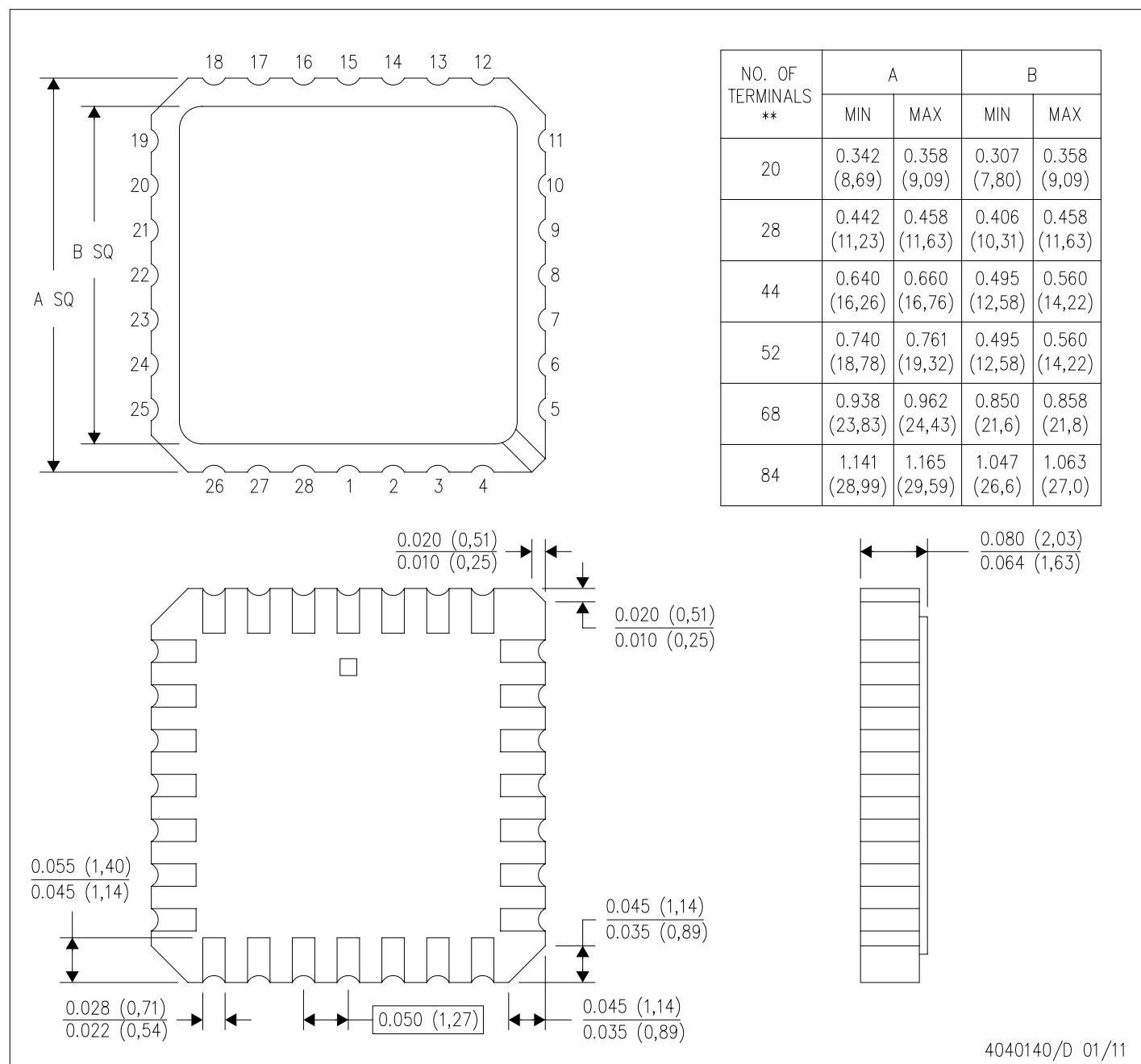
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AS760DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AS760NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

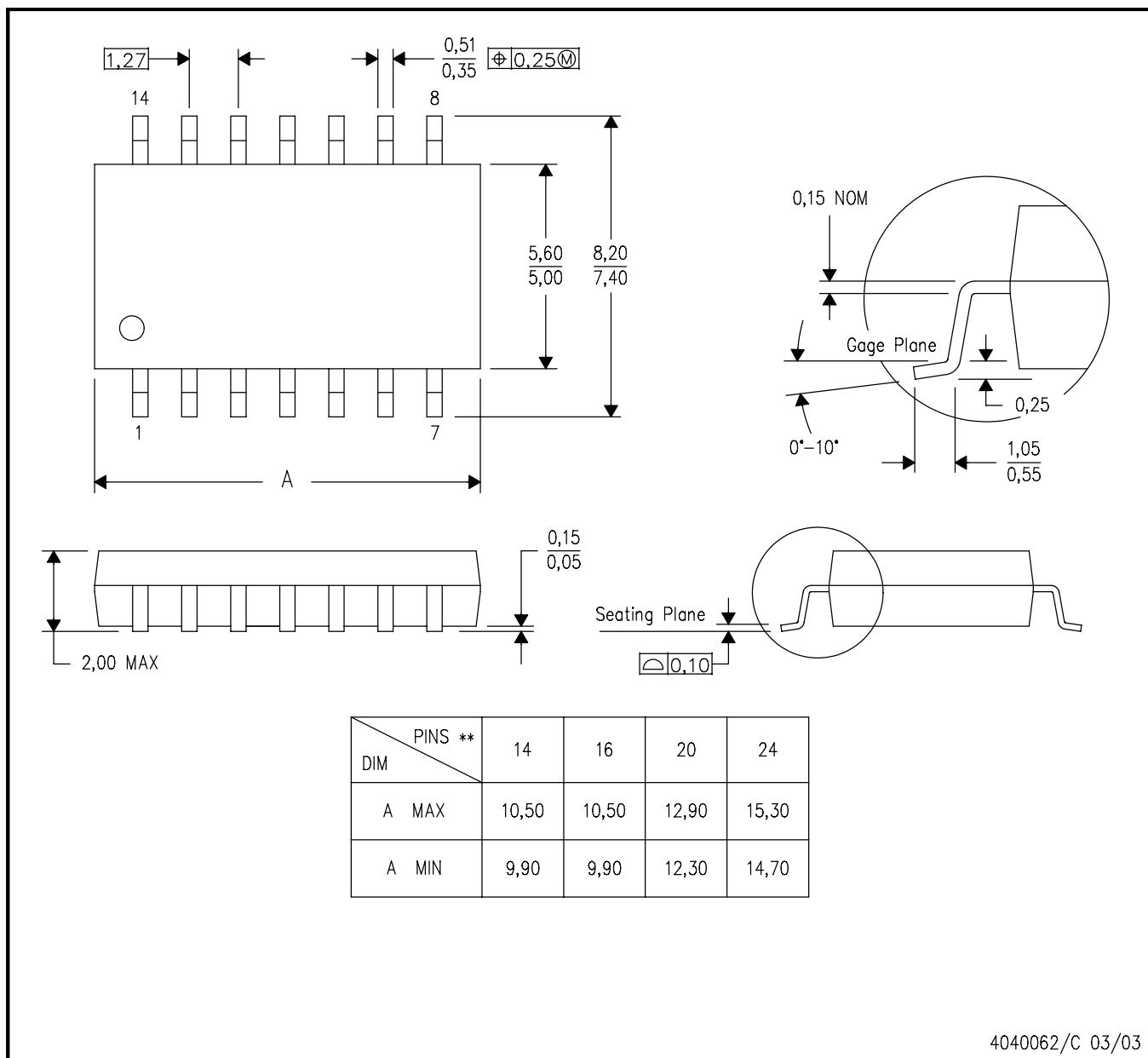
4040140/D 01/11

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



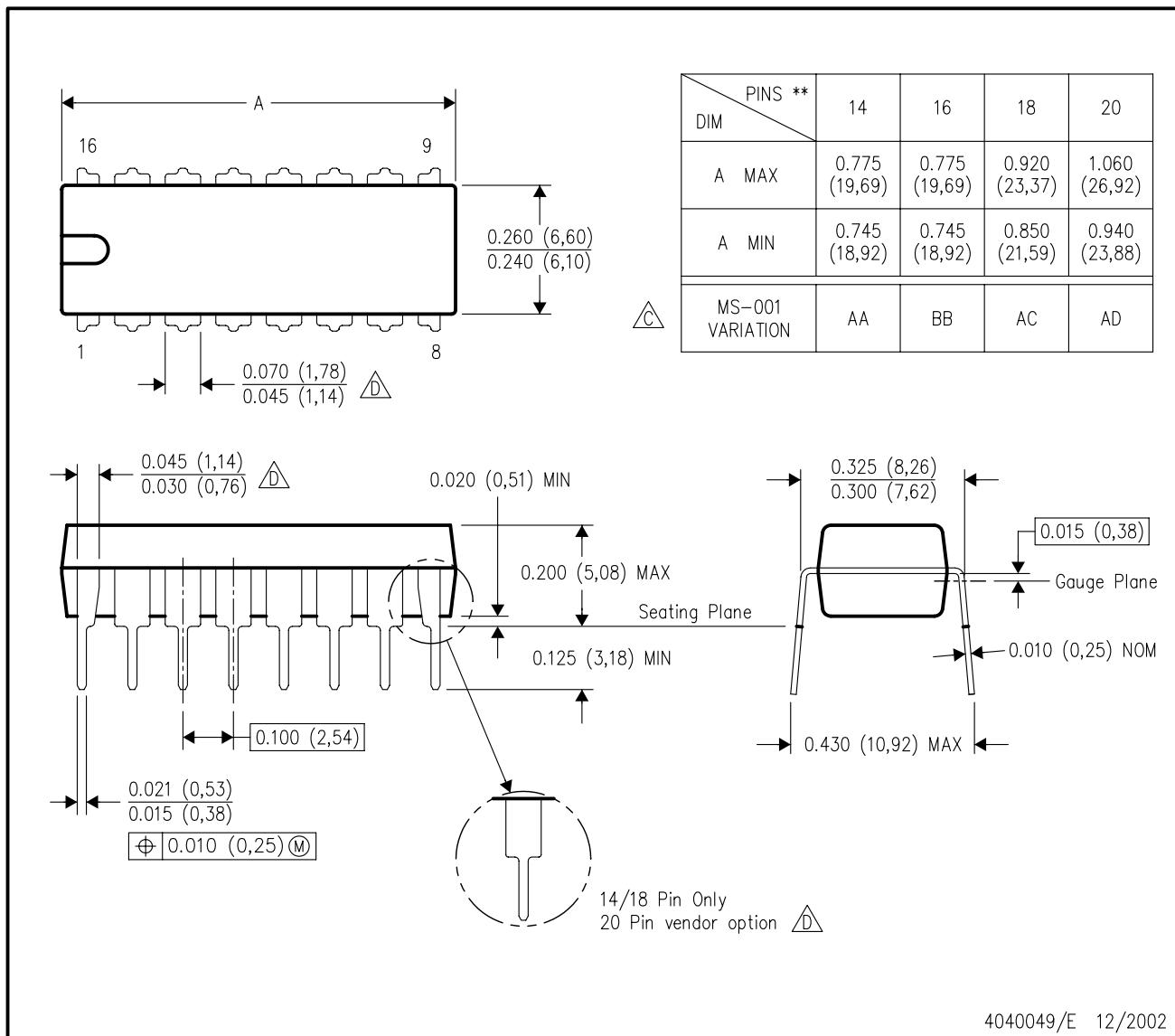
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

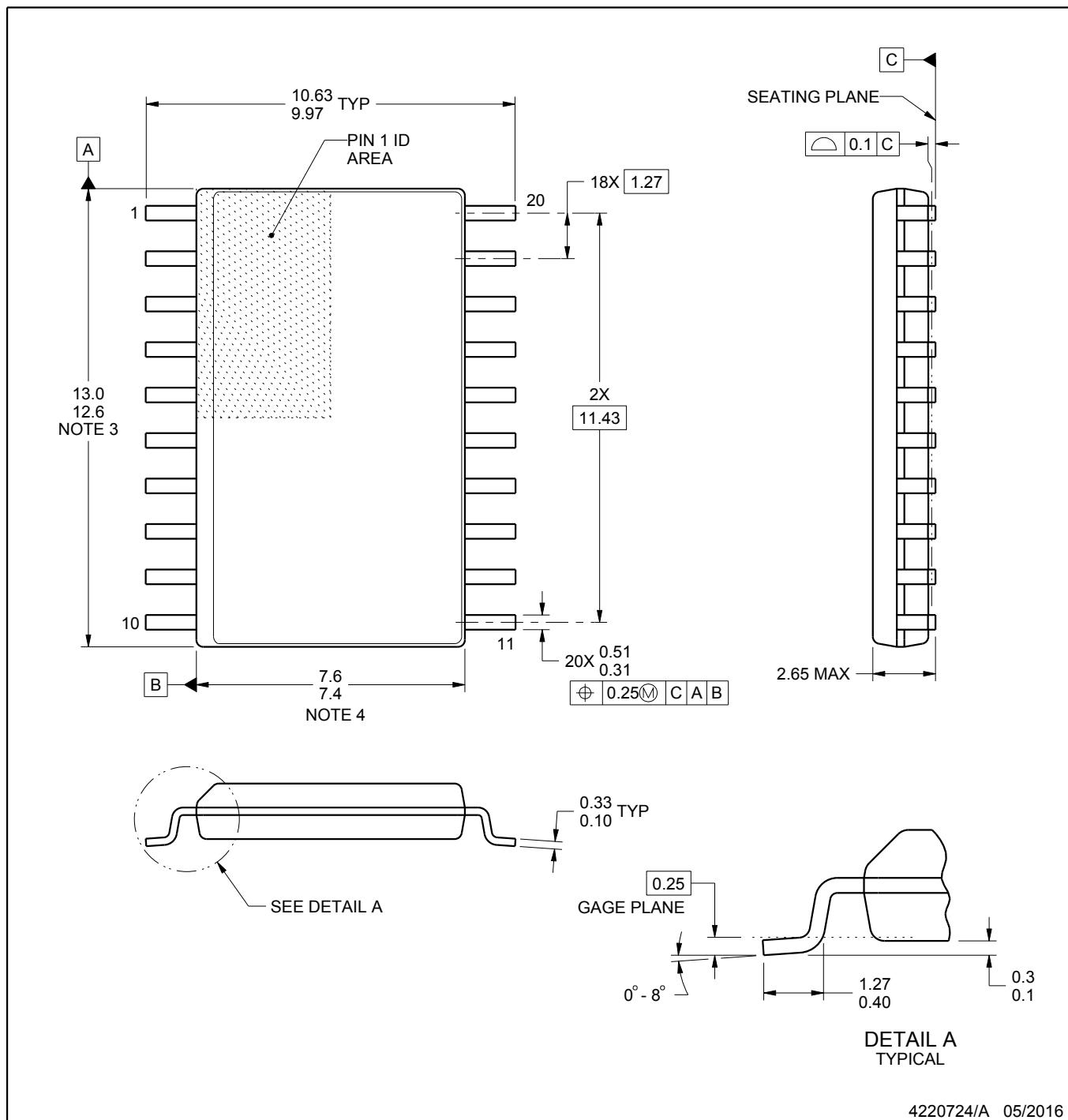


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIG



NOTES:

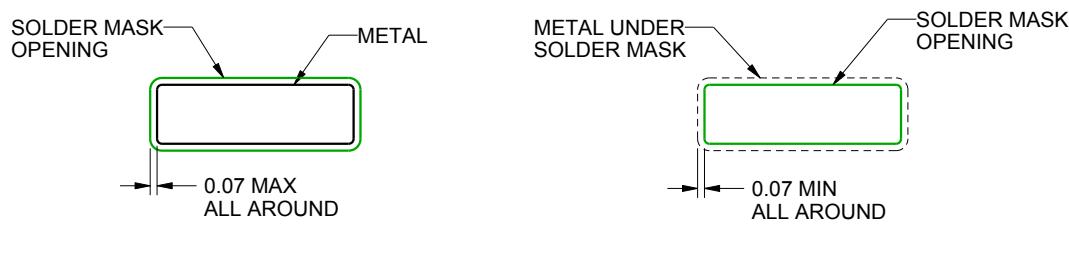
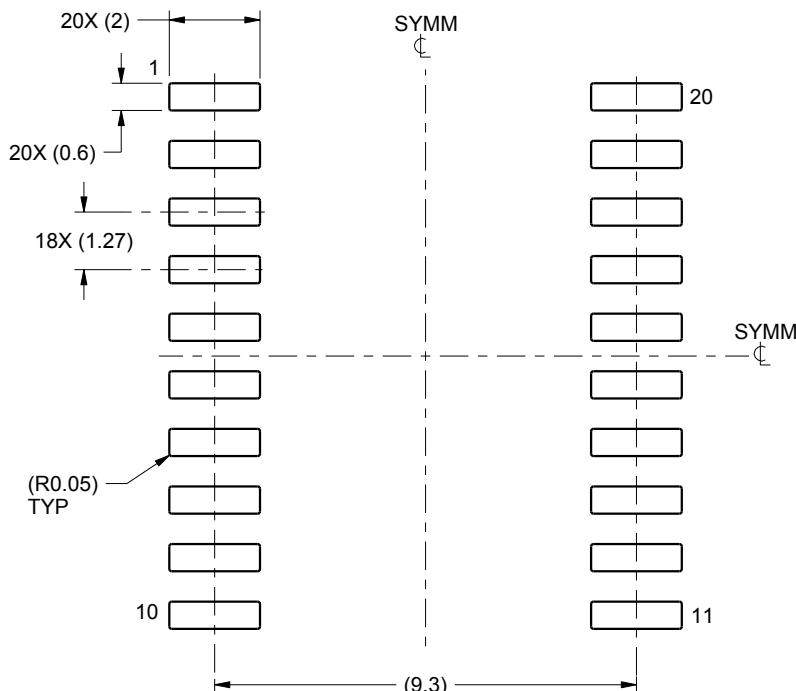
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

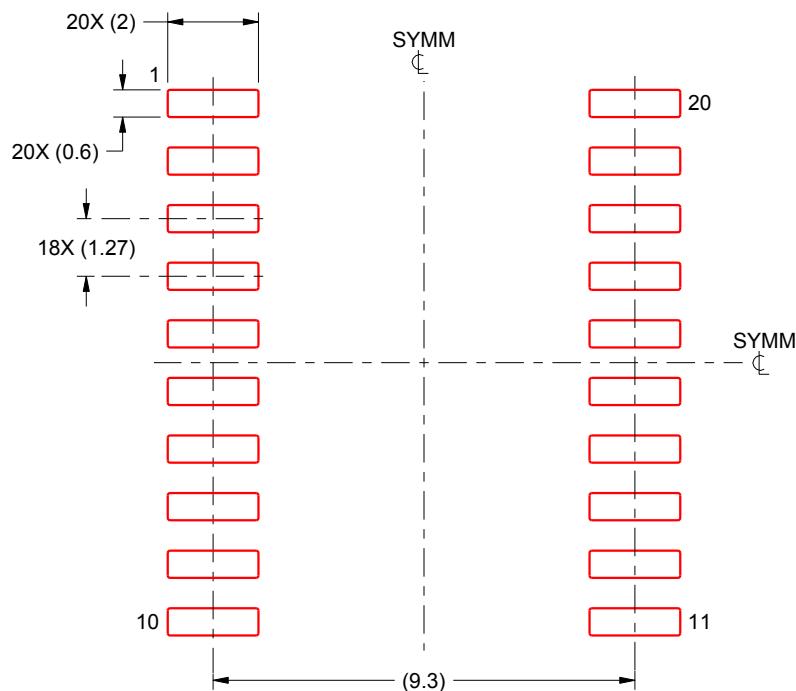
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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