

- Shorted load protection
- Thermal shutdown
- Very low standby current
- Protection against loss of ground

Description

The VNQ860-E and the VNQ860SP-E are monolithic devices realized in STMicroelectronics VIPower M0-3 technology, intended to drive any kind of load with one side connected to ground. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for IEC 61131 compliant industrial applications.

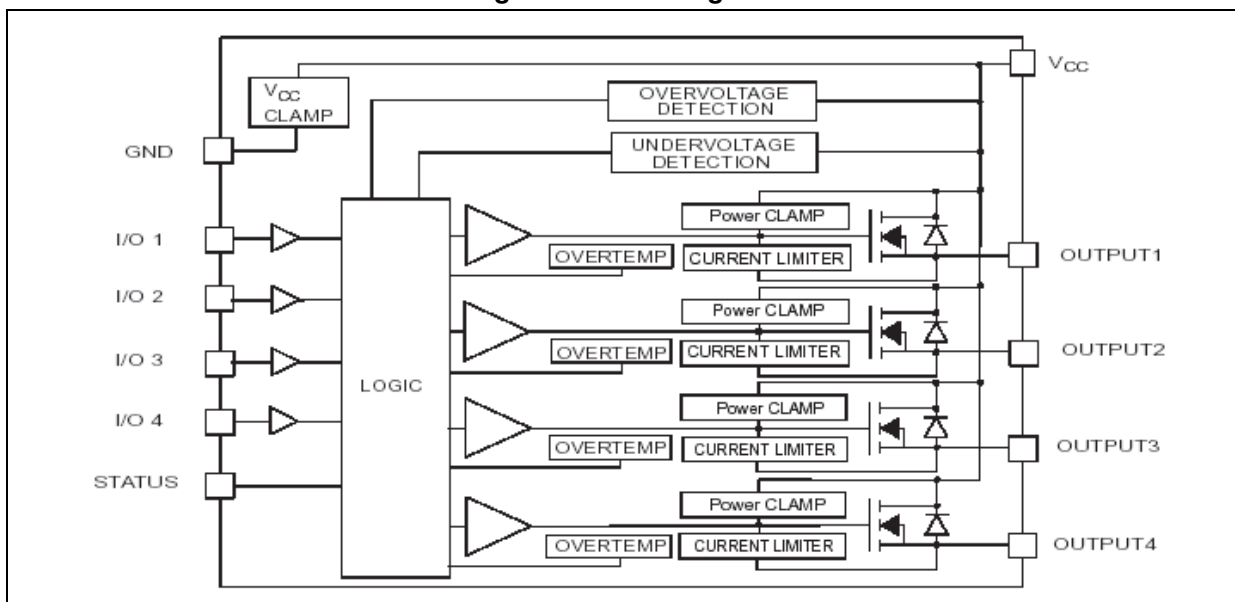
Features

Type	$R_{DS(on)}^{(1)}$	I_{out}	V_{CC}
VNQ860-E VNQ860SP-E	270 mΩ	0.25 A	36 V

1. Per each channel

- CMOS compatible I/Os
- Undervoltage and overvoltage shutdown

Figure 1. Block diagram



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1 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SO20	PowerSO-10	
V_{CC}	DC supply voltage	41		V
$-V_{CC}$	Reverse DC supply voltage	-0.3		V
$-I_{GND}$	DC reverse ground pin	-200		mA
I_{OUT}	DC output current	Internally limited		A
$-I_{OUT}$	Reverse DC output current	-2		A
I_{IN}	DC input current	± 10		mA
V_{IN}	Input voltage range	$-3/+V_{CC}$		V
V_{STAT}	DC status voltage	$+ V_{CC}$		V
V_{ESD}	Electrostatic discharge (R = 1.5 k Ω , C = 100 pF)	2000		V
P_{tot}	Power dissipation at $T_c \leq 25$ °C	16	90	W
T_J	Junction operating temperature	Internally limited		°C
T_c	Case operating temperature	-40 to 150		°C
T_{stg}	Storage temperature	-55 to 150		°C

Table 2. Thermal data

Symbol	Parameter		Values		Unit
			SO20	PowerSO-10	
$R_{th(JP)}$	Thermal resistance junction-pins	Max.	8	-	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	Max.	58	52 ⁽¹⁾	°C/W
				37 ⁽²⁾	
$R_{th(JC)}$	Thermal resistance junction-case	Max.	-	1.4	°C/W

1. When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35 μ thick) connected to all V_{CC} pins.
2. When mounted on FR4 printed circuit board with 6 cm² of copper area (at least 35 μ thick) connected to all V_{CC} pins.

2 Pin connection

Figure 2. Configuration diagram (top view)

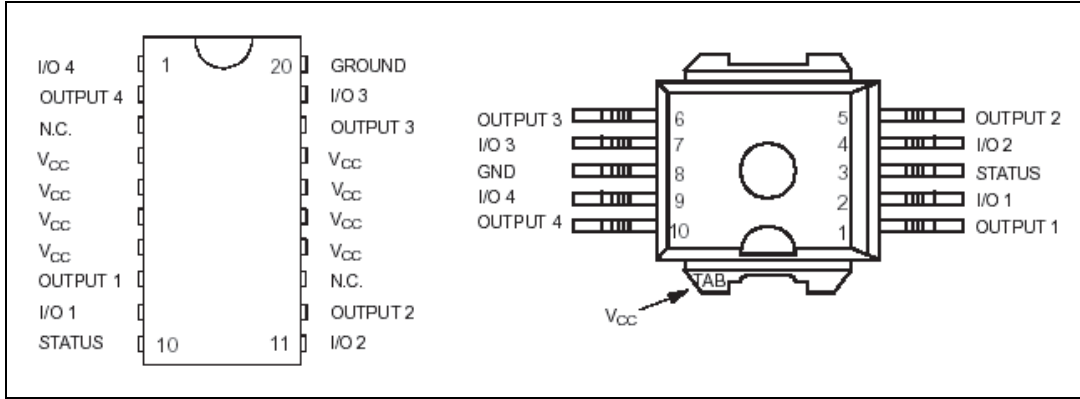
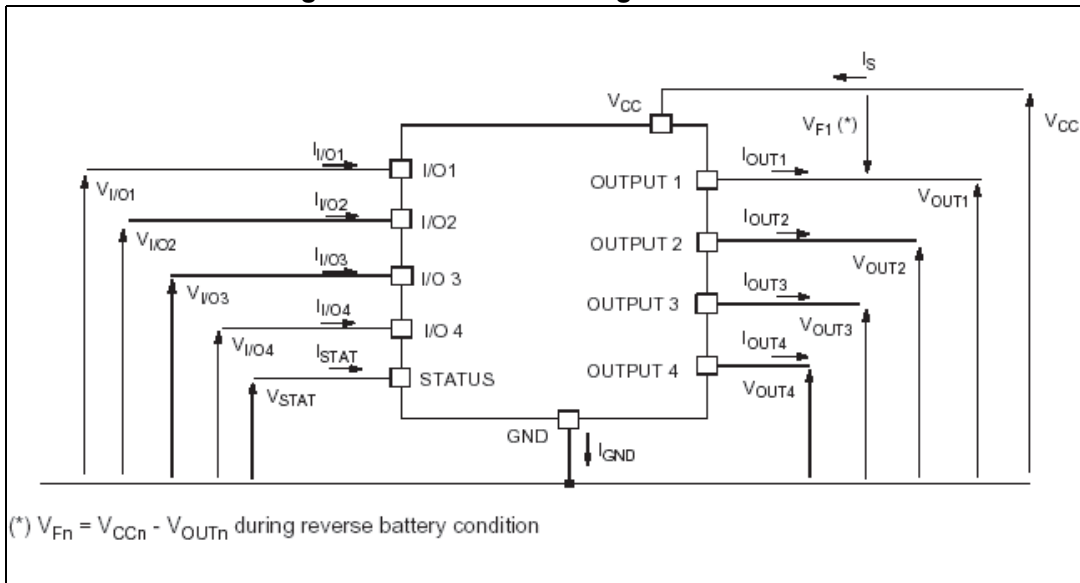


Table 3. Pin connection

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 kΩ resistor

Figure 3. Current and voltage conventions



3 Electrical characteristics

$8\text{ V} < V_{CC} < 36\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_J < 150\text{ }^{\circ}\text{C}$; unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5		36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36	42	48	V
R_{ON}	On state resistance (per channel)	$I_{OUT} = 0.25\text{ A}$; $T_J = 25\text{ }^{\circ}\text{C}$; $I_{OUT} = 0.25\text{ A}$;			270 540	m Ω
I_S	Supply current	OFF state; $V_{CC} = 24\text{ V}$; $T_C = 25\text{ }^{\circ}\text{C}$ ON state (all channels ON)		70 5	120 10	μA mA
I_{LGND}	Output current	$V_{CC} - V_{STAT} = V_{IN} = V_{GND} = 24\text{ V}$; $V_{OUT} = 0\text{ V}$			1	mA
$I_{L(OFF)}$	OFF state output current	$V_{IN} = V_{OUT} = 0\text{ V}$	0		10	μA
$I_{OUTleak}$	OFF state output leakage current	$V_{IN} = V_{GND} = 0\text{ V}$; $V_{CC} = V_{OUT} = 24\text{ V}$; $T_A = 25\text{ }^{\circ}\text{C}$			240	μA
$I_{OUTleak}$	OFF state output leakage current	$V_{IN} = V_{GND} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $V_{OUT} = 10\text{ V}$; $T_A = 25\text{ }^{\circ}\text{C}$			100	μA

Table 5. Switching ($V_{CC} = 24\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{(ON)}$	Turn-on delay time of output current	$R_L = 96\text{ }\Omega$ from V_{IN} rising edge to $V_{OUT} = 2.4\text{ V}$	-	10	-	μs
$t_{(OFF)}$	Turn-off delay time of output current	$R_L = 96\text{ }\Omega$ from V_{IN} rising edge to $V_{OUT} = 21.6\text{ V}$	-	40	-	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 96\text{ }\Omega$ from $V_{OUT} = 2.4\text{ V}$ to 19.2 V	-	0.75	-	V/ μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 96\text{ }\Omega$ from $V_{OUT} = 21.6\text{ V}$ to 2.4 V	-	0.25	-	V/ μs

Table 6. Protections (per channel)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Current limitation		0.35	0.7	1.1	A
$T_{(hyst)}$	Thermal hysteresis		7	15		°C
T_{TSD}	Thermal shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 0.25 \text{ A}$, $V_{CC} = 24 \text{ V}$	$V_{CC} - 59$	$V_{CC} - 52$	$V_{CC} - 47$	V

Table 7. Logic input (per channel)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage			-	1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25 \text{ V}$	1	-		μA
V_{IH}	High level input voltage		3.25	-		V
I_{IH}	High level input current	$V_{IN} = 3.25 \text{ V}$		-	10	μA
$V_{I(HYST)}$	Input hysteresis voltage		0.5	-		V
I_{IN}	Input current	$V_{IN} = V_{CC} = 36 \text{ V}$		-	200	μA
V_{OL}	I/O output voltage	$I_{IN} = 5 \text{ mA}$ (fault condition)		-	1	V

Table 8. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 5 \text{ mA}$ (fault condition)	-	-	1	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = V_{CC} = 36 \text{ V}$	-	-	10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5 \text{ V}$	-	-	100	pF

Table 9. V_{CC} - output diode

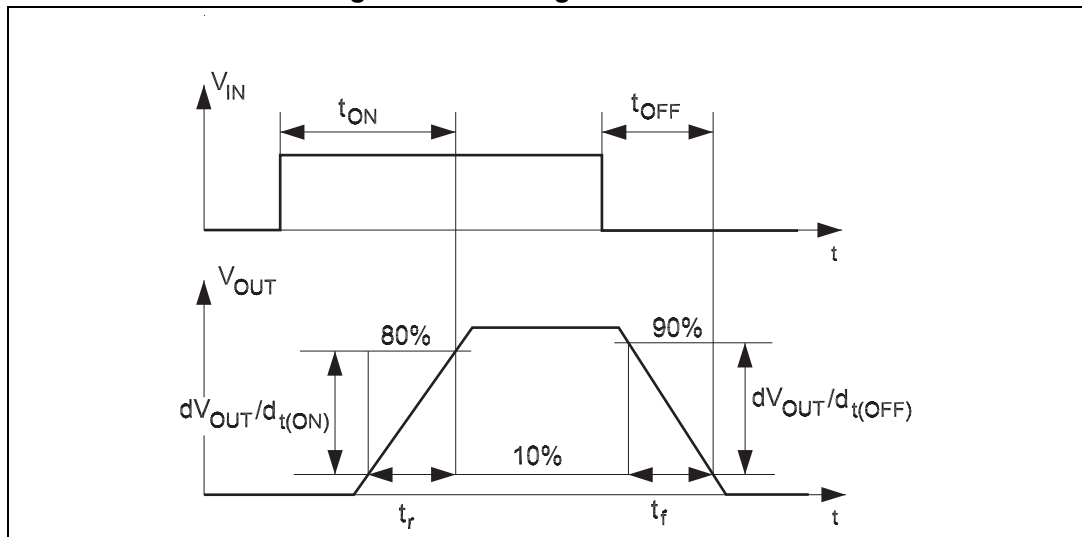
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT} = 0.3 \text{ A}$; $T_J = 150 \text{ °C}$	-	-	1	V

4 Truth table and switching characteristics

Table 10. Truth table

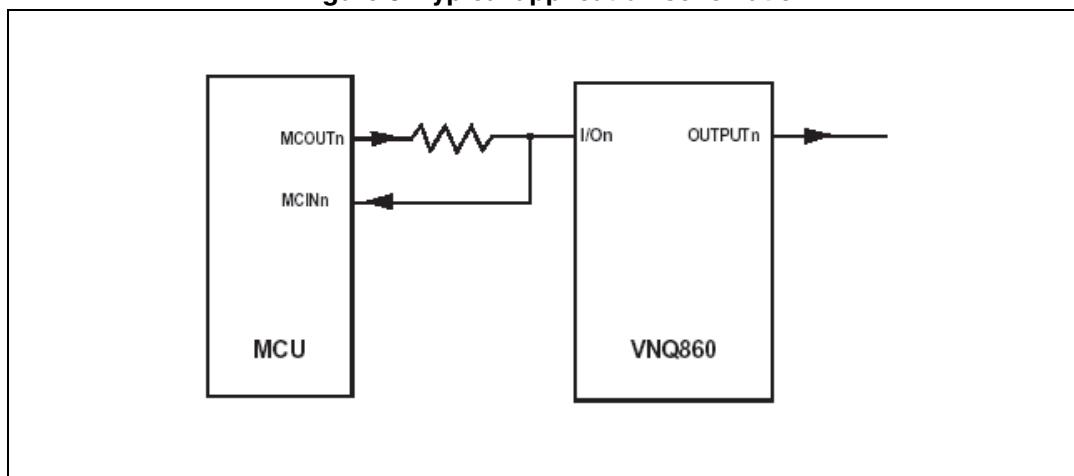
Conditions	MCOUTn	I/On	OUTPUTn	STATUS
Normal operation	L	L	L	H
	H	H	H	H
Current limitation	L	L	L	H
	H	H	X	H
Overtemperature	L	L	L	L
	H	Driven low	L	L
Undervoltage	L	L	L	X
	H	H	L	X
Overvoltage	L	L	L	H
	H	H	L	H

Figure 4. Switching characteristics



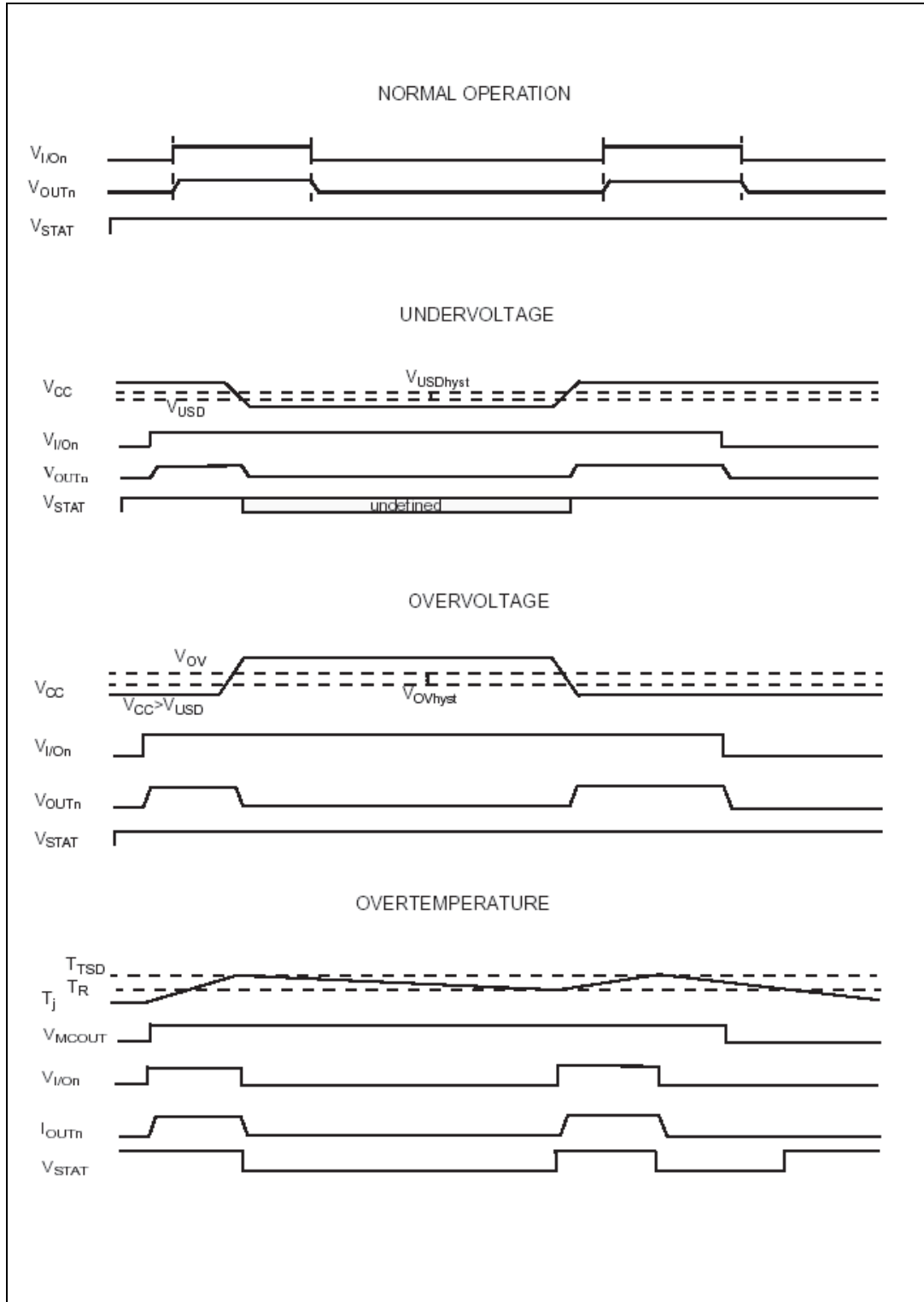
5 Typical application schematic

Figure 5. Typical application schematic



6 Waveforms

Figure 6. Waveforms



7 PowerSO-10™ thermal data

Figure 7. PowerSO-10™ PC board

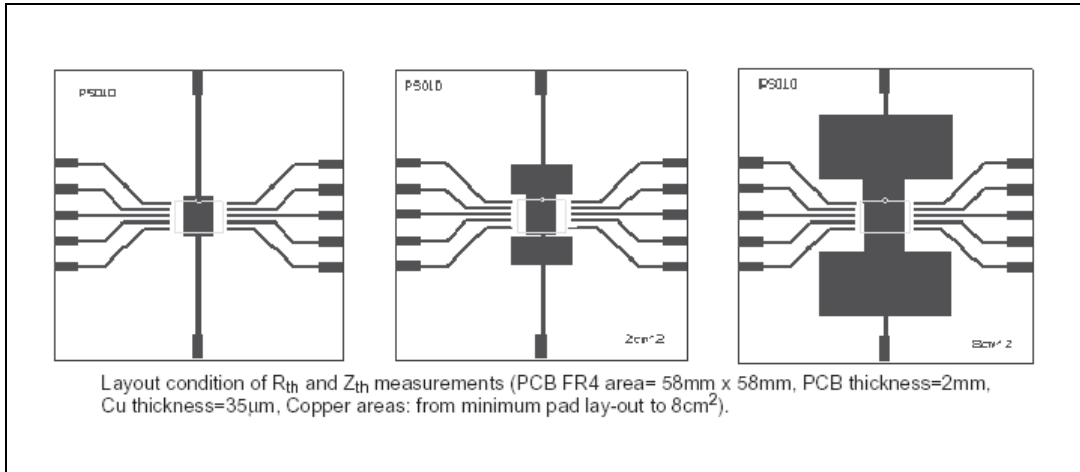
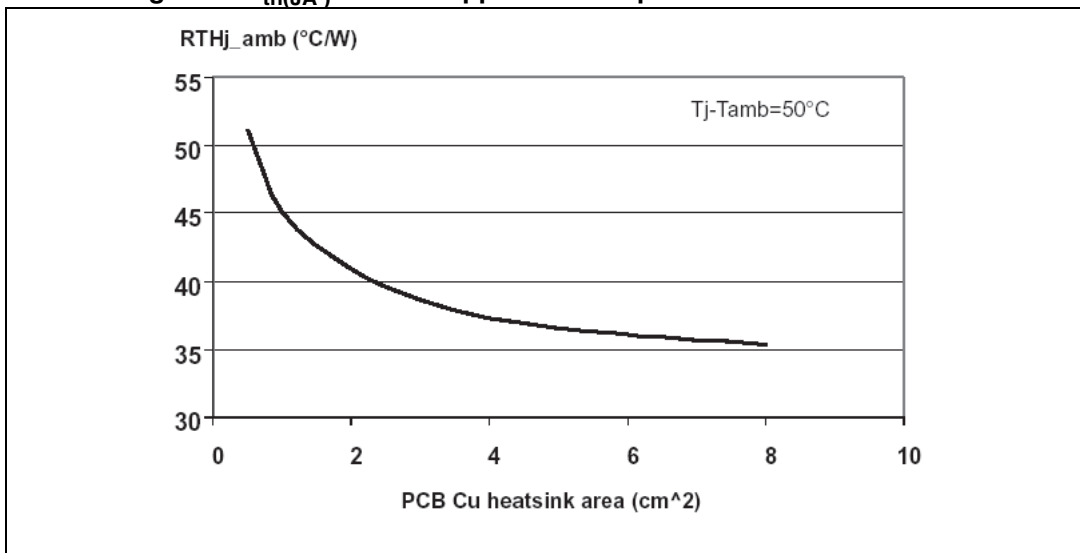


Figure 8. $R_{th(JA)}$ vs PBC copper area in open box free air condition



8 Reverse polarity protection

A solution to protect the IC against a reverse polarity condition is proposed in [Figure 9](#).

This schematic is valid with any type of load connected to the outputs of the IC.

The R_{GND} resistor value can be selected according to the following conditions:

Equation 1

$$R_{GND} \leq 600 \text{ mV} / (I_S \text{ in ON state max.}).$$

Equation 2

$$R_{GND} \geq (-V_{CC}) / (-I_{GND})$$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in [Table 1: Absolute maximum ratings](#).

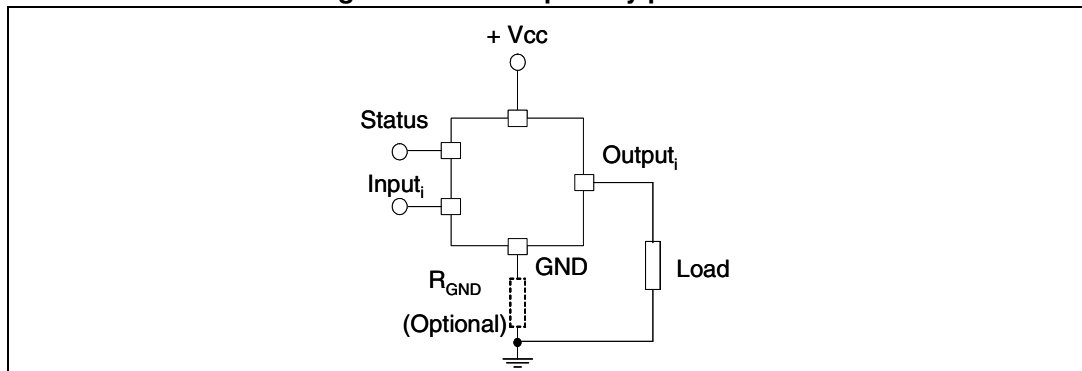
The power dissipation associated to R_{GND} during the reverse polarity condition is:

$$PD = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared by different ICs. In such case, I_S value, indicated in [Equation 1](#), is the sum of the maximum ON-state currents of the different devices.

Please note that, if the microprocessor ground and the device ground are separated then the voltage drop across the R_{GND} (given by I_S in ON state max. * R_{GND}) produces a difference between the generated input level and the IC input signal level. This voltage drop varies depending on how many devices are ON in the case of several high-side switches sharing the same R_{GND} .

Figure 9. Reverse polarity protection



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 11. PowerSO-10™ mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
a	0°		8°			

Figure 10. PowerSO-10™ package dimensions

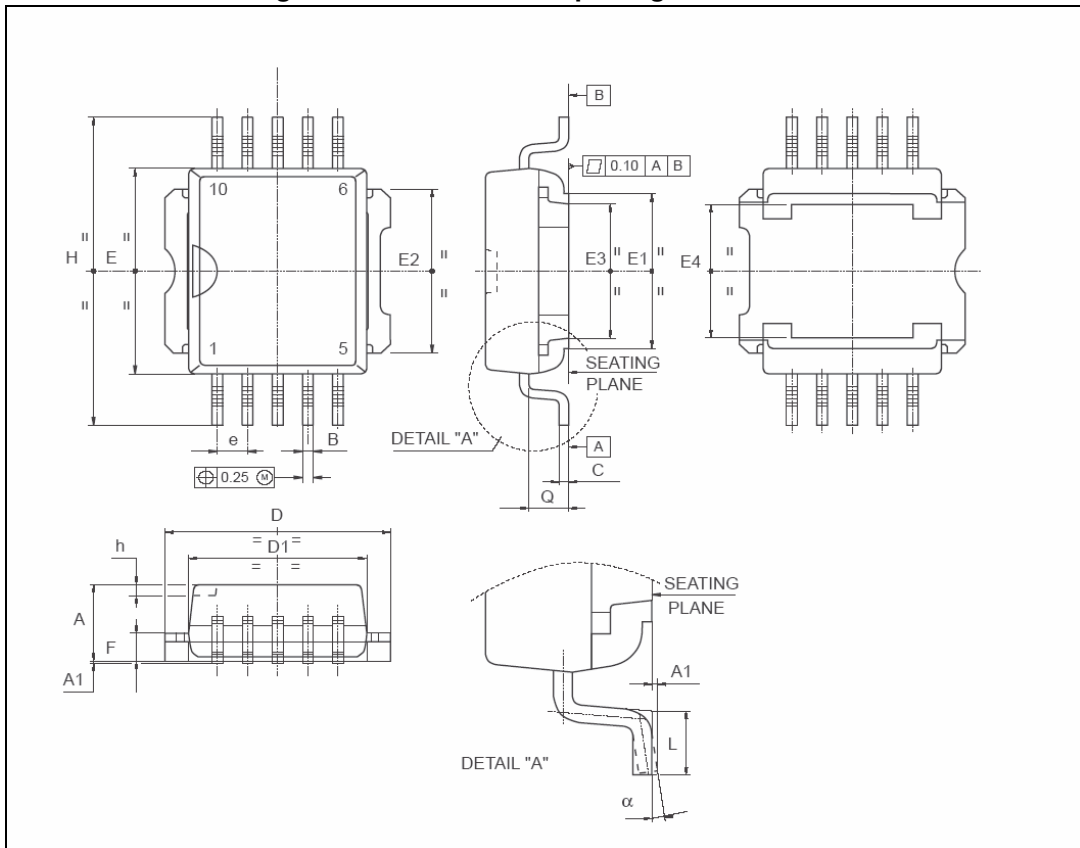


Figure 11. PowerSO-10™ suggested pad and tube shipment (no suffix)

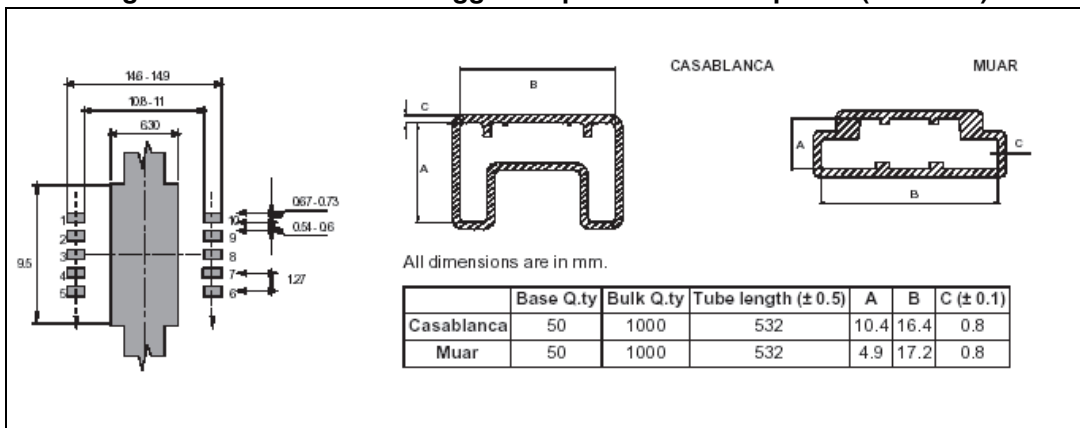


Figure 12. Tape and reel shipment (suffix “TR”)

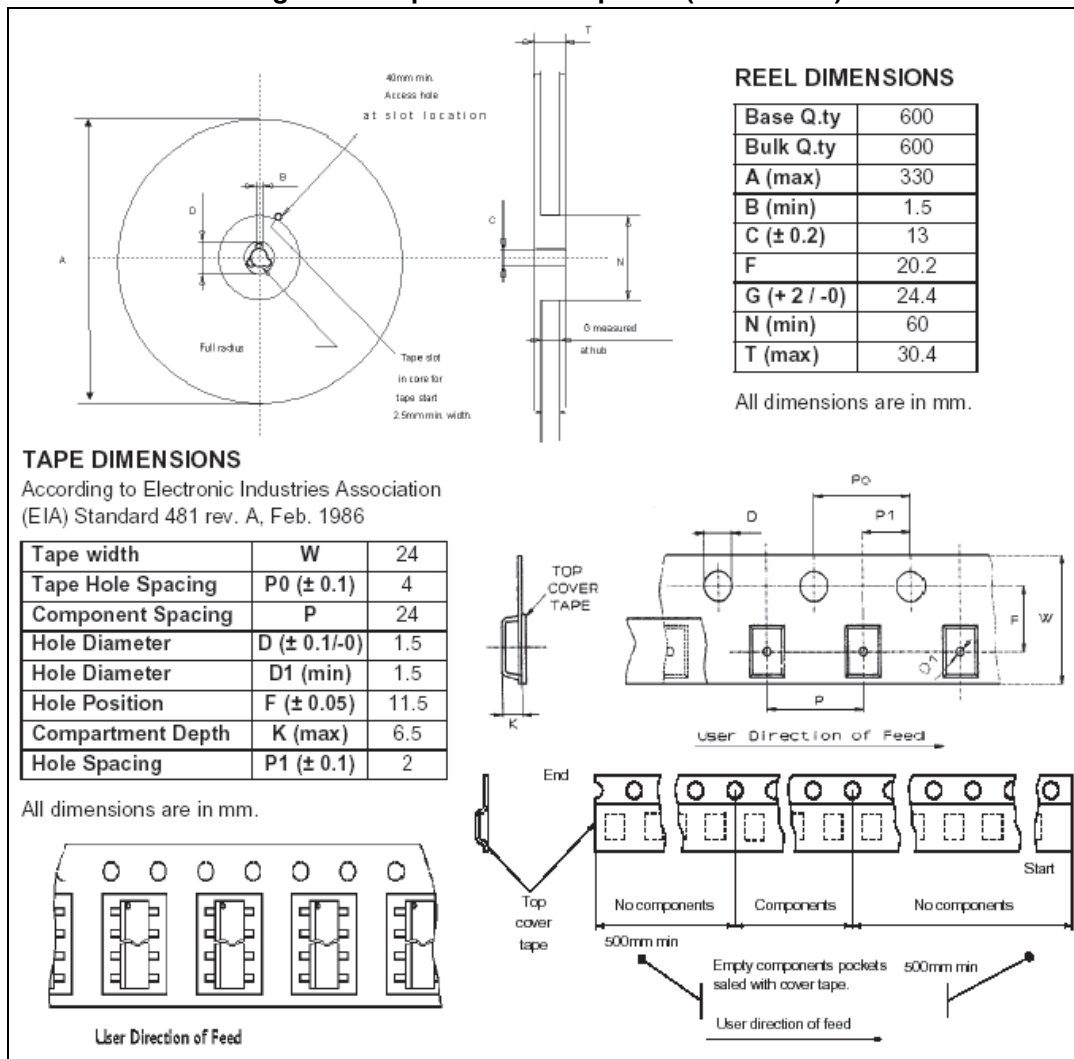


Figure 13. SO20 mechanical data and package dimensions

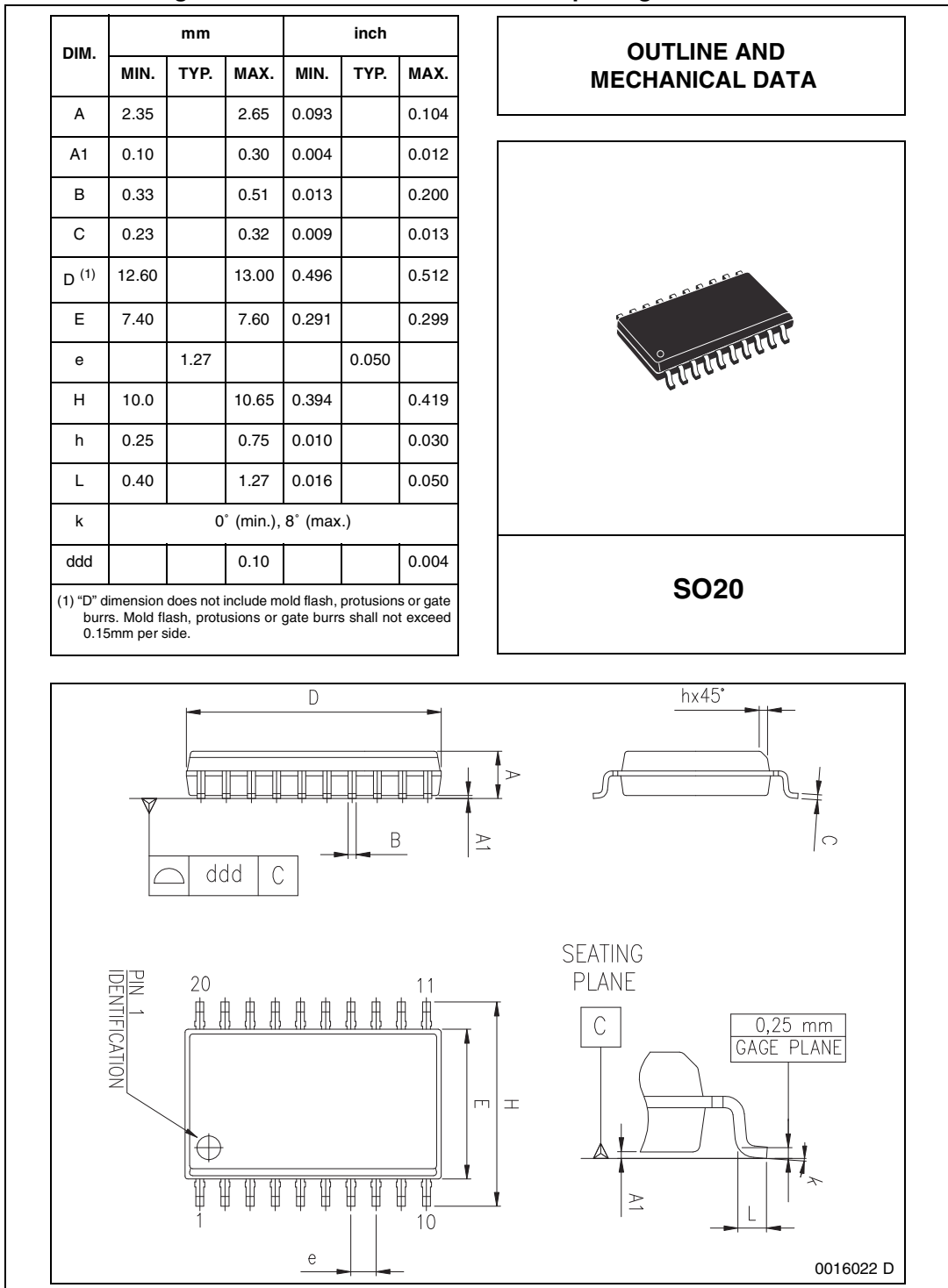


Figure 14. SO20 tube shipment (no suffix)

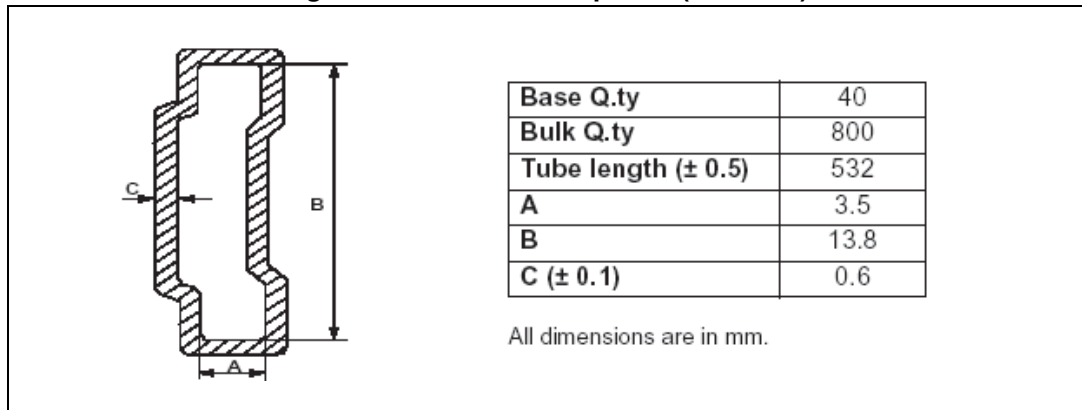
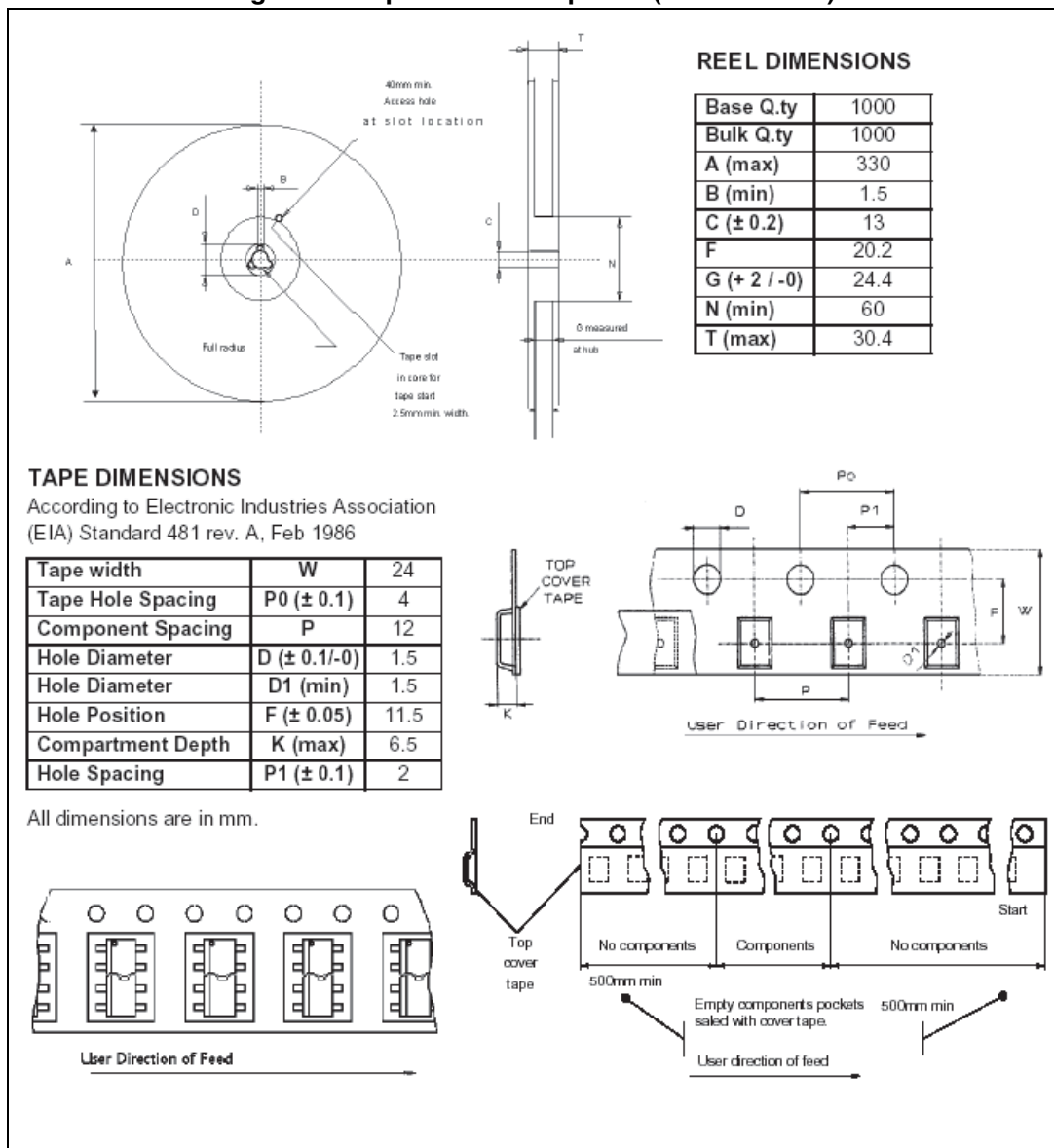


Figure 15. Tape and reel shipment (suffix "13TR")



10 Ordering information

Table 12. Ordering information

Order codes	Package	Packaging
VNQ860-E	SO20	Tube
VNQ860SP-E	PowerSO-10™	
VNQ860TR-E	SO20	Tape and reel
VNQ860SPTR-E	PowerSO-10™	

11 Revision history

Table 13. Document revision history

Date	Revision	Changes
14-Jul-2005	1	Updates, new template
7-Nov-2005	2	Few updates
07-Jul-2008	3	Added <i>Section 8 on page 11</i>
28-Apr-2009	4	Updated <i>Figure 13 on page 15</i>
05-May-2010	5	Updated coverpage
31-Aug-2010	6	Updated <i>Table 10 on page 7</i>
15-Mar-2013	7	Updated <i>Table 1</i> and <i>Table 12</i> . Minor text changes.

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