



## High Performance Sensorless Motor Control IC

### Description

IRMCF188 is a high performance Flash based motion control IC designed and optimized for complete air conditioner control which contains two computation engines integrated into one monolithic chip. One is the Flexible Motion Control Engine (MCE™) for sensorless control of permanent magnet motors or induction motors; the other is an 8-bit high-speed microcontroller (8051). The user can program a motion control algorithm by connecting these control elements using a graphic compiler. Key components of the complex sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks. A unique analog/digital circuit and algorithm fully supports single shunt or leg shunt current reconstruction. IRMCF188 performs a PFC (Power Factor Correction) function in addition to the motor control. IRMCF188 comes in a 64 pin QFP package.

### Features

- MCE™ (Flexible Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal sensorless motor control
- Built-in hardware peripheral for single or two shunt current feedback reconstruction and analog circuits
- Supports induction machine and both interior and surface permanent magnet motor sensorless control
- Dedicated PFC PWM for digital PFC control
- Loss minimization Space Vector PWM
- Three-channel analog output (PWM)
- Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control
- JTAG programming port for emulation/debugger
- Serial communication interface (UART)
- I2C/SPI serial interface
- Three general purpose timers/counters
- Two special timers: periodic timer, capture timer
- Watchdog timer with independent internal clock
- Internal 64 Kbyte flash memory
- 3.3V single supply

### Product Summary

|                                              |                 |
|----------------------------------------------|-----------------|
| Maximum clock input ( $f_{\text{crystal}}$ ) | 60 MHz          |
| Maximum Internal clock (SYSCLK)              | 120MHz          |
| Maximum 8051 clock (8051CLK)                 | 30MHz           |
| MCE™ computation data range                  | 16 bit signed   |
| 8051 Program Flash                           | 52KB            |
| 8051/MCE Data RAM                            | 4KB             |
| MCE Program RAM                              | 12KB            |
| GateKill latency (digital filtered)          | 2 $\mu$ sec     |
| PWM carrier frequency                        | 20 bits/ SYSCLK |
| A/D input channels                           | 10              |
| A/D converter resolution                     | 12 bits         |
| A/D converter conversion speed               | 2 $\mu$ sec     |
| Analog output (PWM) resolution               | 8 bits          |
| UART baud rate (typ)                         | 57.6 Kbps       |
| Number of digital I/O (max)                  | 24              |
| Package (lead free)                          | QFP64           |
| Typical 3.3V operating current               | 30mA            |

| Base Part Number | Package Type | Standard Pack |          | Orderable Part Number |
|------------------|--------------|---------------|----------|-----------------------|
|                  |              | Form          | Quantity |                       |
| IRMCF188         | LQFP64       | Tape and Reel | 1500     | IRMCF188TR            |
| IRMCF188         | LQFP64       | Tray          | 1600     | IRMCF188TY            |

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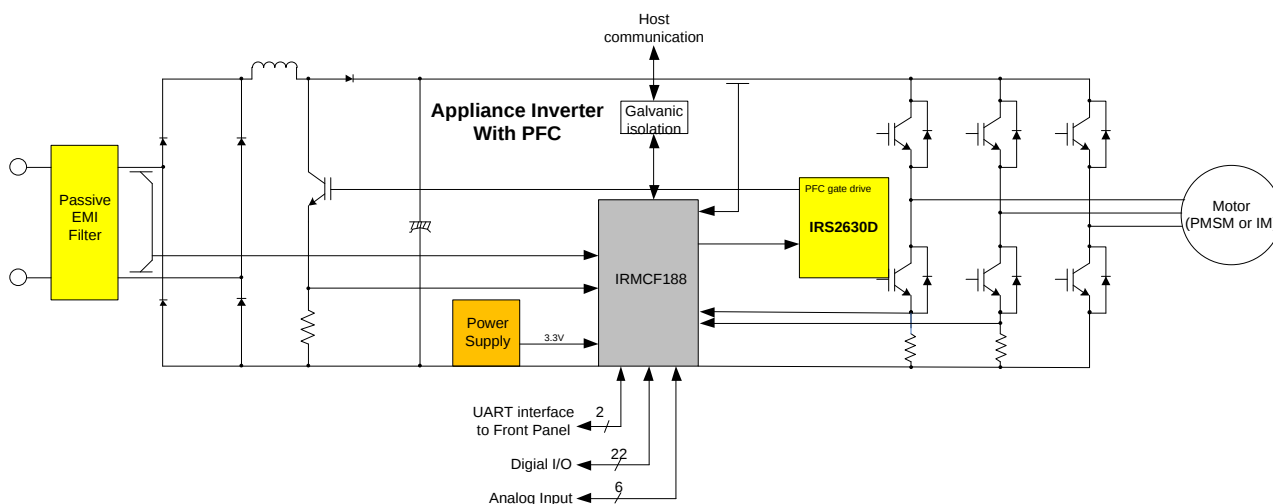
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## 1 Overview

IRMCF188 is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverterized appliance motor control applications. Unlike a traditional microcontroller or DSP, the IRMCF188 provides a built-in closed loop sensorless control algorithm using the unique Flexible Motion Control Engine (MCE™) for permanent magnet motors as well as induction motors. The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCF188 also employs a unique single shunt current reconstruction circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC, while still supporting leg shunt current sensing. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging. Figure 1 shows a typical application schematic using the IRMCF188 in leg shunt mode.

IRMCF188 contains 64K bytes of Flash program memory and comes in a 64-pin QFP package.



**Figure 1. Typical Application Block Diagram Using IRMCF188**

## 2 Pinout

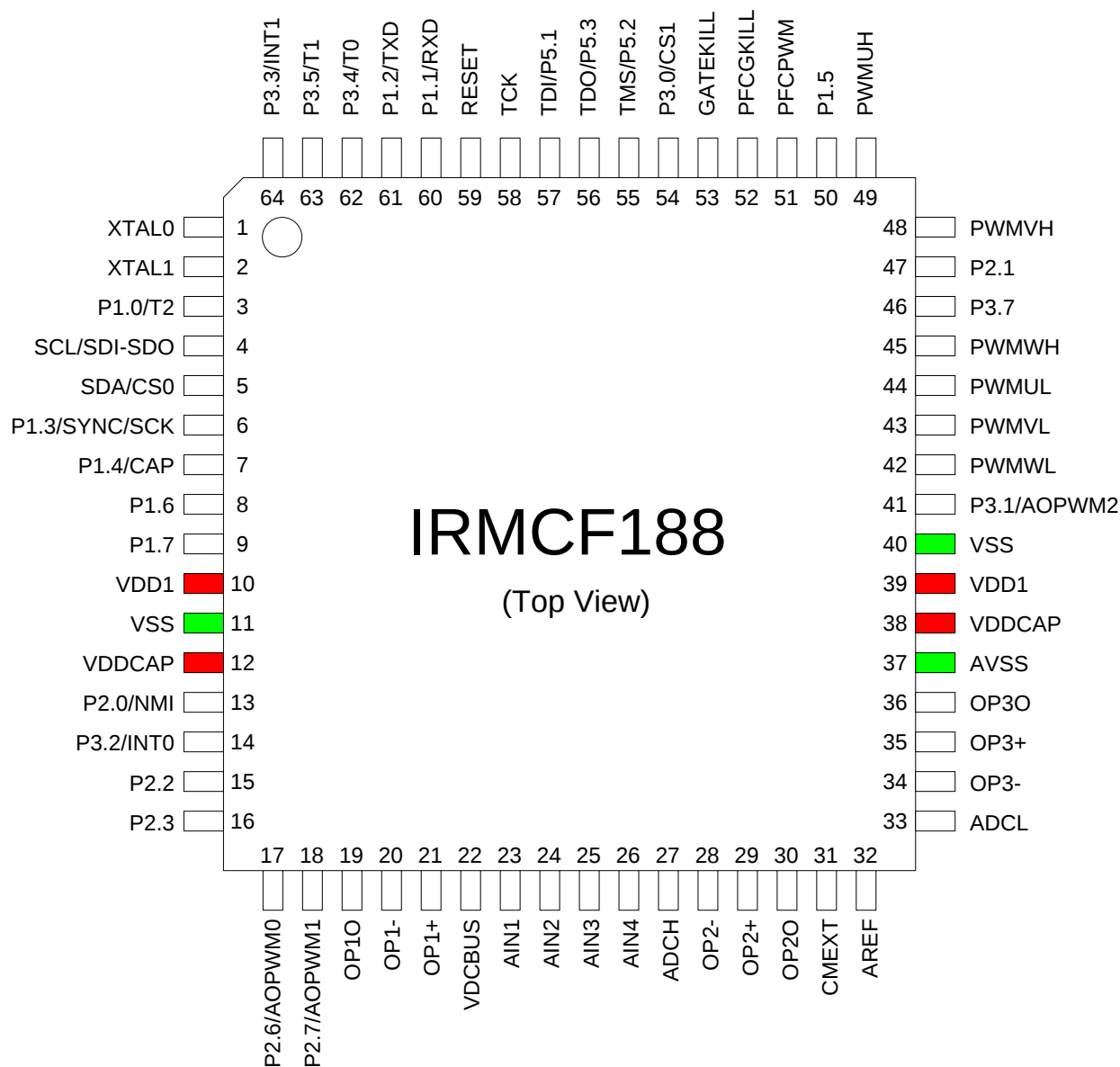
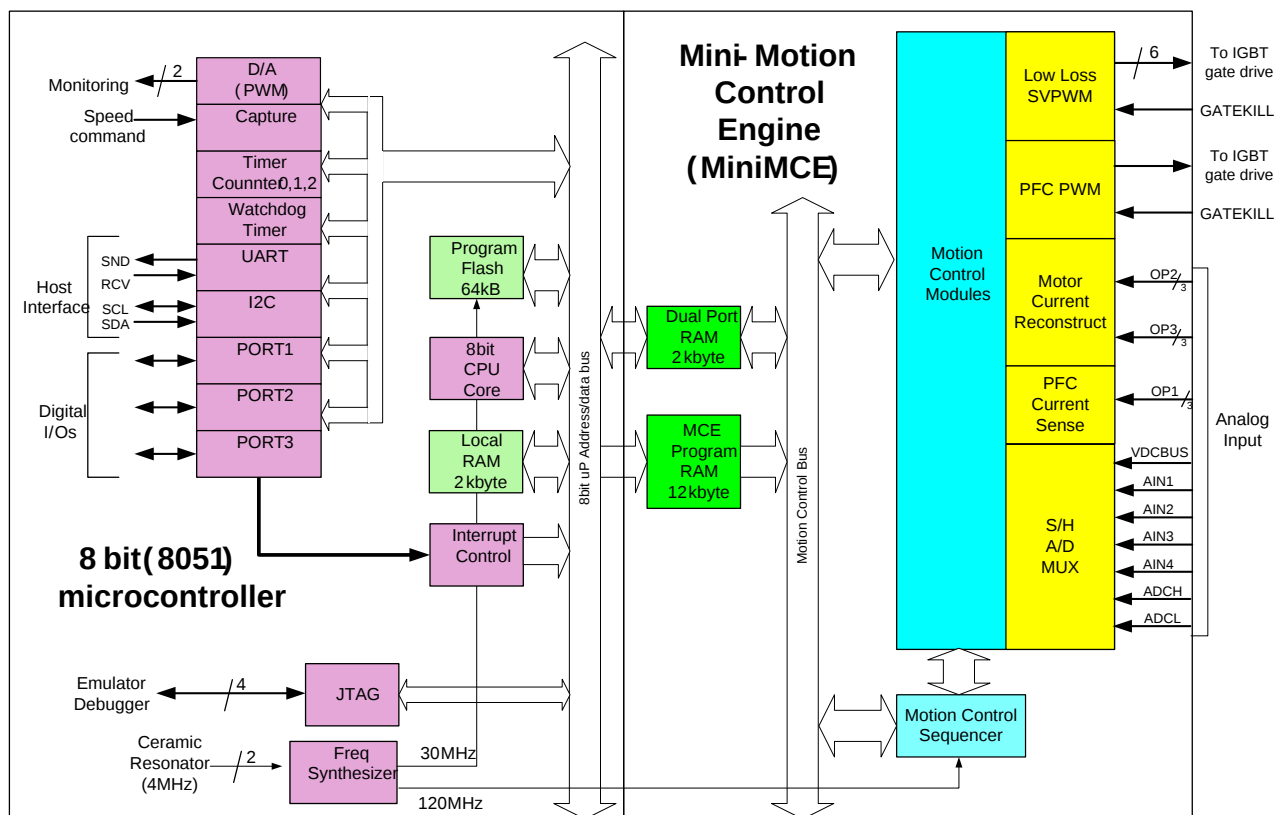


Figure 2. Pinout of IRMCF188

### 3 IRMCF188 Block Diagram and Main Functions

IRMCF188 block diagram for leg shunt mode is shown in Figure 3.



**Figure 3. IRMCF188 Block Diagram**

IRMCF188 contains the following functions for sensorless AC motor control applications:

#### Motion Control Engine (MCE™)

- Sensorless FOC (complete sensorless field oriented control)
- Proportional plus Integral block
- Low pass filter
- Differentiator and lag (high pass filter)
- Ramp
- Limit
- Angle estimate (sensorless control)
- Inverse Clark transformation
- Vector rotator
- Bit latch
- Peak detect
- Transition
- Multiply-divide (signed and unsigned)
- Adder

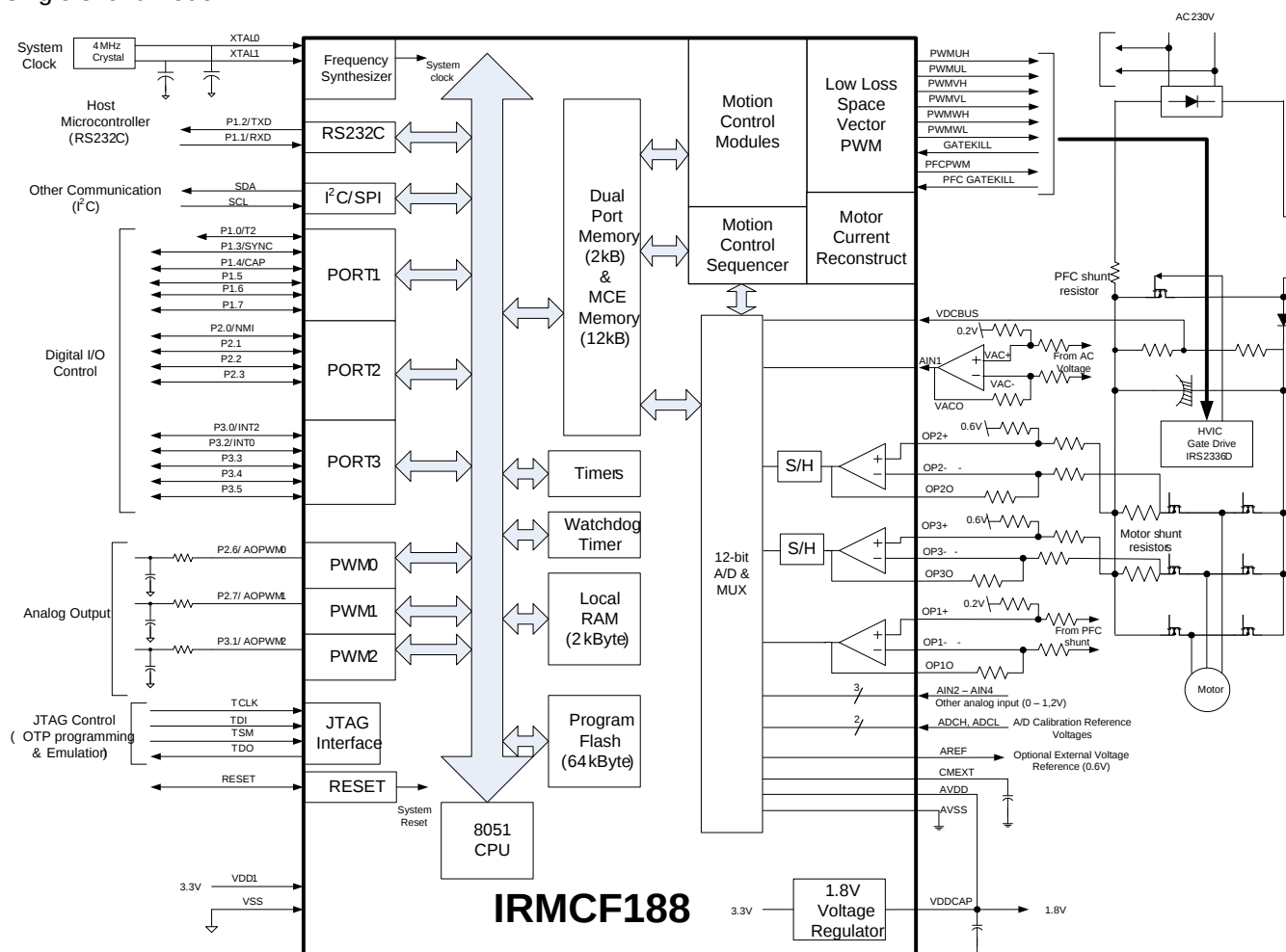
#### 8051 microcontroller

- Two 16 bit timer/counters
- One 16 bit periodic timer
- One 16 bit watchdog timer
- One 16 bit capture timer
- Up to 24 discrete digital I/Os
- Ten-channel 12 bit A/D
  - Buffered (current sensing) three channels (0 – 1.2V input)
  - Unbuffered seven channels (0 – 1.2V input)
- JTAG port (4 pins)
- Up to three channels of analog output (8 bit PWM)
- UART
- I<sup>2</sup>C/SPI port

- |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"><li>• Divide (signed and unsigned)</li><li>• Subtractor</li><li>• Comparator</li><li>• Counter</li><li>• Accumulator</li><li>• Switch</li><li>• Shift</li><li>• ATAN (arc tangent)</li><li>• Function block (any curve fitting, nonlinear function)</li><li>• 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)</li><li>• MCE<sup>TM</sup> program memory and dual port RAM (6K byte)</li><li>• MCE<sup>TM</sup> control sequencer</li></ul> | <ul style="list-style-type: none"><li>• 64K byte Flash memory</li><li>• 2K byte data RAM</li></ul> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|

## 4 Application connection and Pin function

Figure 4 shows the application connections in leg shunt mode. Figure 5 shows the application connections in single shunt mode.



### Figure 4. IRMCF188 Leg Shunt Connection Diagram

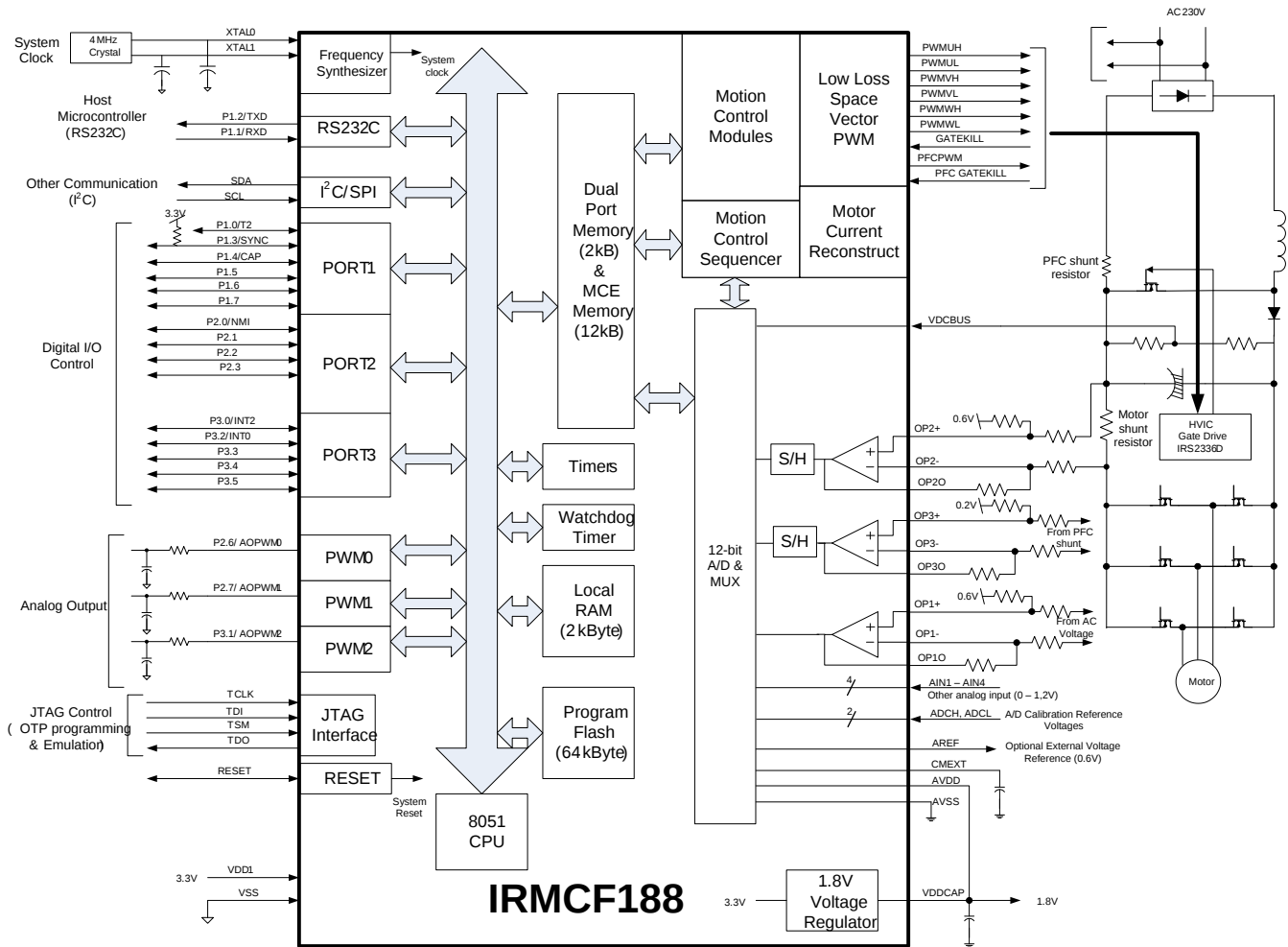


Figure 5. IRMCF188 Single Shunt Connection Diagram

## 4.1 8051 Peripheral Interface Group

### UART Interface

P1.2/TXD Output, Transmit data from IRMCF188  
P1.1/RXD Input, Receive data to IRMCF188

### Discrete I/O Interface

P1.0/T2 Input/output port 1.0, can be configured as Timer/Counter 2 input  
P1.1/RXD Input/output port 1.1, can be configured as RXD input  
P1.2/TXD Input/output port 1.2, can be configured as TXD output  
P1.3/SYNC/SCK Input/output port 1.3, can be configured as SYNC output or SPI clock output  
P1.4/CAP Input/output port 1.4, can be configured as Capture Timer input  
P1.5 Input/output port 1.5  
P1.6 Input/output port 1.6  
P1.7 Input/output port 1.6  
P2.0/NMI Input/output port 2.0, can be configured as non-maskable interrupt input  
P2.2 Input/output port 2.2  
P2.3 Input/output port 2.3  
P2.6/AOPWM0 Input/output port 2.6, can be configured as AOPWM0 output

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| P2.7/AOPWM1   | Input/output port 2.7, can be configured as AOPWM1 output                   |
| P3.0/INT2/CS1 | Input/output port 3.0, can be configured as INT2 input or SPI chip select 1 |
| P3.1/AOPWM2   | Input/output port 3.1, can be configured as AOPWM2 output                   |
| P3.2/NINT0    | Input/output port 3.2, can be configured as INT0 input                      |
| P3.3/NINT1    | Input/output port 3.3, can be configured as INT1 input                      |
| P3.4/T0       | Input/output port 3.4, can be configured as T0 input for counter mode       |
| P3.5/T1       | Input/output port 3.5, can be configured as T1 input for counter mode       |
| P3.7          | Input/output port 3.7                                                       |
| P5.1/TDI      | Input port 5.1, configured as JTAG port by default                          |
| P5.2/TMS      | Input port 5.2, configured as JTAG port by default                          |

#### Analog Output Interface

|             |                                                                                           |
|-------------|-------------------------------------------------------------------------------------------|
| P2.6/AOPWM0 | Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency |
| P2.7/AOPWM1 | Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency |
| P3.1/AOPWM2 | Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency |

#### Crystal Interface

|       |                              |
|-------|------------------------------|
| XTAL0 | Input, connected to crystal  |
| XTAL1 | Output, connected to crystal |

#### Reset Interface

|       |                                                                           |
|-------|---------------------------------------------------------------------------|
| RESET | Input and Output, system reset, doesn't require external RC time constant |
|-------|---------------------------------------------------------------------------|

#### I<sup>2</sup>C Interface

|           |                                                               |
|-----------|---------------------------------------------------------------|
| SCL/SO-SI | Output, I <sup>2</sup> C clock output, or SPI data            |
| SDA/CS0   | Input/output, I <sup>2</sup> C Data line or SPI chip select 0 |

#### I<sup>2</sup>C/SPI Interface

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| SCL/SO-SI     | Output, I <sup>2</sup> C clock output, or SPI data                          |
| SDA/CS0       | Input/output, I <sup>2</sup> C data line or SPI chip select 0               |
| P1.3/SYNC/SCK | Input/output port 1.3, can be configured as SYNC output or SPI clock output |
| P3.0/INT2/CS1 | Input/output port 3.0, can be configured as INT2 input or SPI chip select 1 |

## 4.2 Motion Peripheral Interface Group

#### PWM

|        |                                                                                                               |
|--------|---------------------------------------------------------------------------------------------------------------|
| PWMUH  | Output, PWM phase U high side gate signal, internally pulled down by 58kΩ, configured high true at a power up |
| PWMUL  | Output, PWM phase U low side gate signal, internally pulled down by 58kΩ, configured high true at a power up  |
| PWMVH  | Output, PWM phase V high side gate signal, internally pulled down by 58kΩ, configured high true at a power up |
| PWMVL  | Output, PWM phase V low side gate signal, internally pulled down by 58kΩ, configured high true at a power up  |
| PWMWH  | Output, PWM phase W high side gate signal, internally pulled down by 58kΩ, configured high true at a power up |
| PWMWL  | Output, PWM phase W low side gate signal, internally pulled down by 58kΩ, configured high true at a power up  |
| PFCPWM | Output, PFCPWM output signal, internally pulled up by 70kΩ, configured low true at a power up                 |

**Fault**

|          |                                                                                                  |
|----------|--------------------------------------------------------------------------------------------------|
| GATEKILL | Input, upon assertion this negates all six PWM signals, active low, internally pulled up by 70kΩ |
| PFCGKILL | Input, upon assertion, this negates PFCPWM signal, active low, internally pulled up by 70kΩ      |

**4.3 Analog Interface Group**

|        |                                                                                                                                        |
|--------|----------------------------------------------------------------------------------------------------------------------------------------|
| AVSS   | Analog power return, (analog internal 1.8V power is shared with VDDCAP)                                                                |
| AREF   | 0.6V buffered output                                                                                                                   |
| CMEXT  | Unbuffered 0.6V, input to the AREF buffer, capacitor needs to be connected.                                                            |
| OP1+   | Input, Operational amplifier positive input for application sensing                                                                    |
| OP1-   | Input, Operational amplifier negative input for application sensing                                                                    |
| OP1O   | Output, Operational amplifier output for application sensing                                                                           |
| OP2+   | Input, Operational amplifier positive input for application sensing                                                                    |
| OP2-   | Input, Operational amplifier negative input for application sensing                                                                    |
| OP2O   | Output, Operational amplifier output for application sensing                                                                           |
| OP3+   | Input, Operational amplifier positive input for application sensing                                                                    |
| OP3-   | Input, Operational amplifier negative input for application sensing                                                                    |
| OP3O   | Output, Operational amplifier output for application sensing                                                                           |
| VDCBUS | Input, Analog input channel (0 – 1.2V), allocated for DC bus voltage input                                                             |
| AIN1   | Input, Analog input channel 1 (0 – 1.2V), needs to be pulled down to AVSS if unused                                                    |
| AIN2   | Input, Analog input channel 2 (0 – 1.2V), needs to be pulled down to AVSS if unused                                                    |
| AIN3   | Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused                                                    |
| AIN4   | Input, Analog input channel 4 (0 – 1.2V), needs to be pulled down to AVSS if unused                                                    |
| ADCH   | Input, Analog input channel dedicated for A/D compensation (0 – 1.2V), needs to be pulled down to AVSS if unused                       |
| ADCL   | Input, Analog input channel dedicated for A/D compensation (0 – 1.2V), internally biased to 0.6V, see Figure 23 for internal structure |

| Analog Channel | Leg Shunt Mode        | Single Shunt Mode   | Pin number(s) |
|----------------|-----------------------|---------------------|---------------|
| OP1            | PFC Current           | AC Voltage          | 19, 20, 21    |
| OP2            | Motor U Phase Current | Motor Shunt Current | 28, 29, 30    |
| OP3            | Motor V Phase Current | PFC Current         | 34, 35, 36    |
| AIN1           | AC Voltage            | <i>Unallocated</i>  | 23            |

**Table 1. Analog channel sensing functions in Leg and Single Shunt Modes**
**4.4 Power Interface Group**

|        |                                                                                                                                                                                                                                                    |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD1   | Digital power (3.3V)                                                                                                                                                                                                                               |
| VDDCAP | Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally<br><b>Note:</b> The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin. |
| VSS    | Digital common                                                                                                                                                                                                                                     |

**4.5 Test Interface Group**

|          |                                            |
|----------|--------------------------------------------|
| P5.2/TMS | JTAG test mode input or input digital port |
|----------|--------------------------------------------|

|          |                                        |
|----------|----------------------------------------|
| TDO      | JTAG data output                       |
| P5.1/TDI | JTAG data input, or input digital port |
| TCK      | JTAG test clock                        |

## 5 DC Characteristics

### 5.1 Absolute Maximum Ratings

| Symbol    | Parameter             | Min    | Typ | Max    | Condition       |
|-----------|-----------------------|--------|-----|--------|-----------------|
| $V_{DD1}$ | Supply Voltage        | -0.3 V | -   | 3.6 V  | Respect to VSS  |
| $V_{IA}$  | Analog Input Voltage  | -0.3 V | -   | 1.98 V | Respect to AVSS |
| $V_{ID}$  | Digital Input Voltage | -0.3 V | -   | 6.0 V  | Respect to VSS  |
| $T_A$     | Ambient Temperature   | -40 °C | -   | 125 °C |                 |
| $T_S$     | Storage Temperature   | -65 °C | -   | 150 °C |                 |

**Table 2. Absolute Maximum Ratings**

**Caution:** Stresses beyond those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

### 5.2 System Clock Frequency and Power Consumption

$C_{AREF} = 1nF$ ,  $C_{MEXT} = 100nF$ .  $V_{DD1} = 3.3V$ , Unless specified,  $T_a = 25^{\circ}C$ .

| Symbol | Parameter         | Min | Typ               | Max | Unit |
|--------|-------------------|-----|-------------------|-----|------|
| SYSCLK | System Clock      | 32  | -                 | 120 | MHz  |
| $P_D$  | Power consumption |     | 100 <sup>1)</sup> | -   | mW   |

**Table 3. System Clock Frequency**

Note 1) The value is based on the condition of MCE clock=100MHz, 8051 clock 20MHz with a actual motor and PFC running by a typical MCE application program and 8051 code.

### 5.3 Digital I/O DC Characteristics

| Symbol          | Parameter                 | Min     | Typ         | Max             | Condition               |
|-----------------|---------------------------|---------|-------------|-----------------|-------------------------|
| $V_{DD1}$       | Supply Voltage            | 3.0 V   | 3.3 V       | 3.6 V           | Recommended             |
| $V_{IL}$        | Input Low Voltage         | -0.3 V  | -           | 0.8 V           | Recommended             |
| $V_{IH}$        | Input High Voltage        | 2.0 V   |             | 3.6 V           | Recommended             |
| $C_{IN}$        | Input capacitance         | -       | 3.6 pF      | -               | (1)                     |
| $I_L$           | Input leakage current     |         | $\pm 10$ nA | $\pm 1$ $\mu$ A | $V_O = 3.3$ V or 0 V    |
| $I_{OL1}^{(2)}$ | Low level output current  | 8.9 mA  | 13.2 mA     | 15.2 mA         | $V_{OL} = 0.4$ V<br>(1) |
| $I_{OH1}^{(2)}$ | High level output current | 12.4 mA | 24.8 mA     | 38 mA           | $V_{OH} = 2.4$ V<br>(1) |
| $I_{OL2}^{(3)}$ | Low level output current  | 17.9 mA | 26.3 mA     | 33.4 mA         | $V_{OL} = 0.4$ V<br>(1) |
| $I_{OH2}^{(3)}$ | High level output current | 24.6 mA | 49.5 mA     | 81 mA           | $V_{OH} = 2.4$ V<br>(1) |

**Table 4. Digital I/O DC Characteristics**

Note:

- (1) Data guaranteed by design.
- (2) Applied to SCL/SO-SI, SDA/CS0 pins.
- (3) Applied to all digital I/O pins except SCL/SO-SI and SDA/CS0 pins.

## 5.4 Analog I/O DC Characteristics

- OP amps for application sensing (OP1+, OP1-, OP1O, OP2+, OP2-, OP2O, OP3+, OP3-, OP3O)

$C_{AREF} = 1\text{nF}$ ,  $C_{MEXT} = 100\text{nF}$ .  $V_{DD1} = 3.3\text{V}$ , Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol        | Parameter                     | Min                  | Typ               | Max           | Condition                       |
|---------------|-------------------------------|----------------------|-------------------|---------------|---------------------------------|
| $V_{OFFSET}$  | Input Offset Voltage          | -                    | -                 | 26 mV         | $V_{AVDD} = 1.8\text{ V}$       |
| $V_I$         | Input Voltage Range           | 0 V                  |                   | 1.2 V         | Recommended                     |
| $V_{OUTSW}$   | OP amp output operating range | 50 mV <sup>(1)</sup> | -                 | 1.2 V         | $V_{AVDD} = 1.8\text{ V}$       |
| $C_{IN}$      | Input capacitance             | -                    | 3.6 pF            | -             | (1)                             |
| $R_{FDBK}$    | OP amp feedback resistor      | 5 k $\Omega$         | -                 | 20 k $\Omega$ | Requested between IFBO and IFB- |
| $OP_{GAINCL}$ | Operating Close loop Gain     | 80 db                | -                 | -             | (1)                             |
| CMRR          | Common Mode Rejection Ratio   | -                    | 80 db             | -             | (1)                             |
| $I_{SRC}$     | Op amp output source current  | -                    | 1 mA              | -             | $V_{OUT} = 0.6\text{ V}$<br>(1) |
| $I_{SNK}$     | Op amp output sink current    | -                    | 100 $\mu\text{A}$ | -             | $V_{OUT} = 0.6\text{ V}$<br>(1) |

**Table 5. Analog I/O DC Characteristics**

Note:

(1) Data guaranteed by design.

## 5.5 Under Voltage Lockout DC characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol     | Parameter                     | Min    | Typ    | Max    | Condition |
|------------|-------------------------------|--------|--------|--------|-----------|
| $UV_{CC+}$ | UVcc positive going Threshold | 2.78 V | 3.04 V | 3.23 V | (1)       |
| $UV_{CC-}$ | UVcc negative going Threshold | 2.78 V | 2.97 V | 3.23 V |           |
| $UV_{CCH}$ | UVcc Hysteresys               | -      | 73 mV  | -      | (1)       |

**Table 6. UVcc DC Characteristics**

Note:

(1) Data guaranteed by design.

## 5.6 Itrip comparator DC characteristics

Unless specified,  $V_{DD1}=3.3\text{V}$ ,  $T_a = 25^\circ\text{C}$ .

| Symbol      | Parameter                      | Min | Typ   | Max | Condition                |
|-------------|--------------------------------|-----|-------|-----|--------------------------|
| $I_{trip+}$ | Itrip positive going Threshold | -   | 1.22V | -   | $V_{DD1} = 3.3\text{ V}$ |
| $I_{trip-}$ | Itrip negative going Threshold | -   | 1.10V | -   | $V_{DD1} = 3.3\text{ V}$ |
| $I_{tripH}$ | Itrip Hysteresys               | -   | 120mV | -   |                          |

**Table 7. Itrip DC Characteristics**

## 5.7 CMEXT and AREF Characteristics

$C_{AREF} = 1\text{nF}$ ,  $C_{MEXT} = 100\text{nF}$ . Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol       | Parameter                        | Min    | Typ    | Max    | Condition                 |
|--------------|----------------------------------|--------|--------|--------|---------------------------|
| $V_{CM}$     | CMEXT voltage                    | 495 mV | 600 mV | 700 mV | $V_{VDD1} = 3.3\text{ V}$ |
| $V_{AREF}$   | Buffer Output Voltage            | 495 mV | 600 mV | 700 mV | $V_{VDD1} = 3.3\text{ V}$ |
| $\Delta V_o$ | Load regulation ( $V_{DC}-0.6$ ) | -      | 1 mV   | -      | (1)                       |
| PSRR         | Power Supply Rejection Ratio     | -      | 75 db  | -      | (1)                       |

**Table 8. CMEXT and AREF DC Characteristics**

Note:

(1) Data guaranteed by design.

## 6 AC Characteristics

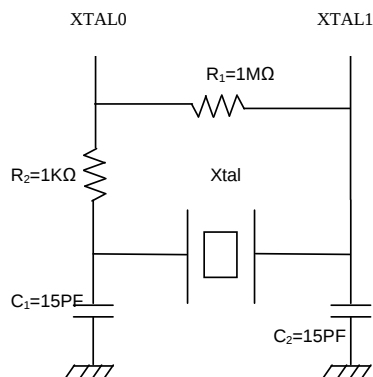
### 6.1 Digital PLL AC Characteristics

| Symbol      | Parameter                   | Min                  | Typ      | Max           | Condition                            |
|-------------|-----------------------------|----------------------|----------|---------------|--------------------------------------|
| $F_{CLKIN}$ | Crystal input frequency     | 3.2 MHz              | 4 MHz    | 60 MHz        | <sup>(1)</sup><br>(see figure below) |
| $F_{PLL}$   | Internal clock frequency    | 32 MHz               | 50 MHz   | 128 MHz       | <sup>(1)</sup>                       |
| $F_{LWPPW}$ | Sleep mode output frequency | $F_{CLKIN} \div 256$ | -        | -             | <sup>(1)</sup>                       |
| $J_S$       | Short time jitter           | -                    | 200 psec | -             | <sup>(1)</sup>                       |
| $D$         | Duty cycle                  | -                    | 50 %     | -             | <sup>(1)</sup>                       |
| $T_{LOCK}$  | PLL lock time               | -                    | -        | 500 $\mu$ sec | <sup>(1)</sup>                       |

**Table 9. PLL AC Characteristics**

Note:

(1) Data guaranteed by design.



**Figure 6. Crystal circuit example**

## 6.2 Analog to Digital Converter AC Characteristics

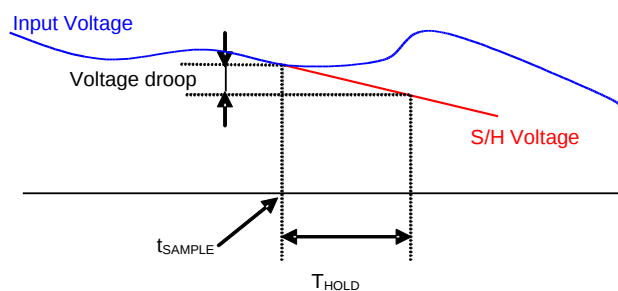
Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol            | Parameter                     | Min | Typ | Max                  | Condition                                         |
|-------------------|-------------------------------|-----|-----|----------------------|---------------------------------------------------|
| $T_{\text{CONV}}$ | Conversion time               | -   | -   | 2.05 $\mu\text{sec}$ | (1)                                               |
| $T_{\text{HOLD}}$ | Sample/Hold maximum hold time | -   | -   | 10 $\mu\text{sec}$   | Voltage droop $\leq 15$ LSB<br>(see figure below) |

**Table 10 . A/D Converter AC Characteristics**

Note:

(1) Data guaranteed by design.



**Figure 7. Voltage droop and S/H hold time**

### 6.3 Op amp AC Characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

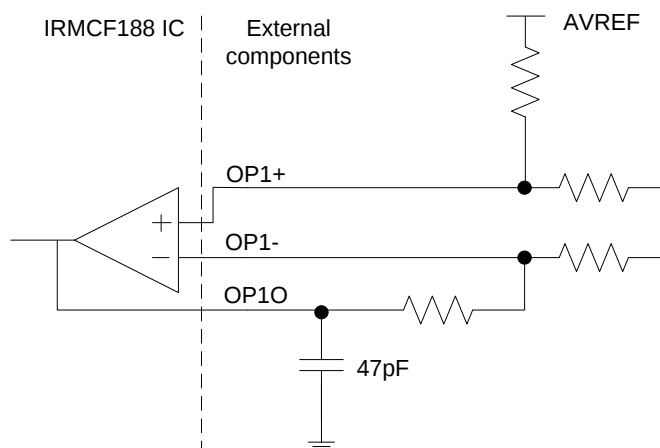
| Symbol     | Parameter          | Min | Typ                   | Max | Condition                                                     |
|------------|--------------------|-----|-----------------------|-----|---------------------------------------------------------------|
| $OP_{SR}$  | OP amp slew rate   | -   | 10 V/ $\mu\text{sec}$ | -   | $V_{DD1} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup> |
| $OP_{IMP}$ | OP input impedance | -   | $10^8\ \Omega$        | -   | <sup>(1)</sup> <sup>(2)</sup>                                 |
| $T_{SET}$  | Settling time      | -   | 400 ns                | -   | $V_{DD1} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup> |

**Table 11 Current Sensing OP Amp AC Characteristics**

Note:

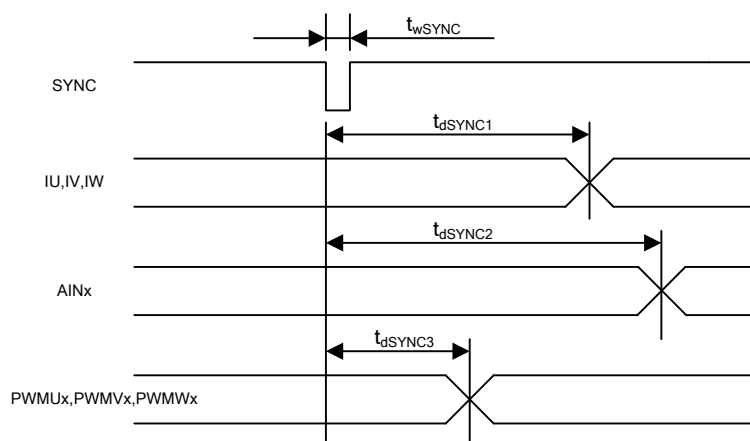
(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 8. Here only Op-amp 1 is shown but all op amp outputs should be loaded with this capacitor value.



**Figure 8 Op amp output capacitor**

## 6.4 SYNC to SVPWM and A/D Conversion AC Timing



**Figure 9. SYNC timing**

Unless specified, Ta = 25°C.

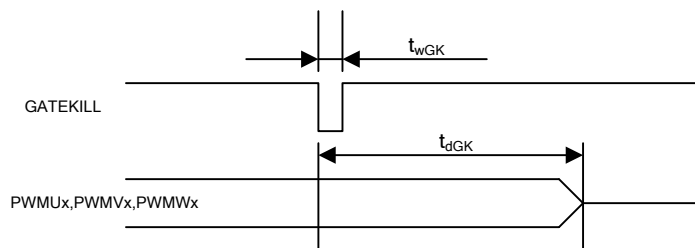
| Symbol              | Parameter                                               | Min | Typ | Max | Unit                  |
|---------------------|---------------------------------------------------------|-----|-----|-----|-----------------------|
| $t_{w\text{SYNC}}$  | SYNC pulse width                                        | -   | 32  | -   | SYSCLK                |
| $t_{d\text{SYNC1}}$ | SYNC to current feedback conversion time                | -   | -   | 100 | SYSCLK                |
| $t_{d\text{SYNC2}}$ | SYNC to AIN0-4, ADCH, ADCL analog input conversion time | -   | -   | 200 | SYSCLK <sup>(1)</sup> |
| $t_{d\text{SYNC3}}$ | SYNC to PWM output delay time                           | -   | -   | 2   | SYSCLK                |

**Table 12. SYNC AC Characteristics**

Note:

(1) AIN2 – AIN4, ADCH, ADCL channels are converted once every 5 SYNC events

## 6.5 GATEKILL to SVPWM AC Timing



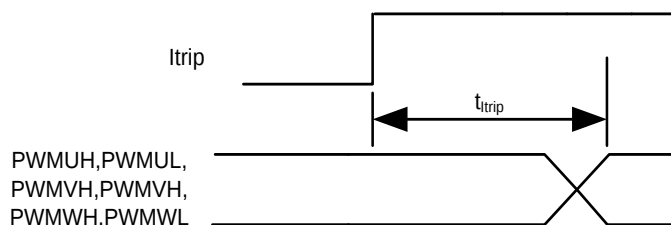
**Figure 10. Gatekill timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol    | Parameter                    | Min | Typ | Max | Unit  |
|-----------|------------------------------|-----|-----|-----|-------|
| $t_{wGK}$ | GATEKILL pulse width         | 32  | -   | -   | SYCLK |
| $t_{dGK}$ | GATEKILL to PWM output delay | -   | -   | 100 | SYCLK |

**Table 13. GATEKILL to SVPWM AC Timing**

## 6.6 Itrip AC Timing



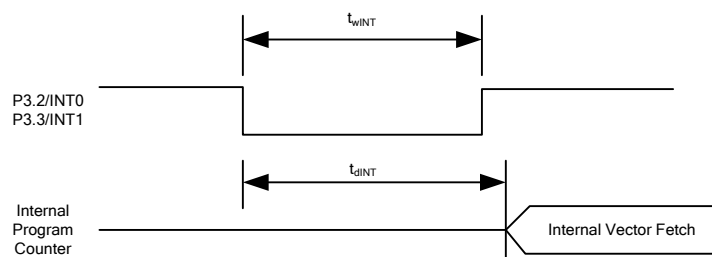
**Figure 11. ITRIP timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol      | Parameter               | Min | Typ | Max                                   | Unit       |
|-------------|-------------------------|-----|-----|---------------------------------------|------------|
| $t_{ITRIP}$ | Itrip propagation delay | -   | -   | $100(\text{sysclk}) + 1.0\text{usec}$ | SYCLK+usec |

**Table 14. Itrip AC Timing**

## 6.7 Interrupt AC Timing



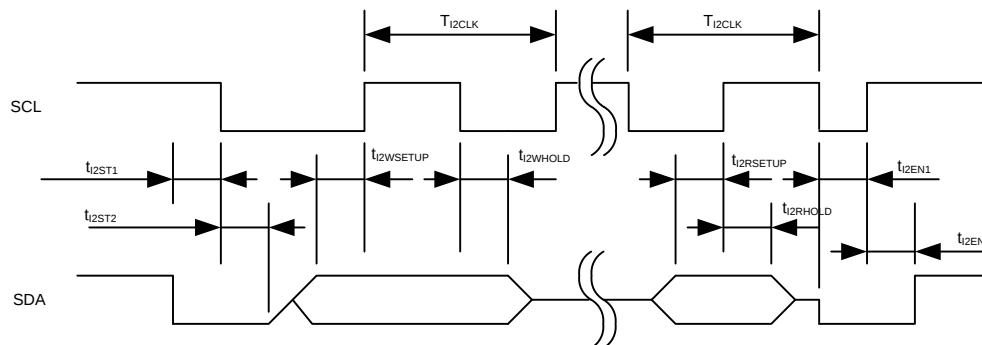
**Figure 12. Interrupt timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol     | Parameter                           | Min | Typ | Max | Unit   |
|------------|-------------------------------------|-----|-----|-----|--------|
| $t_{WINT}$ | INT0, INT1 Interrupt Assertion Time | 4   | -   | -   | SYSCLK |
| $t_{dINT}$ | INT0, INT1 latency                  | -   | -   | 4   | SYSCLK |

**Table 15. Interrupt AC Timing**

## 6.8 I<sup>2</sup>C AC Timing



**Figure 13. I<sup>2</sup>C Timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                         | Min                                         | Typ | Max  | Unit        |
|----------------|-----------------------------------|---------------------------------------------|-----|------|-------------|
| $T_{I2CLK}$    | I <sup>2</sup> C clock period     | 10                                          | -   | 8192 | SYCLK       |
| $t_{I2ST1}$    | I <sup>2</sup> C SDA start time   | 0.25                                        | -   | -    | $T_{I2CLK}$ |
| $t_{I2ST2}$    | I <sup>2</sup> C SCL start time   | 0.25                                        | -   | -    | $T_{I2CLK}$ |
| $t_{I2WSETUP}$ | I <sup>2</sup> C write setup time | 0.25                                        | -   | -    | $T_{I2CLK}$ |
| $t_{I2WHOLD}$  | I <sup>2</sup> C write hold time  | 0.25                                        | -   | -    | $T_{I2CLK}$ |
| $t_{I2RSETUP}$ | I <sup>2</sup> C read setup time  | I <sup>2</sup> C filter time <sup>(1)</sup> |     | -    | SYCLK       |
| $t_{I2RHOLD}$  | I <sup>2</sup> C read hold time   | 1                                           | -   | -    | SYCLK       |

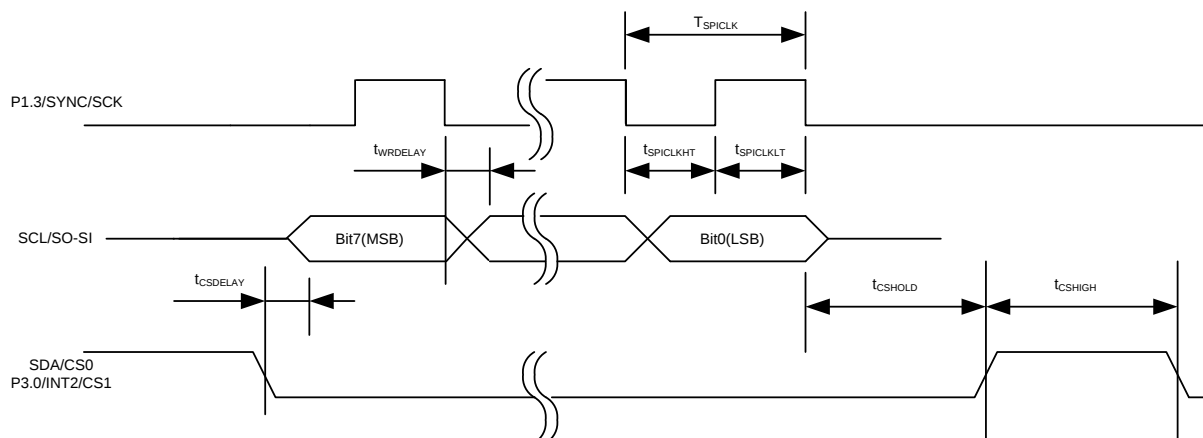
**Table 16. I<sup>2</sup>C AC Timing**

Note:

- (1) I<sup>2</sup>C read setup time is determined by the programmable filter time applied to I<sup>2</sup>C communication.

## 6.9 SPI AC Timing

### 6.9.1.1 SPI Write AC timing



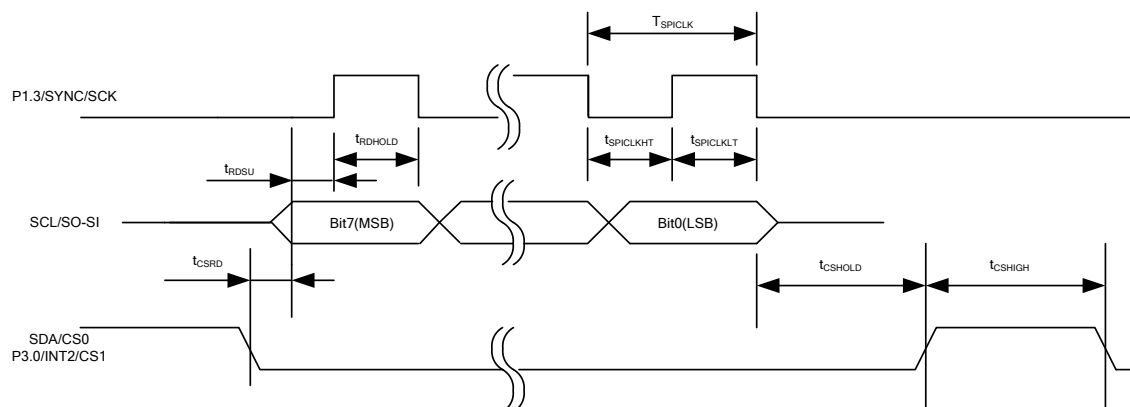
**Figure 14. SPI write timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol                | Parameter                                          | Min | Typ | Max | Unit                |
|-----------------------|----------------------------------------------------|-----|-----|-----|---------------------|
| $T_{\text{SPICLK}}$   | SPI clock period                                   | 4   | -   | -   | $\text{SYSCLK}$     |
| $t_{\text{SPICLKHT}}$ | SPI clock high time                                | -   | 1/2 | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{SPICLKLT}}$ | SPI clock low time                                 | -   | 1/2 | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{CSDELAY}}$  | CS to data delay time                              | -   | -   | 10  | nsec                |
| $t_{\text{WRDELAY}}$  | CLK falling edge to data delay time                | -   | -   | 10  | nsec                |
| $t_{\text{CSHIGH}}$   | CS high time between two consecutive byte transfer | 1   | -   | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{CSHOLD}}$   | CS hold time                                       | -   | 1   | -   | $T_{\text{SPICLK}}$ |

**Table 17. SPI Write AC Timing**

### 6.9.1.2 SPI Read AC Timing



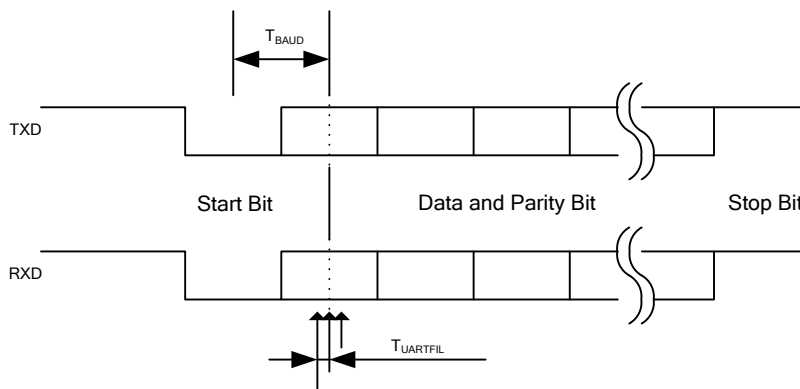
**Figure 15. SPI read timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol                | Parameter                                          | Min | Typ | Max | Unit                |
|-----------------------|----------------------------------------------------|-----|-----|-----|---------------------|
| $T_{\text{SPICLK}}$   | SPI clock period                                   | 4   | -   | -   | SYSCLK              |
| $t_{\text{SPICLKHT}}$ | SPI clock high time                                | -   | 1/2 | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{SPICLKLT}}$ | SPI clock low time                                 | -   | 1/2 | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{CSRD}}$     | CS to data delay time                              | -   | -   | 10  | nsec                |
| $t_{\text{RDSU}}$     | SPI read data setup time                           | 10  | -   | -   | nsec                |
| $t_{\text{RDHOLD}}$   | SPI read data hold time                            | 10  | -   | -   | nsec                |
| $t_{\text{CSHIGH}}$   | CS high time between two consecutive byte transfer | 1   | -   | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{CSHOLD}}$   | CS hold time                                       | -   | 1   | -   | $T_{\text{SPICLK}}$ |

**Table 18. SPI Read AC Timing**

## 6.10 UART AC Timing



**Figure 16. UART timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

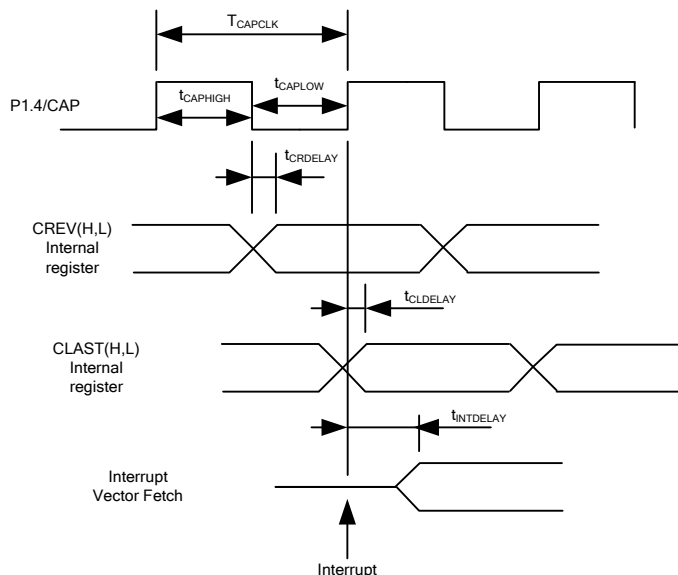
| Symbol        | Parameter                                  | Min | Typ   | Max | Unit       |
|---------------|--------------------------------------------|-----|-------|-----|------------|
| $T_{BAUD}$    | Baud Rate Period                           | -   | 57600 | -   | bit/sec    |
| $T_{UARTFIL}$ | UART sampling filter period <sup>(1)</sup> | -   | 1/16  | -   | $T_{BAUD}$ |

**Table 19. UART AC Timing**

Note:

- (1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of  $1/16 T_{BAUD}$ . If three sampled values do not agree, then UART noise error is generated.

## 6.11 CAPTURE Input AC Timing



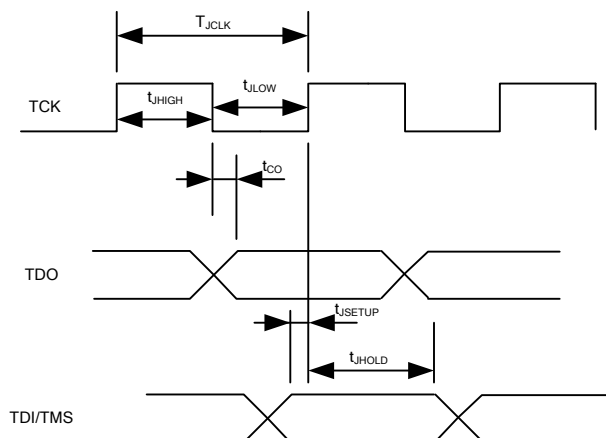
**Figure 17. CAPTURE timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                                           | Min | Typ | Max | Unit    |
|----------------|-----------------------------------------------------|-----|-----|-----|---------|
| $T_{CAPCLK}$   | CAPTURE input period                                | 8   | -   | -   | SYSCCLK |
| $t_{CAPHIGH}$  | CAPTURE input high time                             | 4   | -   | -   | SYSCCLK |
| $t_{CAPLOW}$   | CAPTURE input low time                              | 4   | -   | -   | SYSCCLK |
| $t_{CRDELAY}$  | CAPTURE falling edge to capture register latch time | -   | -   | 4   | SYSCCLK |
| $t_{CLDELAY}$  | CAPTURE rising edge to capture register latch time  | -   | -   | 4   | SYSCCLK |
| $t_{INTDELAY}$ | CAPTURE input interrupt latency time                | -   | -   | 4   | SYSCCLK |

**Table 20. CAPTURE AC Timing**

## 6.12 JTAG AC Timing



**Figure 18. JTAG timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol       | Parameter                         | Min | Typ | Max | Unit |
|--------------|-----------------------------------|-----|-----|-----|------|
| $T_{JCLK}$   | TCK Period                        | -   | -   | 50  | MHz  |
| $t_{JHIGH}$  | TCK High Period                   | 10  | -   | -   | nsec |
| $t_{JLOW}$   | TCK Low Period                    | 10  | -   | -   | nsec |
| $t_{CO}$     | TCK to TDO propagation delay time | 0   | -   | 5   | nsec |
| $t_{JSETUP}$ | TDI/TMS setup time                | 4   | -   | -   | nsec |
| $t_{JHOLD}$  | TDI/TMS hold time                 | 0   | -   | -   | nsec |

**Table 21. JTAG AC Timing**

## 7 I/O Structure

The following figure shows the PWM output (PWMUH/PWMUL/PWMVH/PWMVL/PWMWH/PWMWL/PFCPWM)

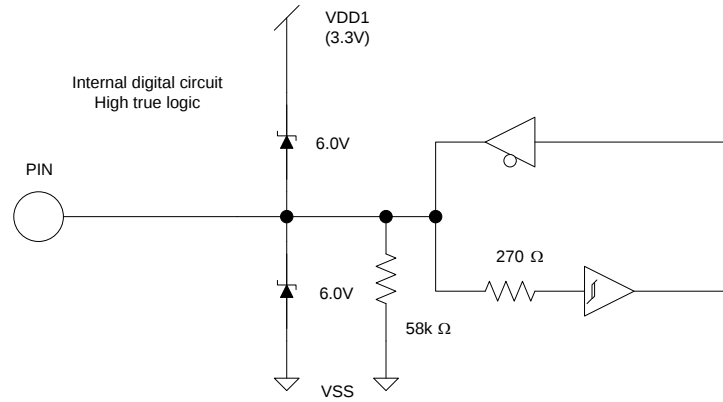


Figure 19. PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH/PFCPWM output

The following figure shows the digital I/O structure except the PWM output

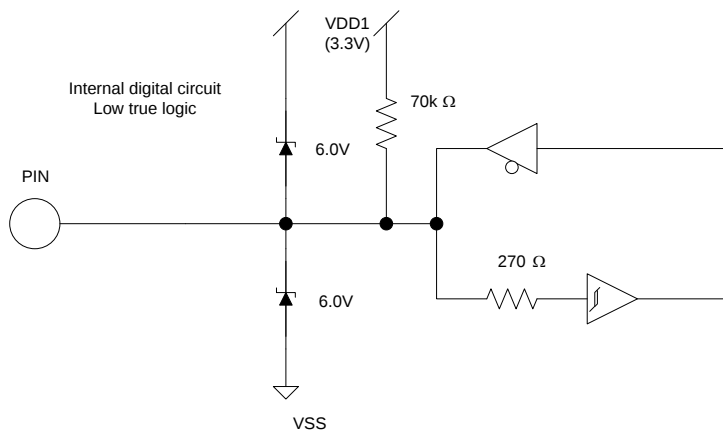
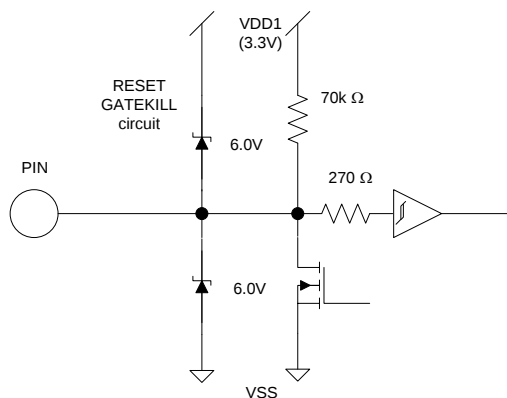


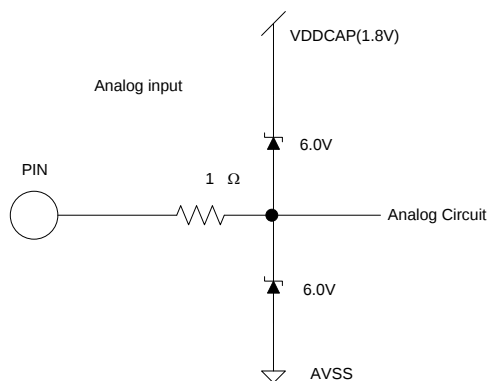
Figure 20. All digital I/O except PWM output

The following figure shows RESET and GATEKILL I/O structure.



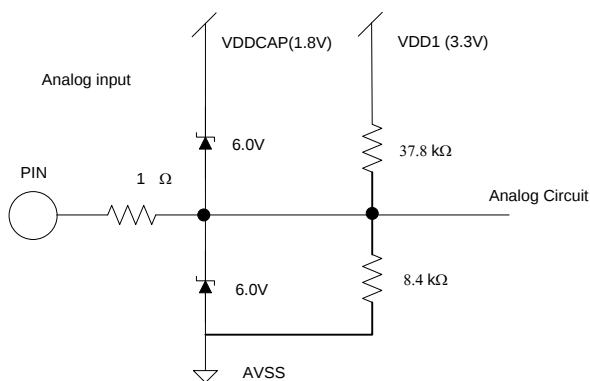
**Figure 21. RESET, GATEKILL I/O**

The following figure shows the analog input structure, except for ADCL.



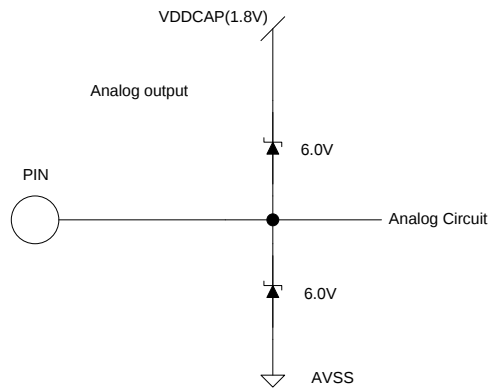
**Figure 22. Analog input**

The following figure shows the ADCL input structure.



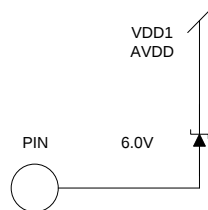
**Figure 23. ADCL pin input structure**

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.



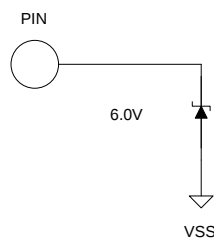
**Figure 24 Analog operational amplifier output and AREF I/O structure**

The following figure shows the VSS,AVSS pin I/O structure



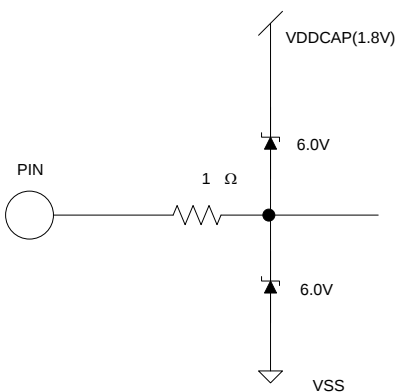
**Figure 25. VSS,AVSS pin I/O structure**

The following figure shows the VDD1,VDDCAP pin I/O structure



**Figure 26. VDD1,VDDCAP pin I/O structure**

The following figure shows the XTAL0 and XTAL1 pins structure



**Figure 27. XTAL0/XTAL1 pins structure**

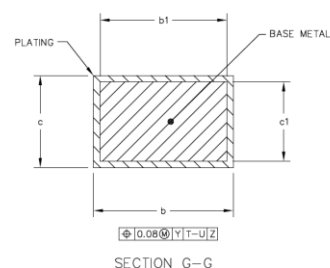
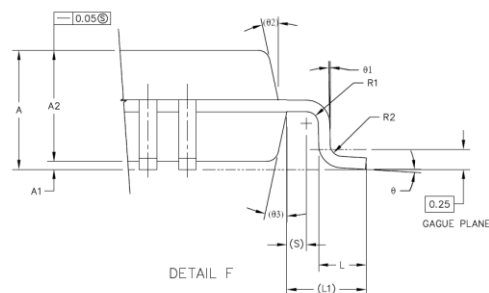
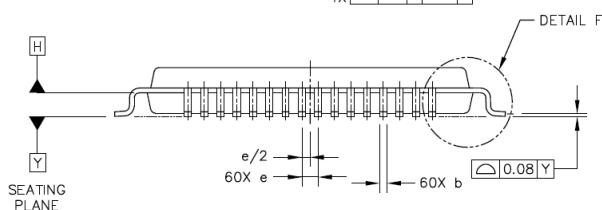
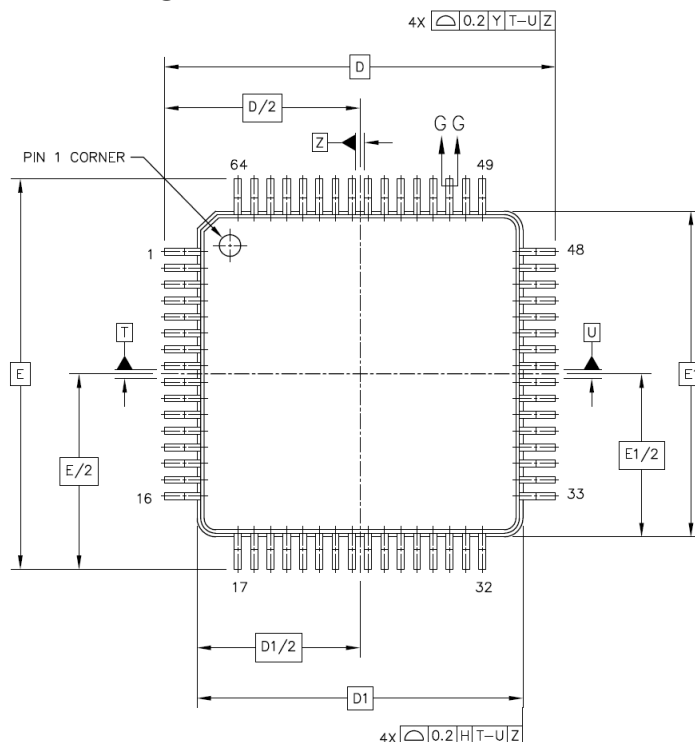
## 8 Pin List

| Pin Number | Pin Name      | Internal Pull-up /Pull-down | Pin Type | Description                                                                                                      |
|------------|---------------|-----------------------------|----------|------------------------------------------------------------------------------------------------------------------|
| 1          | XTAL0         |                             | I        | Crystal input                                                                                                    |
| 2          | XTAL1         |                             | O        | Crystal output                                                                                                   |
| 3          | P1.0/T2       |                             | I/O      | Discrete programmable I/O or Timer/Counter 2 input                                                               |
| 4          | SCL/SO-SI     |                             | I/O      | I <sup>2</sup> C clock output (open drain, need pull up) or SPI data                                             |
| 5          | SDA/CS0       |                             | I/O      | I <sup>2</sup> C data (open drain, need pull up) or SPI Chip Select 0                                            |
| 6          | P1.3/SYNC/SCK |                             | I/O      | Discrete programmable I/O or SYNC output or SPI clock output                                                     |
| 7          | P1.4/CAP      |                             | I/O      | Discrete programmable I/O or Capture timer input                                                                 |
| 8          | P1.6          |                             | I/O      | Discrete programmable I/O                                                                                        |
| 9          | P1.7          |                             |          | Discrete programmable I/O                                                                                        |
| 10         | VDD1          |                             | P        | 3.3V digital power                                                                                               |
| 11         | VSS           |                             | P        | Digital common                                                                                                   |
| 12         | VDDCAP        |                             | P        | Internal 1.8V output, Capacitor(s) to be connected                                                               |
| 13         | P2.0/NMI      |                             | I/O      | Discrete programmable I/O or Non-maskable Interrupt input                                                        |
| 14         | P3.2/INT0     |                             | I/O      | Discrete programmable I/O or Interrupt 0 input                                                                   |
| 15         | P2.2          |                             | I/O      | Discrete programmable I/O                                                                                        |
| 16         | P2.3          |                             | I/O      | Discrete programmable I/O                                                                                        |
| 17         | P2.6/AOPWM0   |                             | I/O      | Discrete programmable I/O or PWM 0 digital output                                                                |
| 18         | P2.7/AOPWM1   |                             | I/O      | Discrete programmable I/O or PWM 1 digital output                                                                |
| 19         | OP1O          |                             | O        | Op amp output for application sensing, 0-1.2V range                                                              |
| 20         | OP1-          |                             | I        | Op amp negative input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused           |
| 21         | OP1+          |                             | I        | Op amp positive input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused           |
| 22         | VDCBUS        |                             | I        | Analog input channel (0 – 1.2V), allocated for DC bus voltage input, needs to be pulled down to AVSS if unused   |
| 23         | AIN1          |                             | I        | Analog input channel 1, 0-1.2V range, needs to be pulled down to AVSS if unused                                  |
| 24         | AIN2          |                             | I        | Analog input channel 2, 0-1.2V range, needs to be pulled down to AVSS if unused                                  |
| 25         | AIN3          |                             | I        | Analog input channel 3, 0-1.2V range, needs to be pulled down to AVSS if unused                                  |
| 26         | AIN4          |                             | I        | Analog input channel 4, 0-1.2V range, needs to be pulled down to AVSS if unused                                  |
| 27         | ADCH          |                             | I        | Input, Analog input channel dedicated for A/D compensation (0 – 1.2V), needs to be pulled down to AVSS if unused |
| 28         | OP2-          |                             | I        | Op amp negative input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused           |
| 29         | OP2+          |                             | I        | Op amp positive input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused           |
| 30         | OP2O          |                             | O        | Op amp output for application sensing, 0-1.2V range                                                              |
| 31         | CMEXT         |                             | O        | Unbuffered 0.6V output. Capacitor needs to be connected.                                                         |
| 32         | AREF          |                             | O        | Analog reference voltage output (0.6V)                                                                           |

| Pin Number | Pin Name      | Internal Pull-up /Pull-down | Pin Type | Description                                                                                                                            |
|------------|---------------|-----------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------|
| 33         | ADCL          |                             | I        | Input, Analog input channel dedicated for A/D compensation (0 – 1.2V), internally biased to 0.6V, see Figure 23 for internal structure |
| 34         | OP3-          |                             | I        | Op amp negative input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused                                 |
| 35         | OP3+          |                             | I        | Op amp positive input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused                                 |
| 36         | OP3O          |                             | O        | Op amp output for application sensing, 0-1.2V range                                                                                    |
| 37         | AVSS          |                             | P        | Analog common                                                                                                                          |
| 38         | VDDCAP        |                             | P        | Internal 1.8V output, Capacitor(s) to be connected                                                                                     |
| 39         | VDD1          |                             | P        | 3.3V digital power                                                                                                                     |
| 40         | VSS           |                             | P        | Digital common                                                                                                                         |
| 41         | P3.1/AOPWM2   |                             | I/O      | Discrete programmable I/O or PWM 2 digital output                                                                                      |
| 42         | PWMWL         | 58 kΩ Pull down             | O        | PWM gate drive for phase W low side, configurable either high or low true.                                                             |
| 43         | PWMVL         | 58 kΩ Pull down             | O        | PWM gate drive for phase V low side, configurable either high or low true                                                              |
| 44         | PWMUL         | 58 kΩ Pull down             | O        | PWM gate drive for phase U low side, configurable either high or low true                                                              |
| 45         | PWMWH         | 58 kΩ Pull down             | O        | PWM gate drive for phase W high side, configurable either high or low true                                                             |
| 46         | P3.7          |                             | I/O      | Discrete programmable I/O                                                                                                              |
| 47         | P2.1          |                             | I/O      | Discrete programmable I/O                                                                                                              |
| 48         | PWMVH         | 58 kΩ Pull down             | O        | PWM gate drive for phase V high side, configurable either high or low true                                                             |
| 49         | PWMUH         | 58 kΩ Pull down             | O        | PWM gate drive for phase U high side, configurable either high or low true                                                             |
| 50         | P1.5          |                             | I/O      | Discrete programmable I/O.                                                                                                             |
| 51         | PFCPWM        |                             | I/O      | PFC PWM gate drive , configurable either high or low                                                                                   |
| 52         | PFCGKILL      | 70 kΩ Pull up               | I        | PFCPWM shutdown input, active low input.                                                                                               |
| 53         | GATEKILL      | 70 kΩ Pull up               | I        | PWM shutdown input, configurable digital filter, active low input.                                                                     |
| 54         | P3.0/INT2/CS1 | 70 kΩ Pull up               | I/O      | Discrete programmable I/O or external interrupt 2 input or SPI Chip Select 1                                                           |
| 55         | P5.2/TMS      |                             | I        | JTAG test mode select or digital input port                                                                                            |
| 56         | TDO           |                             | O        | JTAG test data output                                                                                                                  |
| 57         | P5.1/TDI      |                             | I        | JTAG test data input or digital input port                                                                                             |
| 58         | TCK           |                             | I        | JTAG test clock                                                                                                                        |
| 59         | RESET         |                             | I        | Reset, low true, Schmitt trigger input                                                                                                 |
| 60         | P1.1/RXD      |                             | I/O      | UART receiver input or Discrete programmable I/O                                                                                       |
| 61         | P1.2/TXD      |                             | I/O      | UART transmitter output or Discrete programmable I/O                                                                                   |
| 62         | P3.4/T0       |                             | I/O      | Discrete programmable I/O or Timer/Counter 2 input                                                                                     |
| 63         | P3.5/T1       |                             | I/O      | Discrete programmable I/O or Timer/Counter 2 input                                                                                     |
| 64         | P3.3/INT1     |                             | I/O      | Interrupt 1 input or Discrete I/O                                                                                                      |

**Table 22. Pin List**

## 9 Package Dimensions

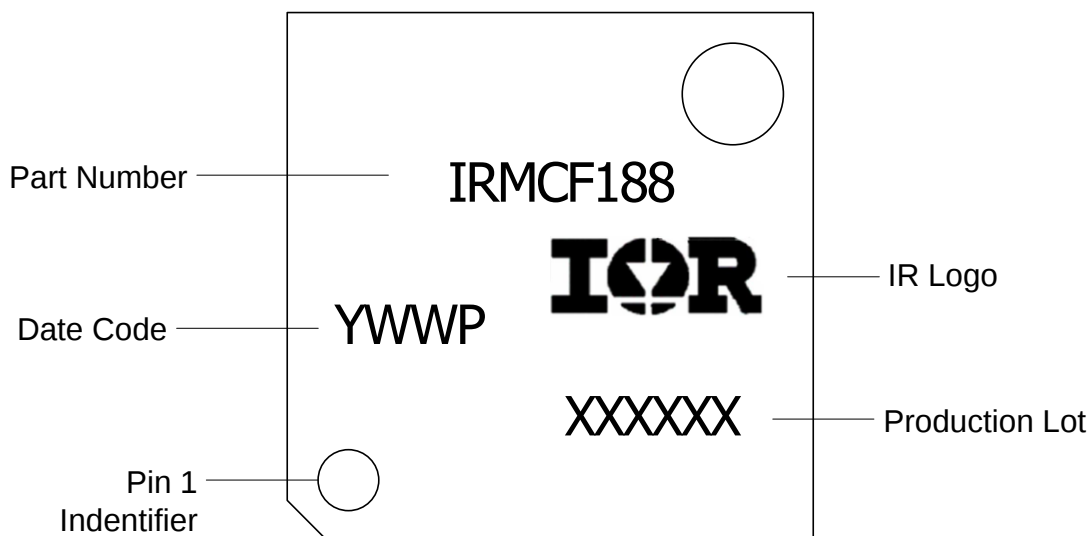


### NOTES:

- DIMENSIONS ARE IN MILLIMETERS.
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
- DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE Y.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

| DIM | MIN     | MAX  | DIM | MIN     | MAX | DIM | MIN | MAX |
|-----|---------|------|-----|---------|-----|-----|-----|-----|
| A   | ---     | 1.6  | L1  | 1 REF   |     |     |     |     |
| A1  | 0.05    | 0.15 | R1  | 0.1     | 0.2 |     |     |     |
| A2  | 1.35    | 1.45 | R2  | 0.1     | 0.2 |     |     |     |
| b   | 0.17    | 0.27 | S   | 0.2 REF |     |     |     |     |
| b1  | 0.17    | 0.23 | θ   | 0°      | 7°  |     |     |     |
| c   | 0.09    | 0.2  | θ1  | 0°      | --- |     |     |     |
| c1  | 0.09    | 0.16 | θ2  | 12° REF |     |     |     |     |
| D   | 12 BSC  |      | θ3  | 12° REF |     |     |     |     |
| D1  | 10 BSC  |      |     |         |     |     |     |     |
| e   | 0.5 BSC |      |     |         |     |     |     |     |
| E   | 12 BSC  |      |     |         |     |     |     |     |
| E1  | 10 BSC  |      |     |         |     |     |     |     |
| L   | 0.45    | 0.75 |     |         |     |     |     |     |

## 10 Part Marking Information



## 11 Qualification Information

|                                   |                         |                                                       |
|-----------------------------------|-------------------------|-------------------------------------------------------|
| <b>Qualification Level</b>        |                         | Industrial <sup>††</sup><br>(per JEDEC JESD 47E)      |
| <b>Moisture Sensitivity Level</b> |                         | MSL3 <sup>†††</sup><br>(per IPC/JEDEC J-STD-020C)     |
| <b>ESD</b>                        | <b>Machine Model</b>    | Class B<br>(per JEDEC standard JESD22-A114D)          |
|                                   | <b>Human Body Model</b> | Class 2<br>(per EIA/JEDEC standard EIA/JESD22-A115-A) |
| <b>RoHS Compliant</b>             |                         | Yes                                                   |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Note:** Test condition for Temperature Cycling test is -40C to 125C.

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Data and Specifications are subject to change without notice

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