USB Transceiver

General Description

The MIC2551A is a single chip transceiver that complies with the physical layer specifications of the Universal Serial Bus (USB) 2.0. It supports both full speed (12Mbps) and low speed (1.5Mbps) operation and introduces superior edge rate control, producing crisper eye diagrams, which ease the task of passing USB compliance testing.

A unique, patented, dual supply voltage operation allows the MIC2551A to reference the system I/F I/O signals to a supply voltage down to 1.6V while independently powered by the USB V_{BUS}. This allows the system interface to operate at its core voltage without addition of buffering logic and also reduce system operating current.

Features

- Compliant to USB Specification Revision 2.0 for full speed (12Mbs) and low speed (1.5Mbps) operation
- Compliant to IEC-61000-4.2 (Level 3)
- Separate I/O supply with operation down to 1.6V
- Integrated speed select termination supply
- Very-low power consumption to meet USB suspend-current requirements
- Small TSSOP and MLF® packages
- No power supply sequencing requirements
- Software controlled re-enumeration

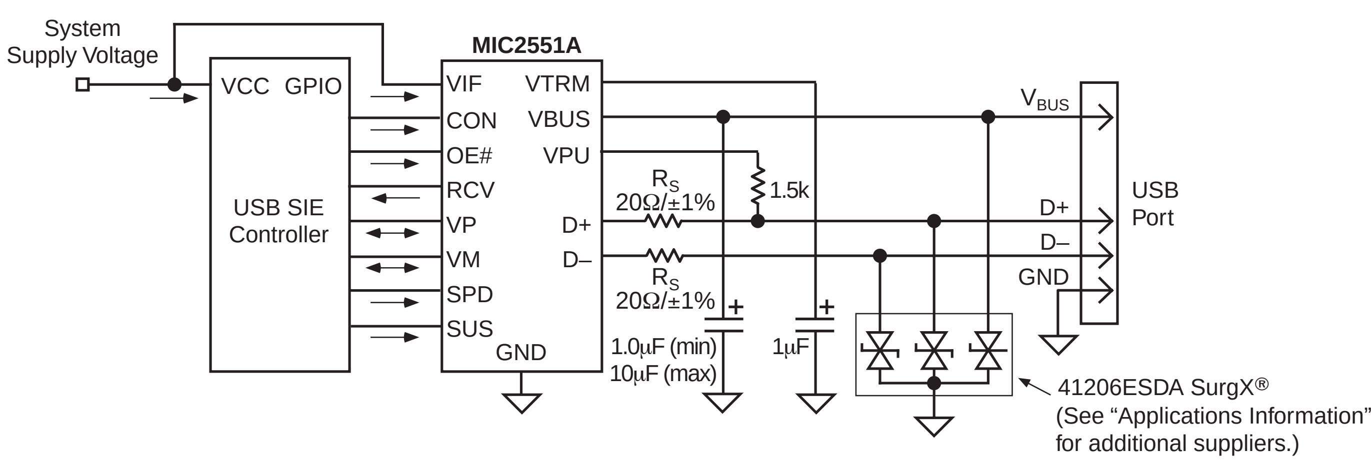
Applications

- PDAs
- Palmtops
- Cell phones

Ordering Information

Part Number		
Standard	Pb-Free	Package
MIC2551ABTS	MIC2551AYTS	14-Pin TSSOP
MIC2551ABML	MIC2551AYML	16-Pin MLF®

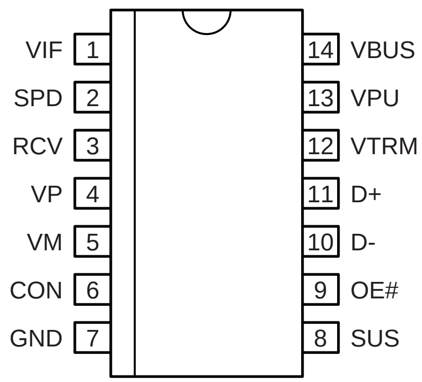
Typical Application



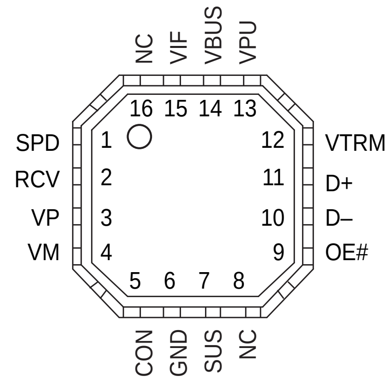
Typical Application Circuit

*Micro*LeadFrame and MLF are registered trademarks of Amkor Technology.
SurgX is a registered trademark of Cooper Electronics Technologies.

Pin Configuration



14-Pin TSSOP



16-Pin MLF® (ML)

Pin Description

Pin Number MIC2551ABTS	Pin Number MIC2551ABML	Pin Name	I/O	Pin Function
1	15	VIF	I	System Interface Supply Voltage: Used to provide reference supply voltage for system I/O interface signaling.
2	1	SPD	I	Edge Rate Control: A logic HIGH operates at edge rates for “full speed” operation. A logic LOW operates edge rates for “low speed” operation.
3	2	RCV*	O	Receive Data: Output for USB differential data.
4	3	VP*	I/O	If OE# = 1, VP = Receiver output (+) If OE# = 0, VP = Driver input (+)
5	4	VM*	I/O	If OE# = 1 VM, = Receiver output (-) If OE# = 0, VM = Driver input (-)
6	5	CON	I	CONNECT (Input): Controls state of VPU. Refer to VPU pin description for detail.
7	6	GND		Ground Reference.
8	7	SUS	I	Suspend: Active-High. Turns off internal circuits to reduce supply current.
9	9	OE#*	I	Output Enable: Active-Low. Enables the transceiver to transmit data onto the bus. When inactive, the transceiver is in the receive mode.
10/11	10/11	D–, D+*	I/O	Differential data lines conforming to the USB standard.
12	12	VTRM	O	3.3V Reference Supply Output: Requires a minimum 0.1μF decoupling capacitor for stability. A 1μF capacitor is recom-mended
13	13	VPU	O	Pull-up Supply Voltage Output: Used to connect 1.5kΩ pull-up speed detect resistor. If CON = 1, VPU is high impedance. If CON = 0, VPU = 3.3V.
14	14	VBUS	I	USB Bus Supply Voltage: Used to power USB transceiver and internal circuitry.
	8,16	NC		No connect.

* See Table 1 for description of logic states.

SUS	OE#	D+, D–	RCV	VP/VM	Function
0	0	Driving	Active	Active	Normal transmit mode.
0	1	Receiving	Active	Active	Normal receive mode.
1	0	Hi-Z	0	Not active	Low power state.
1	1	Hi-Z	0	Active	Receiving during suspend (low power state) (Note 1).

Note 1. During suspend VP and VM are active in order to detect out-of-band signaling conditions.

Table 1. Function Selection

OE# = 0:					
Input		**Output**			**Result**
VP	**VM**	**D+**	**D-**	**RCV**	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined
OE# = 1:					
Input		**Output**			**Result**
D+	**D-**	**VP**	**VM**	**RCV**	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

X - Undefined

Table 2. Truth Table During Normal Mode

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{BUS}) 6.5V
All Other Inputs .... –0.5V to 5.5V
Ambient Storage Temperature .... –65°C to +150°C
Output Current (D+, D–) .... ± 50mA
Output Current (all others) .... ±15mA
Input Current .... ±50mA
ESD, **Note 3**
V_{BUS}, D+, D– .... ±11KV
All other pins .... ±2KV

Operating Ratings (Note 2)

Supply Voltage (V_{BUS}) .... 4.0V to 5.25V
Ambient Operating Temperature .... –40°C to +85°C
Package Thermal Resistance
TSSOP (θ_{JA}) .... 100(°C/W)
MLF® (θ_{JA}) .... 59(°C/W)

DC Electrical Characteristics (System and USB Interface) (Note 7)

V_{IF} = 3.6V, V_{BUS} = 5V unless otherwise noted; T_A = 25°C. **Bold** indicates specifications over temperature, –40°C to 85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{BUS}	USB Supply Voltage		**4.0**		**5.25**	V
V_{IF}	System I/F Supply Voltage		**1.6**		**3.6**	V
V_{IL}	LOW-Level Input Voltage, **Note 4**		V_{IF}–0.3		0.15V_{IF}	V
V_{IH}	HIGH-Level Input Voltage, **Note 4**		0.85V_{IF}		V_{IF}+0.3	V
V_{OH}	HIGH-Level Output Voltage, **Note 4**	I_{OH} = 20μA	0.9V_{IF}			V
V_{OL}	LOW-Level Output Voltage, **Note 4**	I_{OL} = 20μA			0.1	V
I_{IL}	Input Leakage Current, **Note 4**		**–5**		**5**	μA

Symbol	Parameter	Conditions					Min	Typ	Max	Units
		SPD	SUS	OE#	Voltage	Load				
I_{IF}	VIF Supply Current	1	0	1	VBUS = 5.25V VIF = 3.6V			1	**5**	μA
		1	0	0				1	**5**	μA
		0	0	1				1	**5**	μA
		0	0	0				1	**5**	μA
		0	1	0				1	**5**	μA
		1	0	0		f = 6MHz CLOAD = 50 pF, **Note 7**		325	**650**	μA
		0	0	0		f = 750kHz CLOAD = 600 pF **Note 7**		40	**75**	μA
I_{VBUS}	VBUS Supply Current	1	0	1	VBUS = 5.25V VIF = 3.6V			800	1100	μA
		1	0	0				3000	**5000**	μA
		0	0	1				230	**350**	μA
		0	0	0				400	700	μA
		0	1	0				130	200	μA
		1	0	0		f = 6MHz CLOAD = 50 pF, **Note 7**		7.3	**10**	mA
		0	0	0		f = 750kHz CLOAD = 600 pF **Note 7**		3.6	**5**	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{VPULEAK}$	VPU Leakage Current	CON = 1, V_{PU} = 0V	**–5**		**5**	μA
$I_{VIFLEAK}$	VIF Leakage Current	V_{IF} = 3.6V, V_{BUS} = 0V	**–5**		**5**	μA
V_{PU}	Pull-Up Output Voltage	I_{TERM} = 200μA, V_{BUS} = 4.0 to 5.25V	**3.0**	3.3	**3.6**	V
R_{SW}	Internal Pull-Up Termination	I_{TERM} = 10mA, V_{BUS} = 4.0 to 5.25V		10		Ω
ESD Protection						
IEC-1000-4-2	Air Discharge	10 pulses		±8		kV
(D+, D–, V_{BUS} only)	Contact Discharge	10 pulses		±9		kV

DC Electrical Characteristics (Transceiver) (Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Leakage Current						
I_{LO}	Hi-Z State Data Line Leakage (Suspend Mode)	0V < V_{IN} < 3.3V, SUS = 1	**–10**		**10**	µA
Input Levels						
V_{DI}	Differential Input Sensitivity	|(D+) – (D–)|	0.2			V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-Ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
Output Levels						
V_{OL}	Static Output Low	R_L = 1.5kΩ to 3.6V			0.3	V
V_{OH}	Static Output High	R_L = 15kΩ to GND	2.8		3.6	V
Capacitance						
C_{IN}	Transceiver Capacitance	Pin to GND		10		pF
Z_{DRV}	Driver Output Resistance	Steady state drive	**8**	16	**24**	Ω

AC Electrical Characteristics (Notes 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver Characteristics (Low Speed)						
T_R	Transition Rise Time	C_L = 50pF, Figure 2 C_L = 600pF	75		 300	ns
T_F	Transition Fall Time	C_L = 50pF, Figure 2 C_L = 600pF	75		 300	ns
T_R, T_F	Rise/Fall Time Matching	(T_R, T_F)	80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Driver Characteristics (Full Speed)						
T_R	Transition Rise Time	C_L = 50pF, Figure 2	4		20	ns
T_F	Transition Fall Time	C_L = 50pF, Figure 2	4		20	ns
T_R, T_F	Rise/Fall Time Matching	(T_R, T_F)	90		111.11	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Transceiver Timing						
t_{PVZ}	OE# to RCVR Tri-State Delay	Figure 1			15	ns
t_{PZD}	Receiver Tri-State to Transmit Delay	Figure 1	15			ns
t_{PDZ}	OE# to DRVR Tri-State Delay	Figure 1			15	ns
t_{PZV}	Driver Tri-State to Receive Delay	Figure 1	15			ns
t_{PLH} t_{PHL}	VP, VM to D+, D– Propagation Delay	Figure 4			15	ns
t_{PLH} t_{PHL}	D+, D– to RCV Propagation Delay	Figure 3			15	ns
t_{PLH} t_{PHL}	D+, D– to V_P, V_M Propagation Delay	Figure 3			8	ns

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4. Specification applies to the following pins: SUS, SPD, RCV, CON, RCV, VP, VM, OE#.

Note 5. Characterized specification(s), but not production tested.

Note 6. All AC parameters guaranteed by design but not production tested.

Note 7. Specification for packaged product only.

Timing Diagrams

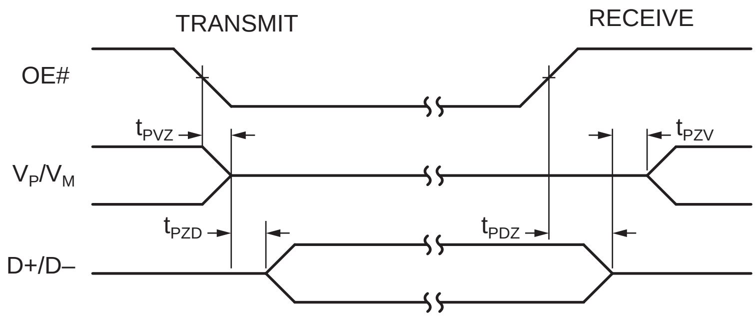


Figure 1. Enable and Disable Times

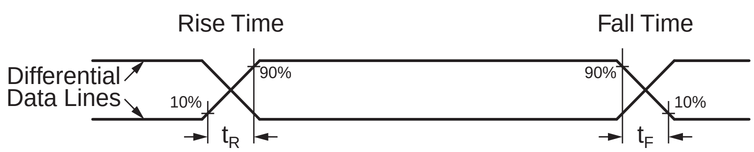


Figure 2. Rise and Fall Times

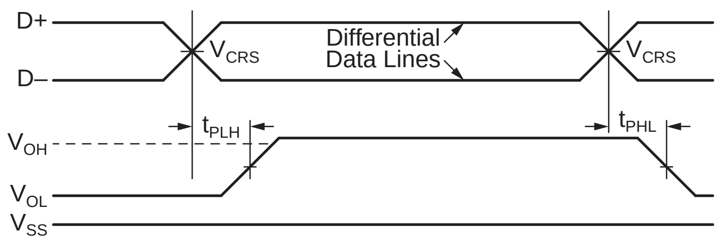


Figure 3. Receiver Propagation Delay

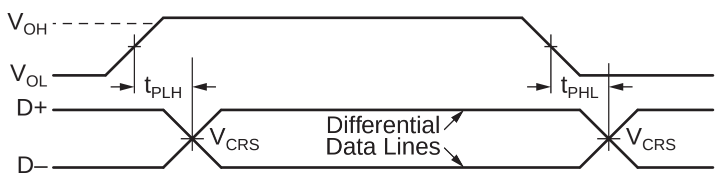


Figure 4. Driver Propagation Delay

Test Circuits

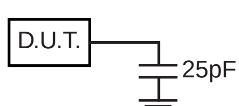


Figure 5. Load for V_P, V_M, RCV

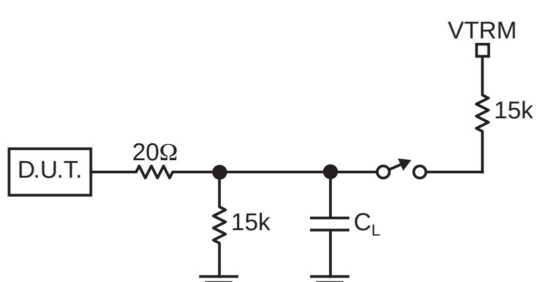
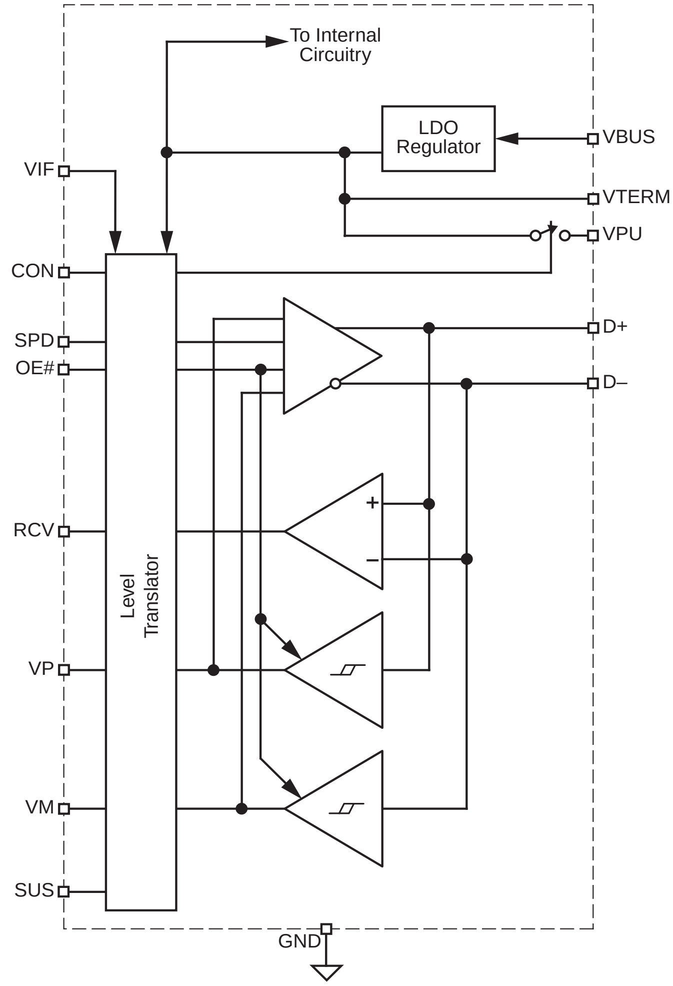


Figure 6. Load for D+, D–

Functional Diagram



MIC2551A

Applications Information

The MIC2551A is designed to provide USB connectivity in mobile systems where available system supply voltages are not able to satisfy USB requirements. The MIC2551A can operate down to supply voltages of 1.6V and still meet USB physical layer specifications. As shown in the circuit above, the MIC2551A takes advantage of the USB supply voltage, V_{BUS}, to operate the transceiver. The system voltage, V_{IF}, is used to set the reference voltage used by the digital I/O lines interfacing to the system controller. Internal circuitry provides translation between the USB and system voltage domains. V_{IF} will typically be the main supply voltage rail for the controller.

In addition, a 3.3V, 10% termination supply voltage, (V_{PU}), is provided to support speed selection. V_{PU} can be disabled or enabled under software control via the CON input. This allows for software-controlled connect or disconnect states. A 1.5k resistor is required to be connected between this pin and the D+ or D– lines to respectively specify high speed or low speed operation.

The use of ESD transient protection devices is not required for operation, but is recommended. The MIC2551A is ESD rated for 11kV at the VBUS and D+, D– pins and 2kV for all other pins.

Power Supply Configuration

The MIC2551A can be set up for different power supply configurations which modify the behavior of the device. Both V_{BUS} and V_{IF} have special thresholds that detect when they are either removed or grounded. Table 3 depicts the behavior under the different power supply configuration scenarios that are explained below.

Normal Mode

V_{BUS} is connected to the 5.0V USB bus voltage and V_{IF} is connected to a supply voltage in the range of 1.6V to 3.6V. In this case V_{TRM} supplies a 3.3V voltage for powering the speed select resistor via V_{PU} depending on the state of CON pin.

Disconnect Mode

V_{IF} is connected to a supply in a range of 1.6V to 3.6V and V_{BUS} is open or grounded. If V_{BUS} is opened while transmitting, the data lines (D+, D–) have sharing capability and may be driven with external devices up to approximately 3.6V if and only if SUSPEND is enabled (SUS = 1). With V_{BUS} ground, D+, D– sharing mode is not permitted.

Disable Mode

V_{BUS} is connected to the 5.0V USB bus voltage and V_{IF} is open. All logic controlled inputs become high impedances, thus minimal current will be supplied by V_{IF} if the input pins are pulled up to an external source.

Alternate Power Supply Configuration Options

I/O Interface Using 3.3V

In systems where the I/O interface utilizes a 3.3V USB controller, an alternate solution is shown in Figure 7. No extra components are required; however, the load on V_{TRM} must not exceed 10mA.

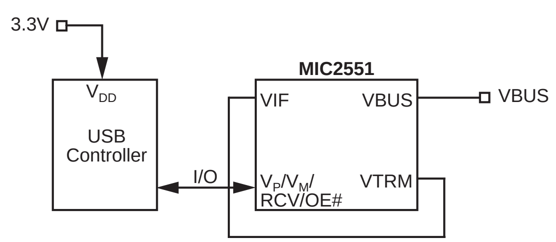


Figure 7. I/O Interface Using 3.3V

Signal Amplitude Respective to V_{IF}

When operating the MIC2551A, it is necessary to provide input signals which do not exceed V_{IF} + 0.3V.

Suspend

When the suspend pin (SUS) is high, power consumption is reduced to a minimum. V_{TRM} is not disabled. RCV, V_P and V_M are still functional to enable the device to detect USB activity. For minimal current consumption in suspend mode, it is recommended that OE# = 1, and SPD = 0.

Speed

The speed pin (SPD) sets D+/D– output edge rates by increasing or decreasing biasing current sources within the output drivers. For low speed, SPD = 0. For full speed, SPD = 1. By setting SPD = 0 during idle periods, in conjunction with suspend (SUS), the lowest quiescent current can be obtained. However, designers must provide a 300ns delay between changing SPD from 0 to 1 and transmission of data at full speed. This delay ensures the output drivers have arrived at their proper operating conditions. Failure to do so can result in leading edge distortion on the first few data bits transmitted.

External ESD Protection

The use of ESD transient protection devices is not required for operation, but is recommended. We recommend the following devices or the equivalent:

Cooper Electronic Technologies (www.cooperet.com)

41206ESDA SurgX®
0805ESDA SurgX®

Littelfuse (www.littelfuse.com)

V0402MHS05
SP0503BAHT

Non-Multiplexed Bus

In order to save pin count for the USB logic controller interface, the MIC2551A was designed with V_P and V_M as bi-directional pins. To interface the MIC2551A with a non-multiplexed data bus, resistors can be used for low cost isolation as shown in Figure 8.

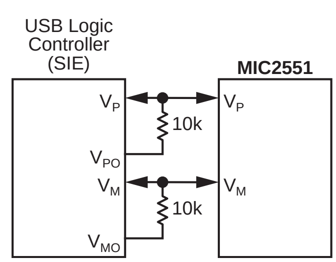


Figure 8. MIC2551A Interface to Non-Multiplexed Data Bus

Configuration Mode	VBUS/VTRM	VIF	Notes
Normal	Connected	Connected	Normal supply configuration and operation.
Disconnect (D+/D– sharing)	Open	Connected	VP/VM are HIGH outputs, RCV is LOW. With OE# = 0 and SUS = 1, data lines may be driven with external devices up to 3.6V. With D+, D– floating, I_{IF} draws less than 1µA.
Disconnect	Ground	Connected	VP/VM are HIGH outputs, RCV is LOW. With D+, D– floating, I_{IF} draws less than 1µA.
Disable Mode	Connected	Open	Logic controlled inputs pins are Hi-Z.
Prohibited	Connected	Ground	Prohibited condition.

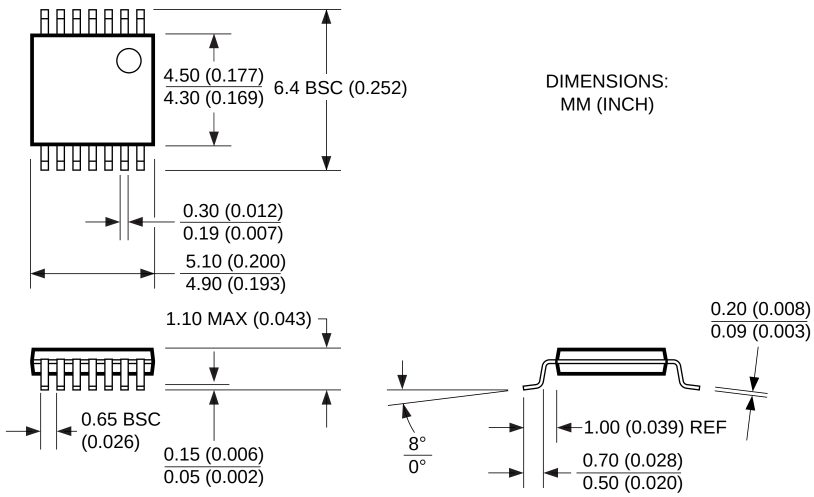
Table 3. Power Supply Configuration

PCB Layout Recommendations

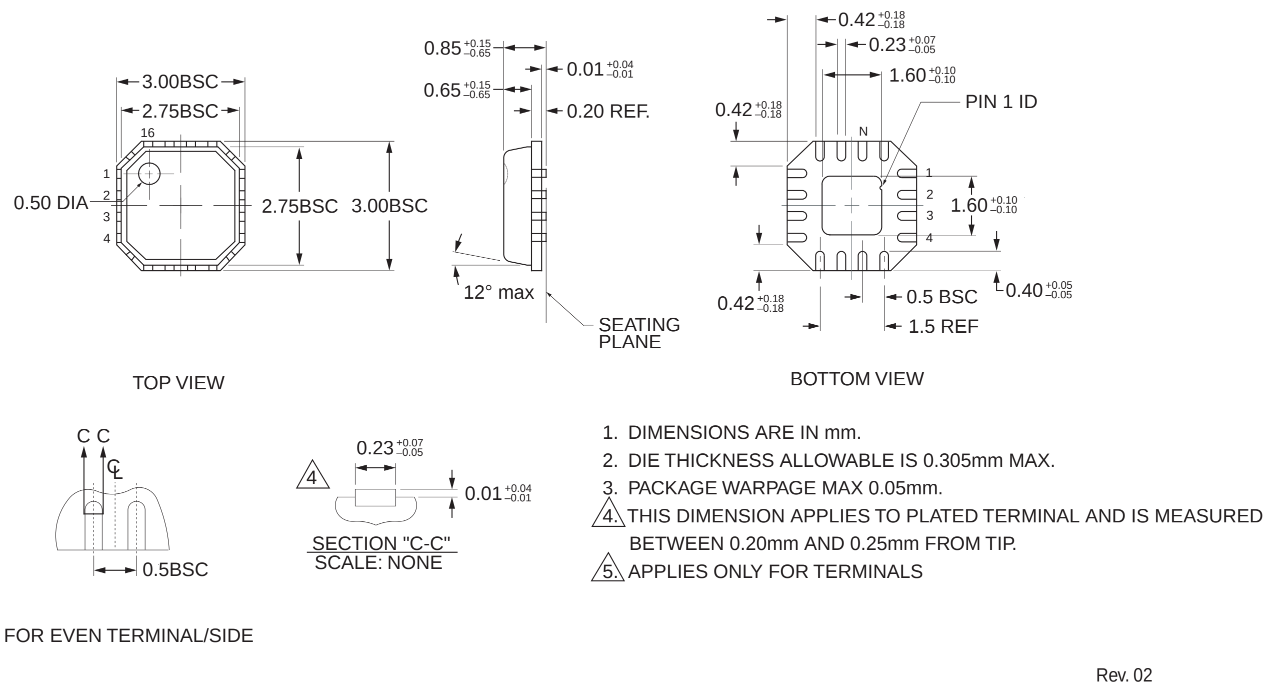
Although the USB standard and applications are not based in an impedance controlled environment, a properly designed PCB layout is recommended for optimal transceiver performance. The suggested PCB layout hints are as follows:

- Match signal line traces (VP/VM, D+, D–) to 40ps, approximately $^{1}/_{3}$ inch if possible. FR-4 PCB material propagation is about 150ps/inch, so to minimize skew try to keep VP/VM, D+/D– traces as short as possible.
- For every signal line trace width (w), separate the signal lines by 1.5 – 2 widths. Place all other traces at >2 widths from all signal line traces.
- Maintain the same number of vias on each differential trace, keeping traces approximately at same separation distance along the line.
- Control signal line impedances to ±10%.
- Keep R_S as close to the IC as possible, with equal distance between R_S and the IC for both D+ and D–.

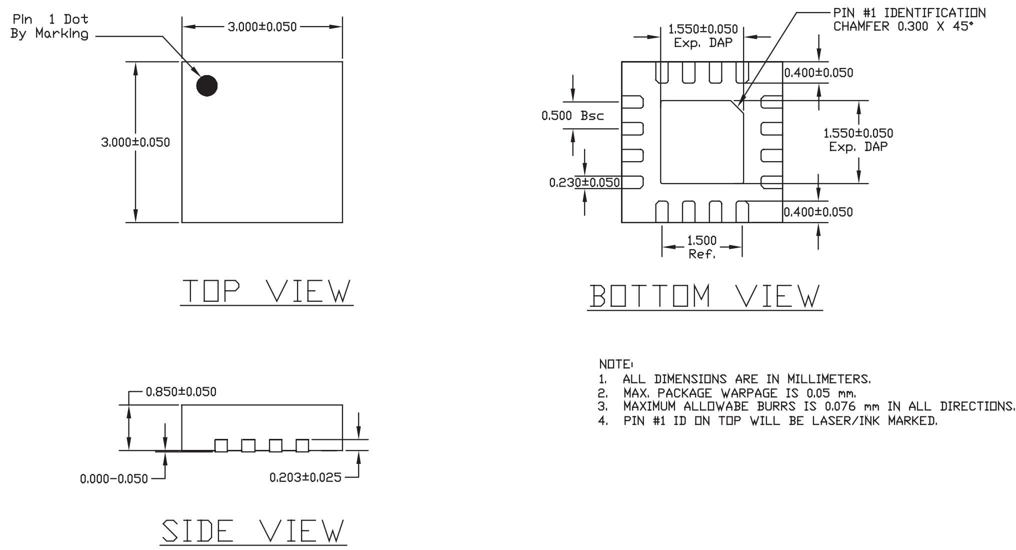
Package Information



14-lead TSSOP (TS)



16-Pin MLF® (ML)



16-Pin MLF® (ML)

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