DATASHEET

ISL97675

4-Channel LED Driver with Phase Shift Control

FN7630
Rev.2.00
Sep 13, 2017

The ISL97675 is an LED driver that drives 4 channels of low power LEDs from 4.5V to 26V input and up to 45V output.

The ISL97675 compensates for non-uniformity of the forward voltage drops in the LED strings with its 4 voltage controlled-current source channels. Its headroom control monitors the highest LED forward voltage string for output regulation, to minimize the voltage headroom and power loss in the typical multi-string operation.

The ISL97675 offers two PWM Dimming modes: The part digitizes the incoming 100Hz to 30kHz PWM signal and provides 8-bit PWM dimming with phase shift function. Another mode is direct PWM mode without phase shift, where the dimming frequency follows the input PWM signal and the minimum on time can be as short as 350ns.

The ISL97675 features channel phase shift control to minimize the input, output ripple characteristics and load transients as well as spreading the light output to help eliminate or reduce the video and audio noise interference from the backlight driver operation.

Related Literature

- For a full list of related documents, visit our website
  - ISL97675 product page

Features

- 4 x 30mA Channels
- 45V Output Max
- 4.5V to 26V Input
- Channel Phase Shift PWM Dimming with 8-bit Resolution
- 0.007% Direct PWM dimming at 200Hz
- Current Matching of ±1.5% from 1% ~ 100% Dimming
- Dynamic Headroom Control
- Protections
  - String Open/Short Circuit, V_{OUT} Short Circuit Overvoltage, and Over-temperature Protections
  - Optional Master Fault Protection
- Selectable 600kHz or 1.2MHz Switching Frequency
- 20 Ld QFN 4mmx4mm Package

Applications

- Netbook Displays LED Backlighting
- Notebook Displays LED Backlighting

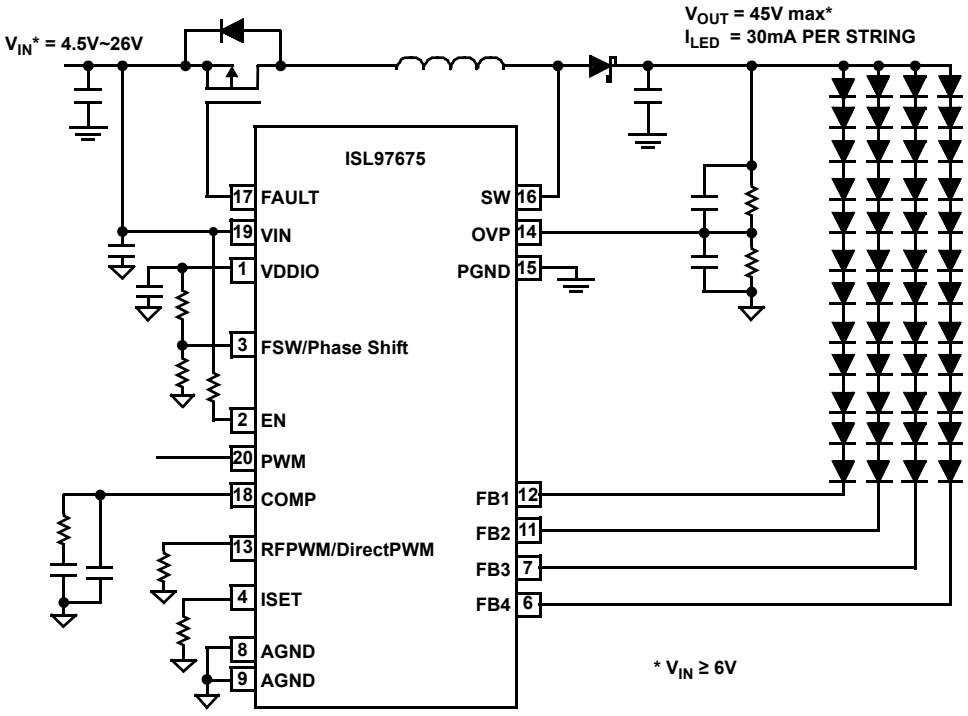
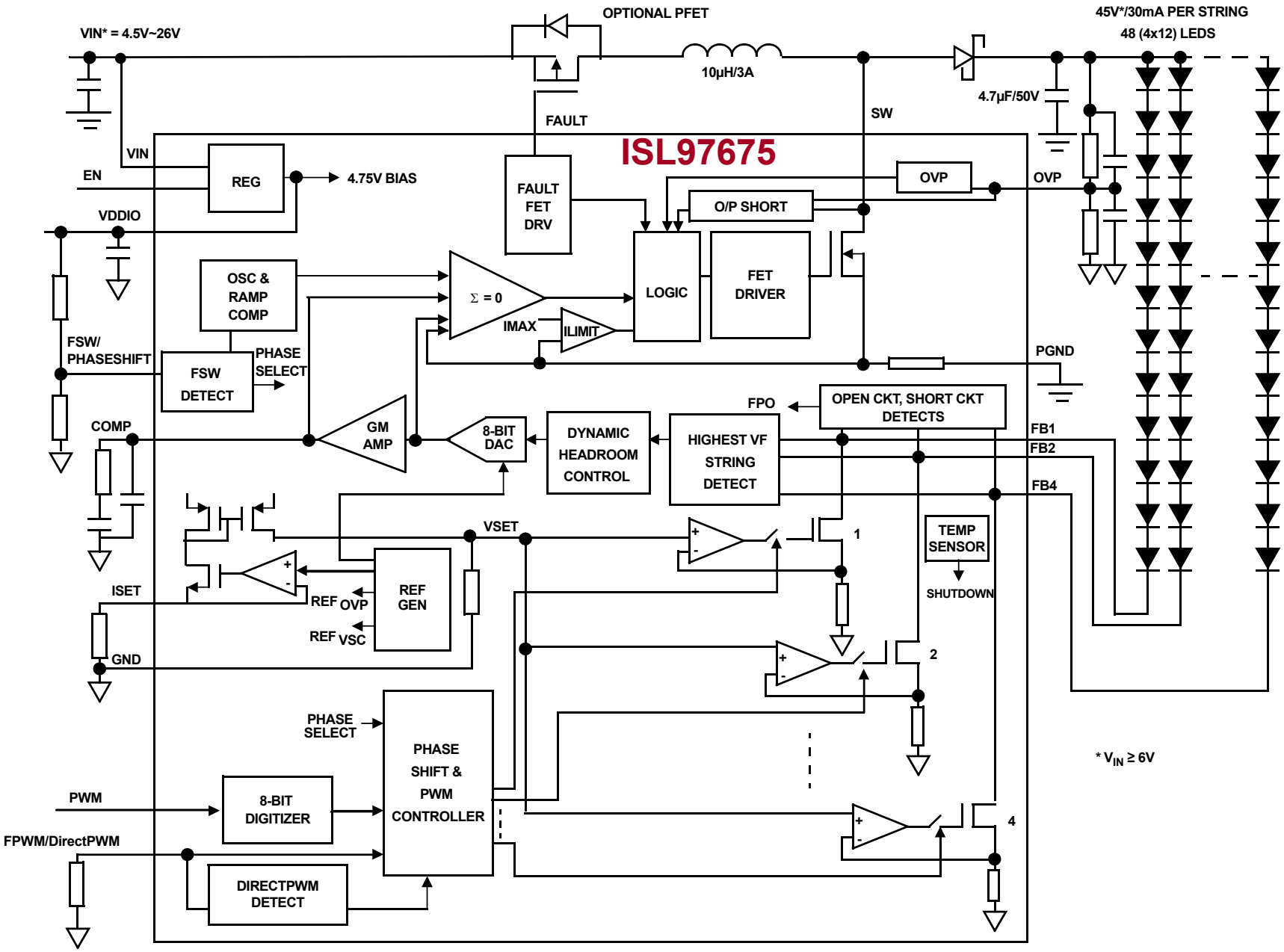


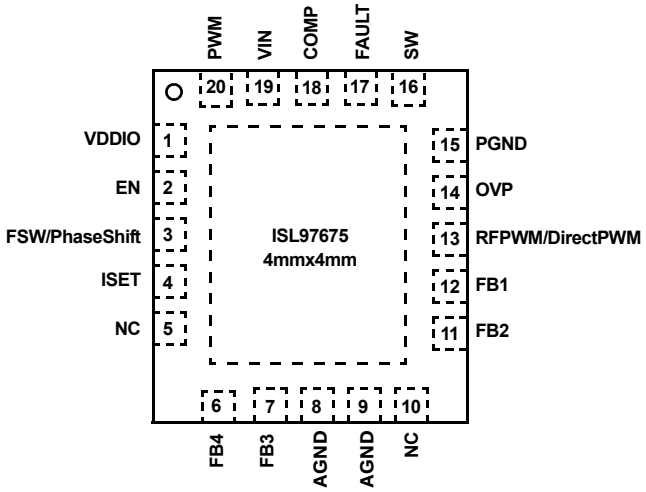
FIGURE 1. TYPICAL APPLICATION CIRCUIT

Block Diagram



Pin Configuration

ISL97675
(20 LD QFN)
TOP VIEW



Pin Descriptions (I = Input, O = Output, S = Supply)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VDDIO	1	S	Decouple with capacitor for internally generated supply rail.
EN	2	I	Enable
FSW/PhaseShift	3	I	FSW = 0 ~ 0.25 * VDDIO, Boost Switching Frequency = 1.2MHz with phase shift. FSW = 0.25 * VDDIO ~ 0.5 * VDDIO, Boost Switching Frequency = 1.2MHz without phase shift. FSW = 0.5 * VDDIO ~ 0.75 * VDDIO, Boost Switching Frequency = 600KHz without phase shift. FSW = 0.75 * VDDIO ~ VDDIO, Boost Switching Frequency = 600KHz with phase shift.
ISET	4	I	Resistor connection for setting LED current, (see Equation 3 for calculating the I_{LED}peak).
NC	5, 10	I	No Connect.
FB4	6	I	Input 4 to current source, FB, and monitoring.
FB3	7	I	Input 3 to current source, FB, and monitoring.
AGND	8, 9	S	Analog Ground for precision circuits.
FB2	11	I	Input 2 to current source, FB, and monitoring.
FB1	12	I	Input 1 to current source, FB, and monitoring.
RFPWM/DirectPWM	13	I	External PWM dimming with frequency modulation or Direct PWM dimming without frequency modulation. When this pin is not biased and a resistor is connected to ground, the dimming frequency will be set by the Setting Resistor. When this pin is floating, the part enters Direct PWM mode such that the dimming follows the input PWM signal without frequency modulation.
OVP	14	I	Overvoltage protection input.
PGND	15	S	Power ground (LX Power return).
SW	16	O	Input to boost switch.
FAULT	17	O	Gate drive signal for external fault MOSFET. This pin should be left floating when fault MOSFET is omitted in the application.
COMP	18	I	External compensation pin.

Pin Descriptions (I = Input, O = Output, S = Supply) (Continued)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VIN	19	S	LED driver supply voltage.
PWM	20	I	PWM brightness control pin.
EP	21	S	Connect Exposed Pad (EP) to junction of AGND and PGND with adequate Vias to form a star ground.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL97675IRZ	976 75IRZ	-40 to +85	20 Ld 4x4 QFN	L20.4x4C

NOTES:

1. Add “-T” suffix for 6k unit or “-TK” suffix for 1k unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see the product information page for ISL97675. For more information on MSL, see TB363.

Table of Contents

Absolute Maximum Ratings (T_A = +25°C)

VIN . . . . . -0.3V to 28V
FAULT, EN . . . . . -0.3V to min(28, VIN + 0.3)V
FSW/PhaseShift, RFPWM/DirectPWM, OVP . . . . . -0.3V to 5.5V
VDDIO, PWM, COMP . . . . . -0.3V to min(5.5, VIN + 0.3)V
ISET . . . . . -0.3V to min(VDDIO + 0.3, 5.5)V
FB1, FB2, FB3, FB4 . . . . . -0.3V to 45V
SW . . . . . -0.3V to 46V
PGND, AGND . . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to AGND pin
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A) 300V
Charged Device Model 1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5, 7)	39	2.5

Thermal Characterization (Typical)	PSI_{JT} (°C/W)
20 Ld QFN Package (Note 6)	3

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.
7. Refer to JESD51-7 high effective thermal conductivity board layout for proper via and plane designs.

Electrical Specifications

All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN = 3.3V, R_{ISET} = 19.6kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
GENERAL						
V_{IN} (Note 9)	Backlight Supply Voltage		**4.5**		**26**	V
IVIN_STBY	V_{IN} Shutdown Current	EN = 0V			**10**	µA
V_{OUT}	Output Voltage	4.5V < V_{IN} ≤ 26V, F_{SW} = 600kHz			**45**	V
		6.75V < V_{IN} ≤ 26V, F_{SW} = 1.2MHz			**45**	V
		4.5V < V_{IN} ≤ 6.75V, F_{SW} = 1.2MHz			**V_{IN}/0.15**	V
V_{UVLO}	Undervoltage Lockout Threshold		**2.6**	3.1	**3.3**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis			320		mV
REGULATOR						
V_{DDIO}	LDO Output Voltage	V_{IN} > 5.5V	**4.6**	4.8	**5**	V
I_{VDDIO_STBY}	Standby Current	EN = 0V			**10**	µA
I_{VIN}	Driver Input Current	100% Dimming		9		mA
V_{LDO}	VDDIO LDO Dropout Voltage	V_{IN} >5.5V, I_{VDDIO} = 20mA		30	**200**	mV
EN_{Low}	Guaranteed Range for EN Input Low Voltage				**0.5**	V
EN_{Hi}	Guaranteed Range for EN Input High Voltage		**1.8**			V
t_{ENLow}	EN Low Time before Shut-Down			29.5		ms

Electrical Specifications All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN = 3.3V, R_{ISET} = 19.6kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
BOOST						
SWILimit	Boost FET Current Limit		**1.5**	2.2	**2.7**	A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance	T_A = +25°C		230	300	mΩ
SS	Soft-Start	100% LED Duty Cycle		14		ms
Eff_peak	Peak Efficiency	V_{IN} = 12V, 48 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		92		%
$\Delta I_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		%
D_{MAX}	Boost Maximum Duty Cycle	FSW < 0.5 * VDDIO	**91**			%
		FSW > 0.5 * VDDIO	**82**			%
D_{MIN}	Boost Minimum Duty Cycle	FSW < 0.5 * VDDIO			**8.5**	%
		FSW > 0.5 * VDDIO			**16.5**	%
F_{SW}	Boost Switching Frequency	FSW <0.5 * VDDIO	**475**	600	**640**	kHz
		FSW >0.5 * VDDIO	**950**	1200	**1280**	kHz
ISW_leakage	SW Leakage Current	SW = 45V, EN = 0			**10**	µA
CURRENT SOURCES						
I_{MATCH}	DC Channel-to-Channel Current Matching	R_{ISET} = 19.6kΩ, (I_{OUT} = 20mA)	**-1.5**		**+1.5**	%
		R_{ISET} = 39.2kΩ, (I_{OUT} = 10mA)	**-1.5**		**+1.5**	%
I_{ACC}	Current Accuracy	R_{ISET} = 19.6kΩ, (I_{OUT} = 20mA)	**-1.5**		**+1.5**	%
$V_{HEADROOM}$	Dominant Channel Current Source Headroom at FBx Pin			500 (Note 10)		mV
$V_{HEADROOM\_RANGE}$	Dominant Channel Current Sink Headroom Range at FBx Pin	I_{LED} = 20mA, T_A = +25°C		90		mV
V_{ISET}	Voltage at I_{SET} Pin		**1.2**	1.22	**1.24**	V
I_{LEDmax}	Maximum LED Current per Channel	4-Channel, V_{IN} = 4.5V, V_{OUT} = 40V, F_{SW} = 600kHz		30		mA
PWM INTERFACE						
V_{IL}	Guaranteed Range for PWM Input Low Voltage				**0.8**	V
V_{IH}	Guaranteed Range for PWM Input High Voltage		**1.5**			V
FPWMI	PWMI Input Frequency Range		**100**		**30,000**	Hz
PWMACC	PWMI Input Accuracy			8		bits
PWMHYST	PWMI Input Allowable Jitter Hysteresis		**-0.46**		**+0.46**	LSB
PWM GENERATOR						
FPWM	PWM Dimming Frequency Range	RFPWM = 1.5MΩ	**45**	50	**55**	Hz
		RFPWM = 1.5kΩ	**33**	37	**39**	kHz
VRFPWM	Voltage at RFPWM pin		**1.19**	1.22	**1.24**	V
tDIRECTPWM	Direct PWM Minimum On Time	Direct PWM Mode	**250**		**350**	ns

Electrical Specifications All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN = 3.3V, R_{ISET} = 19.6kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
FAULT DETECTION						
V_{SC}	Channel Short Circuit Threshold		**3.15**	3.6	**4.3**	V
V_{TEMP_ACC}	Over-Temperature Threshold Accuracy			5		°C
V_{TEMP_SHDN}	Over-Temperature Shutdown			150		°C
V_{OVPlo}	Overvoltage Limit on OVP Pin		**1.2**	1.22	**1.24**	V
OVP_{FAULT}	OVP Short Detection Fault Level			350		mV
I_{FAULT}	Fault Pull-down Current	V_{IN} = 12V	**8**	15	**25**	µA
V_{FAULT}	Fault Clamp Voltage with Respect to V_{IN}	V_{IN} = 12, V_{IN} - V_{FAULT}	**6**	7	**8.3**	V
SWStart_thres	SW Start-Up Threshold		**1.2**	1.4	**1.5**	V
ISW_Startup	SW Start-Up Current		**1**	3.5	**5**	mA

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. At minimum V_{IN} of 4.5V, the maximum output is limited by the V_{OUT} specifications. Also at maximum V_{IN} of 26V, the minimum V_{OUT} is 28V but minimum V_{OUT} can be lower at lower V_{IN}. In general, the V_{IN} and V_{OUT} relationship is bounded by D_{MAX} and D_{MIN}.
10. Varies within range specified by $V_{HEADROOM\_RANGE}$.

Typical Performance Curves

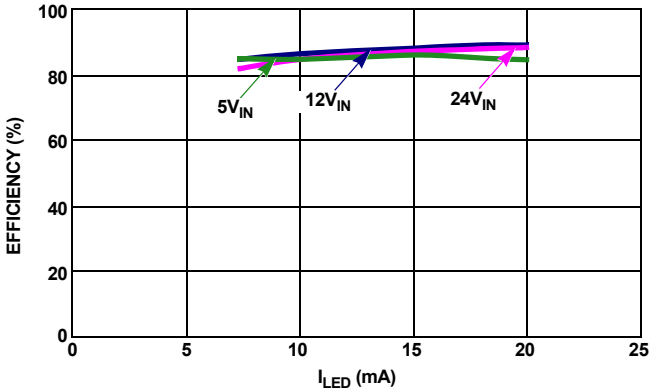


FIGURE 2. EFFICIENCY vs 20mA LED CURRENT (100% LED DUTY CYCLE) for 4P12S vs V_{IN}

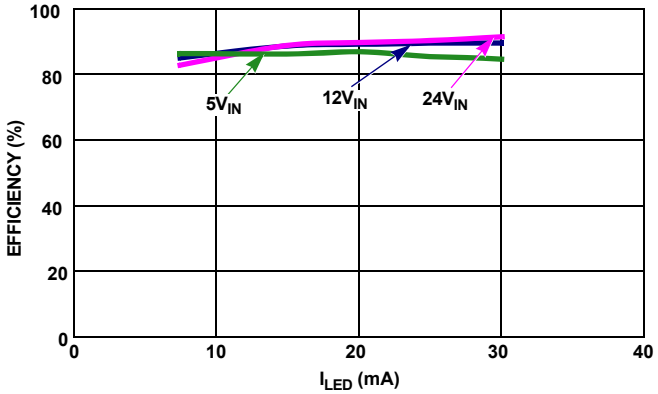


FIGURE 3. EFFICIENCY vs 30mA LED CURRENT (100% LED DUTY CYCLE) for 4P10S vs V_{IN}

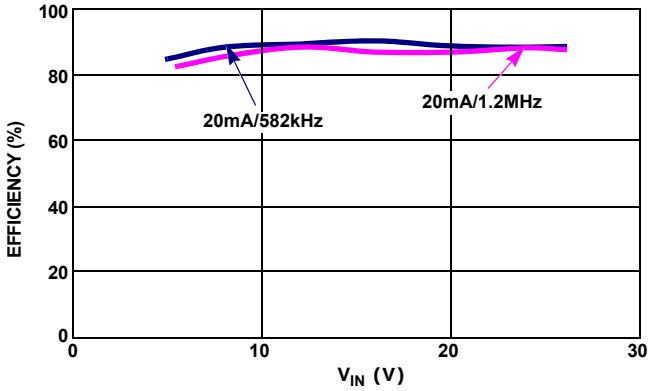


FIGURE 4. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 20mA for 4P12S (100% LED DUTY CYCLE)

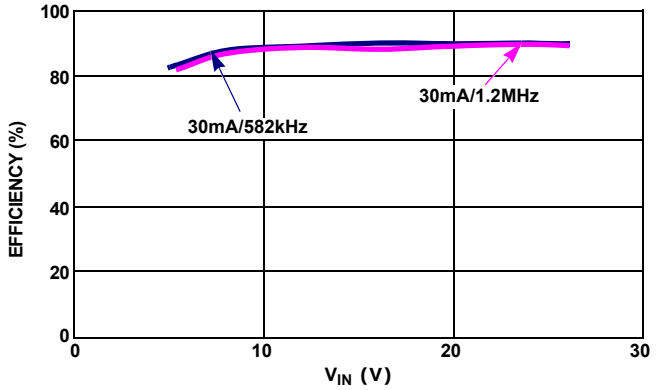


FIGURE 5. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 30mA for 4P10S (100% LED DUTY CYCLE)

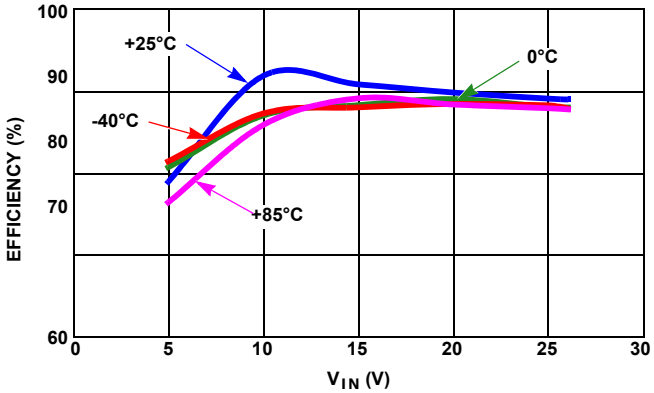


FIGURE 6. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA

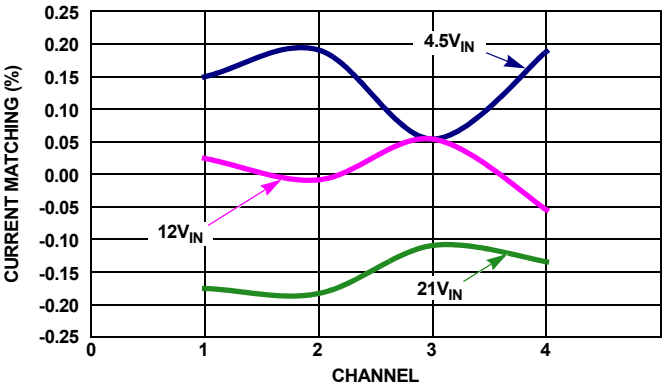


FIGURE 7. CHANNEL-TO-CHANNEL CURRENT MATCHING

Typical Performance Curves (Continued)

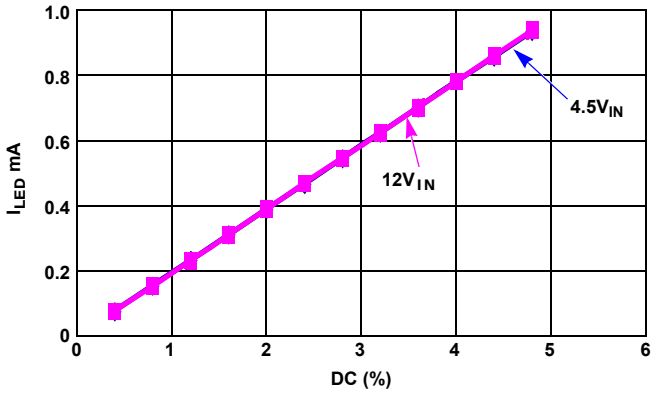


FIGURE 8. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE vs V_{IN}

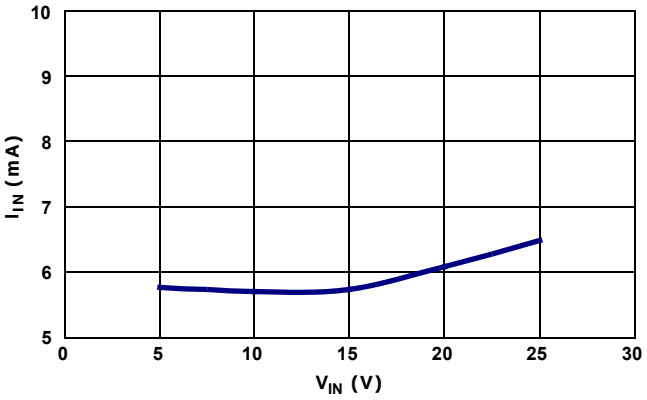


FIGURE 9. QUIESCENT CURRENT vs V_{IN} WITH PART ENABLED

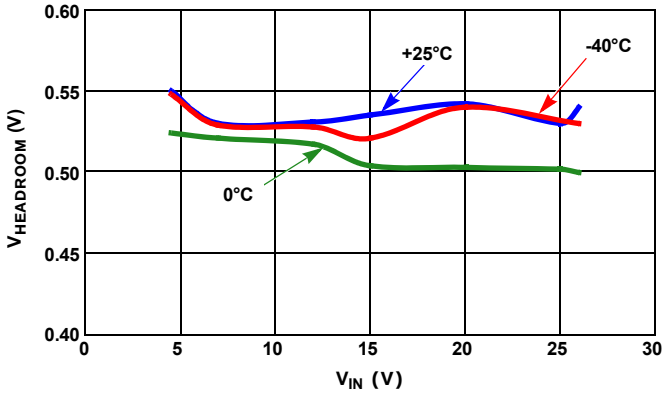


FIGURE 10. $V_{HEADROOM}$ vs V_{IN} vs TEMPERATURE AT 20mA

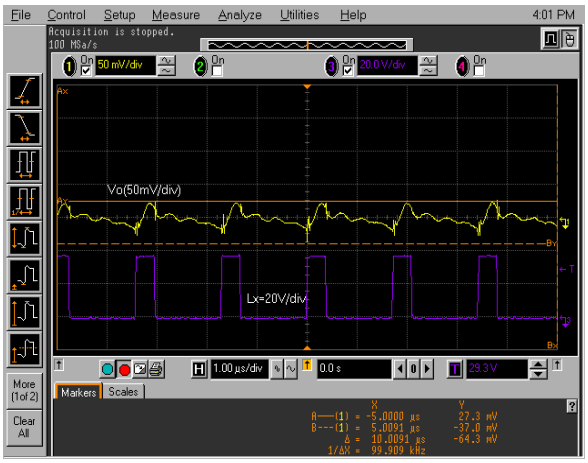


FIGURE 11. V_{OUT} RIPPLE VOLTAGE, V_{IN} = 12V, 4P12S AT 20mA/CHANNEL

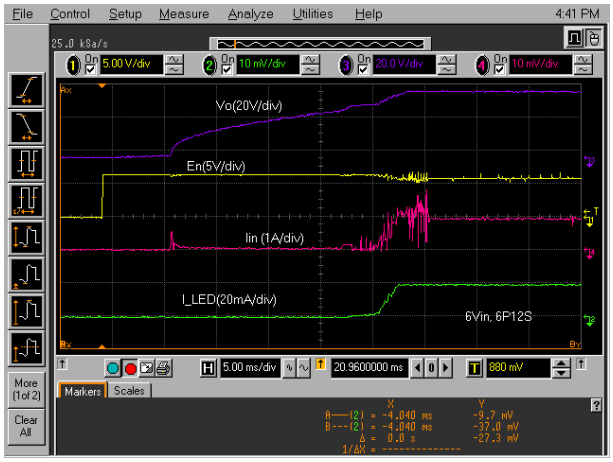


FIGURE 12. IN-RUSH AND LED CURRENT AT V_{IN} = 6V FOR 4P12S AT 20mA/CHANNEL

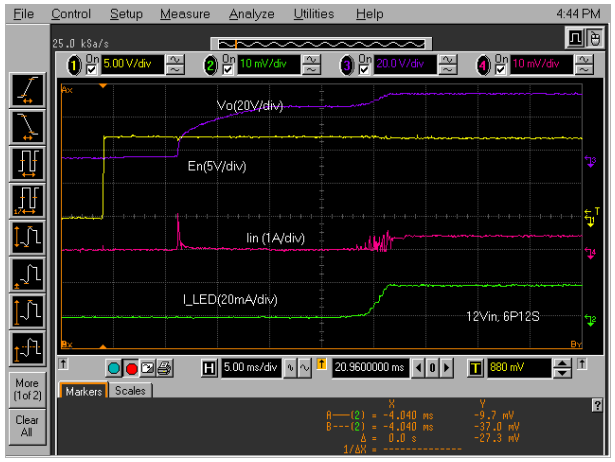


FIGURE 13. IN-RUSH AND LED CURRENT AT V_{IN} = 12V FOR 4P12S AT 20mA/CHANNEL

Typical Performance Curves (Continued)

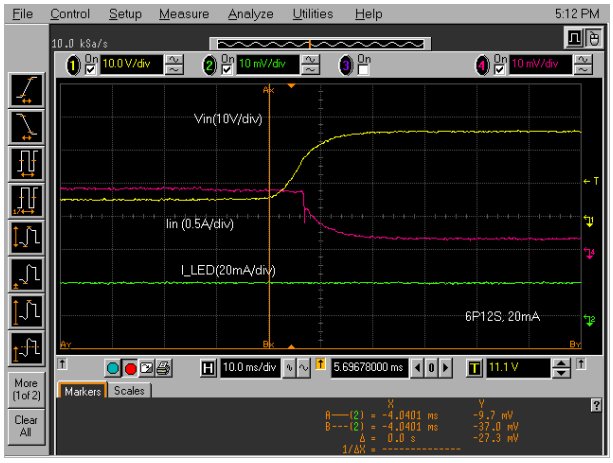


FIGURE 14. LINE REGULATION WITH V_{IN} CHANGE FROM 6V TO 26V, V_{IN} = 12V, 4P12S AT 20mA/CHANNEL

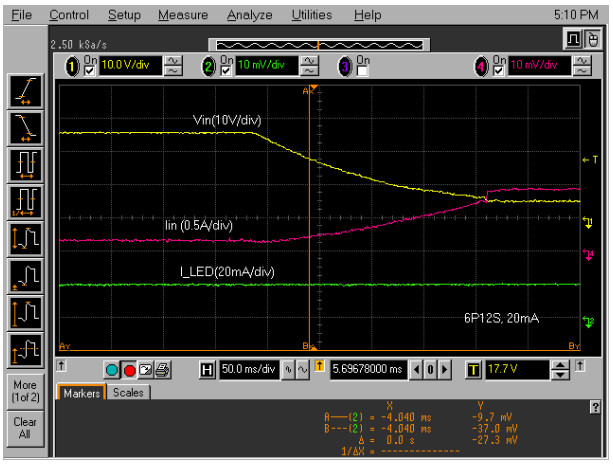


FIGURE 15. LINE REGULATION WITH V_{IN} CHANGE FROM 26V TO 6V FOR 4P12S AT 20mA/CHANNEL

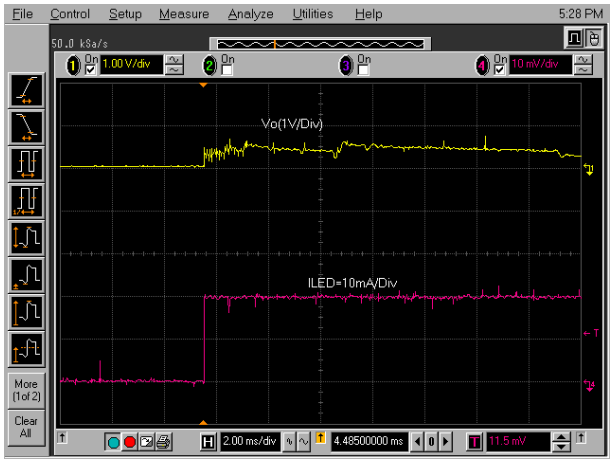


FIGURE 16. LOAD REGULATION WITH I_{LED} CHANGE FROM 0% TO 100% PWM DIMMING, V_{IN} = 12V, 4P12S AT 20mA/CHANNEL

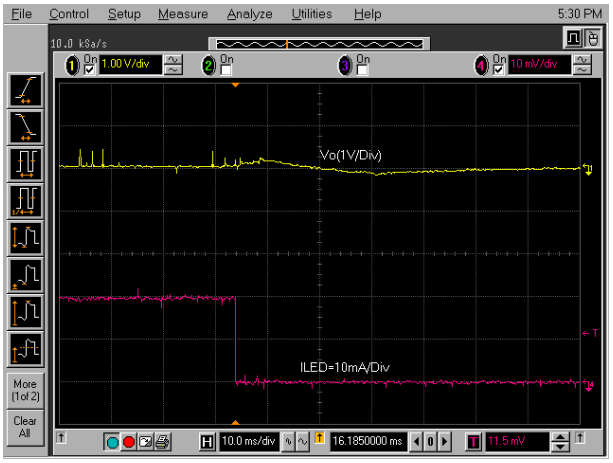


FIGURE 17. LOAD REGULATION WITH I_{LED} CHANGE FROM 100% TO 0% PWM DIMMING, V_{IN} = 12V, 4P12S AT 20mA/CHANNEL

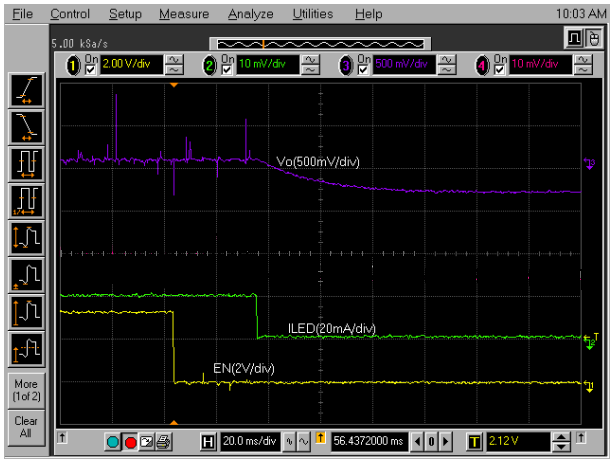


FIGURE 18. ISL97675 SHUTS DOWN AND STOPS SWITCHING ~ 30ms AFTER EN GOES LOW

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97675 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the notebook backlight application. The input power may instantly change when the user switches from a drained battery to a AC/DC adapter without causing any flicker in the display backlight. The ISL97675 is capable of boosting up to 45V and typically can drive 13 (3.2V/20mA) LEDs in series on each of the 4 channels.

OVP

The Overvoltage Protection (OVP) pin has a primary function of setting the overvoltage trip level.

The ISL97675 OVP threshold is set by R_{UPPER} and R_{LOWER} such that:

$$V_{OUT}\_OVP = 1.21V \times (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ. 1)}$$

The ISL97675 has a patent pending switching architecture that uses the OVP block for feedback monitoring, hence allowing very low PWM dimming duty cycle operation. As a result, the overvoltage trip level also limits the V_{OUT} regulation range between 64% and 100% of the V_{OUT}_OVP and the equation is:

$$\text{Allowable } V_{OUT} = 64\% \text{ to } 100\% \text{ of } V_{OUT}\_OVP \quad \text{(EQ. 2)}$$

For example, if 10 LEDs are used with the worst case V_{OUT} of 35V, and R_{UPPER} and R_{LOWER} are chosen such that the OVP level is set at 40V, then the allowed V_{OUT} range is between 25.6V and 40V. If the requirement is changed to 6 LEDs/channel for a maximum V_{OUT} of 21V, then the OVP level must be reduced according to Equation 2 to accommodate the new reduced output voltage. Otherwise, the headroom control will be disturbed and the channel voltage may be higher and prevent the driver from operating properly.

The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if R_{UPPER}/R_{LOWER} = 33/1, then C_{UPPER}/C_{LOWER} = 1/33. For example, if C_{UPPER} = 100pF then C_{LOWER} = 3.3nF.

Enable

An EN signal is required to enable the internal regulator for normal operation. If there is no signal longer than 28ms, the device will enter shutdown.

Power Sequence

There is no specific power sequence requirement for the ISL97675. The EN signal can be tied to V_{IN} but not the VDDIO as it will prevent the device from powering up.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 19.

The LED peak current is set by translating the R_{ISET} current to the output with a scaling factor of $392/R_{ISET}$. The drain terminals of the current source MOSFETs are designed to operate within a range at about ~ 500mV to minimize power loss. The sources of errors for the channel-to-channel current matching are due to internal mismatches, offsets and the external R_{ISET} resistor. To minimize this external offset, a 1% tolerance resistor is recommended.

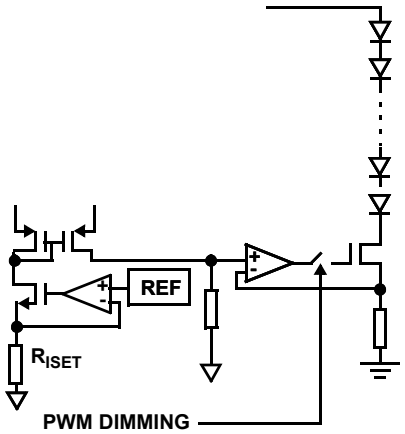


FIGURE 19. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97675 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the FB1-4 pins digitally. This lowest FB voltage is used as the feedback signal for the boost regulator. Since all LED stacks are connected in parallel to the same output voltage, the other FB pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same current. The output voltage will regulate cycle by cycle and it is always referenced to the highest forward voltage string in the architecture.

Dimming Controls

The ISL97675 allows two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment.
2. PWM chopping of the LED current defined in step 1.

Maximum DC Current Setting

The initial brightness should be set by choosing an appropriate value for R_{ISET}. This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{(392)}{R_{ISET}} \quad \text{(EQ. 3)}$$

For example, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 3 yields Equation 4:

$$R_{ISET} = (392)/0.02 = 19.6k\Omega \quad \text{(EQ. 4)}$$

PWM Control

The ISL97675 has a high speed 8-bit digitizer that decodes an incoming PWM signal and converts it into four channels of 8-bit PWM current with a phase shift function that will be described later. During the PWM On period, the LED peak current is defined by the value of R_{ISET} resistor, the average LED current of each channel is controlled by I_{LEDmax} and the PWM duty cycle in percent as:

$$I_{LED(ave)} = I_{LEDmax} \times PWM \quad \text{(EQ. 5)}$$

When the PWM input = 0, all channels are disconnected and the I_{LED} is guaranteed to be <10µA in this state.

The PWM dimming frequency is adjusted by a resistor at the RFPWM pin, which will be described in "PWM Dimming Frequency Adjustment" on page 14.

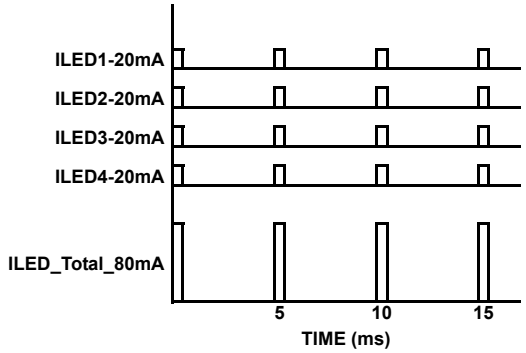


FIGURE 20. CONVENTIONAL 4-Ch LED DRIVER WITH 10% PWM DIMMING CHANNEL CURRENT (UPPER) AND TOTAL CURRENT (LOWER)

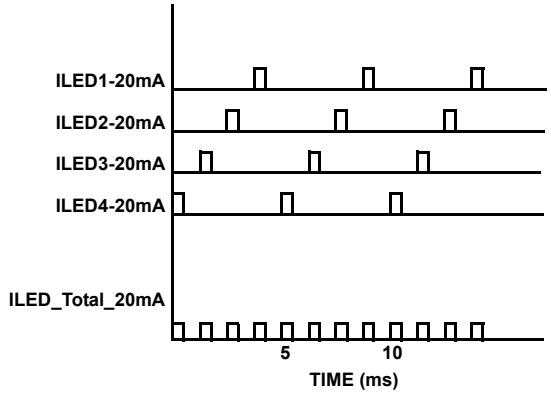


FIGURE 21. PHASE SHIFT 4-Ch LED DRIVER WITH 10% PWM DIMMING CHANNEL CURRENT (UPPER) AND TOTAL CURRENT (LOWER)

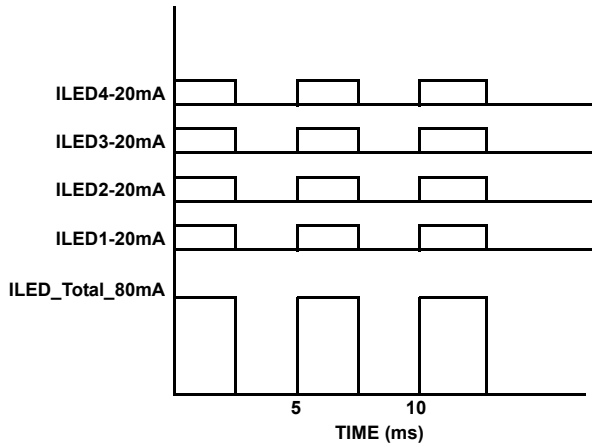


FIGURE 22. CONVENTIONAL LED DRIVER PWM DIMMING CHANNEL AND TOTAL CURRENT AT 50% DUTY CYCLE

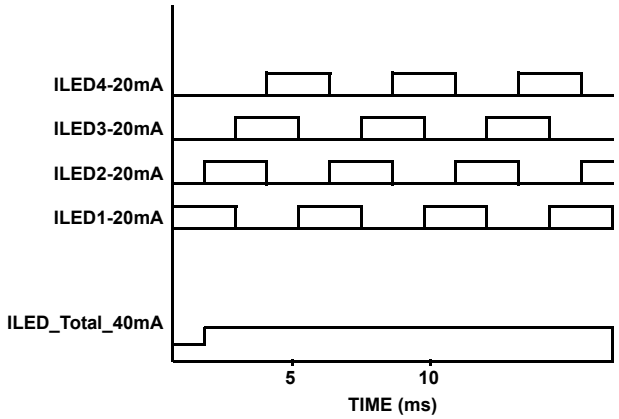


FIGURE 23. EQUAL PHASE SHIFT LED DRIVERpwm DIMMING CHANNEL AT 50% DUTY CYCLE

Phase Shift Control

The ISL97675 is capable of delaying the phase of each current source. Conventional LED drivers pose the worst load transients to the boost circuit by turning on all channels simultaneously as shown in Figure 20. In contrast, the ISL97675 phase shifts each channel by turning them on once during each PWM dimming period as shown in Figure 21. At each dimming duty cycle except at 100%, the sum of the phase shifted channel currents will be less than a conventional LED driver as shown in Figure 21 and 23. Equal phase means there is fixed delay between channels and such delay can be calculated as:

$$t_{D1} = \frac{t_{FPWM}}{(255)} x \left(\frac{255}{N}\right) \quad \text{(EQ. 6)}$$

$$t_{D2} = \frac{t_{FPWM}}{255} x \left((255) - (N-1)\left(\frac{255}{N}\right)\right) \quad \text{(EQ. 7)}$$

where (*255/N*) in Equation 6 and Equation 7 can only be integer because the PWM dimming is controlled by an internal 8-bit

digital counter. As a result, any decimal value of (255/N) will be discarded. For example for N = 4, (*255/N*) = 63, thus:

$$t_{D1} = t_{FPWM} \times \frac{63}{255}$$
$$t_{D2} = t_{FPWM} \times \frac{66}{255} \quad \text{(EQ. 8)}$$

where t_{FPWM} is the sum of t_{ON} and t_{OFF}. N is the number of active channels. The ISL97675 will detect the numbers of active channels automatically and is illustrated in Figure 24 for 4-channel.

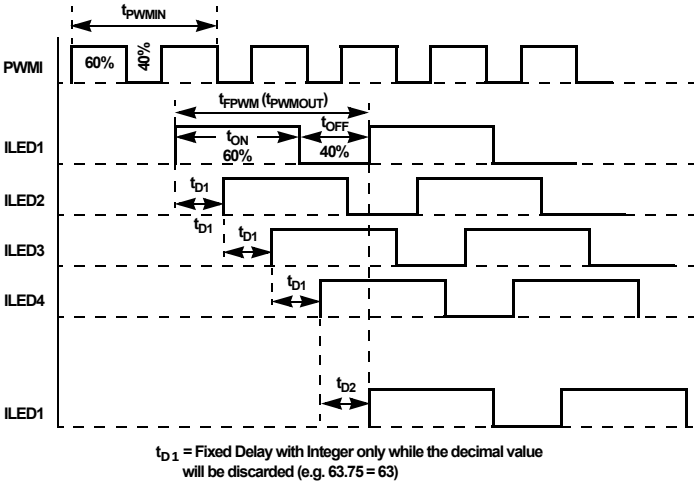


FIGURE 24. 4 EQUAL PHASE CHANNELS PHASE SHIFT ILLUSTRATION

PWM Dimming Frequency Adjustment

The dimming frequency is set by an external resistor at the RFPWM/DirectPWM pin to GND:

$$F_{PWM} = \frac{6.66 \times 10^7}{RFPWM} \quad \text{(EQ. 9)}$$

where FPWM is the desirable PWM dimming frequency and R_{FPWM} is the setting resistor. Do not bias RFPWM/DirectPWM if direct PWM dimming is used, see Table 1 for clarification.

The PWM dimming frequency can be set or applied up to 30kHz with duty cycle from 0.4% to 100%. The lower limit of 0.4% is the result of 8-bit digitizer resolution.

Direct PWM Dimming

The ISL97675 can also operate in direct PWM dimming mode such that the output follows the input PWM signal without phase shifting. To use Direct PWM mode, users should float RFPWM/DirectPWM pin. The input PWM frequency should be limited to 30kHz and the minimum duty cycle be calculated by the following Equation 10:

$$\text{Min Duty Cycle} = 350\text{ns} \times \text{Input PWM Frequency} \quad \text{(EQ. 10)}$$

For example, for a 200 Hz input PWM frequency, the minimum duty cycle is:

$$\text{Min DC} = 350\text{ns} \times 200\text{Hz} = 0.007\% \quad \text{(EQ. 11)}$$

Table 1 shows the PWM Dimming with Phase Shift and Direct PWM Dimming configurations.

TABLE 1.

RFWM/ DIRECTPWM	FUNCTION	PHASE SHIFT	Dimming Resolution
Connects with Resistor	PWM Dimming with frequency adjust	Yes	8-bit
Floating	DirectPWM without frequency adjust	No	N/A

Switching Frequency

When the FSW/PhaseShift pin is biased from VDDIO with a resistor divider R_{UPPER} and R_{LOWER}, the switching frequency and phase shift function will change according to the following FSW/PhaseShift levels shown in Table 2 with the recommended R_{UPPER} and R_{LOWER} values.

TABLE 2.

FSW/PHASE SHIFT LEVEL	SWITCHING FREQUENCY	PHASE SHIFT	R_{UPPER} (kΩ)	R_{LOWER} (kΩ)
0 ~ 0.25 * VDDIO	1.2MHz	Yes	Open	0
0.25 * VDDIO ~ 0.5 * VDDIO	1.2MHz	No	150	100
0.5 * VDDIO ~ 0.75 * VDDIO	600kHz	No	100	150
0.75 * VDDIO ~ VDDIO	600kHz	Yes	0	Open

Inrush Control and Soft-Start

The ISL97675 has separate built-in independent inrush control and soft-start functions. The inrush control function is built around the short circuit protection FET, and is only available in applications which include this device.

After an initial delay from the point where the master Fault Protection FET is turned on, it is assumed that inrush has completed. At this point, the boost regulator will begin to switch and the current in the inductor will ramp-up. The current in the boost power switch is monitored and the switching is terminated in any cycle where the current exceeds the current limit. The ISL97675 includes a soft-start feature where this current limit starts at a low value (275mA). This is stepped up to the final 2.2A current limit in 7 further steps of 275mA. These steps will happen over at least 8ms, and will be extended at low LED PWM frequencies if the LED duty cycle is low. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

For systems with no master fault protection FET, the inrush current will flow towards C_{OUT} when V_{IN} is applied and it is determined by the ramp rate of V_{IN} and the values of C_{OUT} and boost inductor, L.

Fault Protection and Monitoring

The ISL97675 features extensive protection functions to cover all the perceivable failure conditions. The failure mode of an LED can be either open circuit or as a short. The behavior of an open circuited LED can additionally take the form of either infinite

resistance or, for some LEDs, a zener diode, which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel of LEDs without affecting other channels. Similarly, a LED short circuit condition which causes the FB voltage to rise to ~4V, will result in that channel turning off. This does not affect any other channels.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97675 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 3 for more details.

A fault condition that results in high input current due to a short on V_{OUT} with master fault protection switch will result in a shutdown of all output channels. The control device logic will remain functional.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected above the programmed short circuit threshold. When an LED becomes shorted, the action taken is described in Table 3. The short circuit threshold is 4V.

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97675 monitors the current in each channel such that any string which reaches the intended output current is considered “good”. Should the current subsequently fall below the target, the channel will be considered an “open circuit”. Furthermore, should the boost output of the ISL97675 reach the OVP limit or should the lower over-temperature threshold be reached, all channels which are not “good” will immediately be considered as “open circuit”. Detection of an “open circuit” channel will result in a time-out before disabling of the affected channel. This time-out is run when the device is above the lower over-temperature threshold in an attempt to prevent the upper over-temperature trip point from being reached.

Some users employ special types of LEDs that have zener diode structure in parallel with the LED for ESD enhancement, thus enabling open circuit operation. When this type of LED goes open circuit, the effect is as if the LED forward voltage has increased, but no light is emitted. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, to make sure that multiple failures on one string do not cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channels look as if they have LED shorts. See Table 3 for details for responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as:

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad \text{(EQ. 12)}$$

These resistors should be large to minimize the power loss. For example, a 1MΩ R_{UPPER} and 30kΩ R_{LOWER} sets OVP to 41.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the PWM Off time. Parallel capacitors should also be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 3.1V, the device will stop switching and be reset. Operation will restart once the input voltage is back in the normal operating range.

Master Fault Protection

During normal switching operation, the current through the internal boost power FET is monitored. If the input current exceeds the current limit due to output shorted to ground or excessive loading, the internal switch will be turned off. This monitoring happens on a cycle by cycle basis in a self protecting way.

Additionally, the ISL97675 monitors the voltage at the LX and OVP pins. At start-up, a fixed current is injected out of the LX pins and into the output capacitor. The device will not start up unless the voltage at LX exceeds 1.2V. The OVP pin is also monitored such that if it rises above and subsequently falls below 20% of the target OVP level, the input protection FET will be switched off.

Over-Temperature Protection (OTP)

The ISL97675 includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel which is outputting current at a level below the regulation target will be treated as “open circuit” and disabled after a time-out period. The intention of the lower threshold is to allow bad channels to be isolated and disabled before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off.

For the extensive fault protection conditions, please refer to Figure 25 and Table 3 for details.

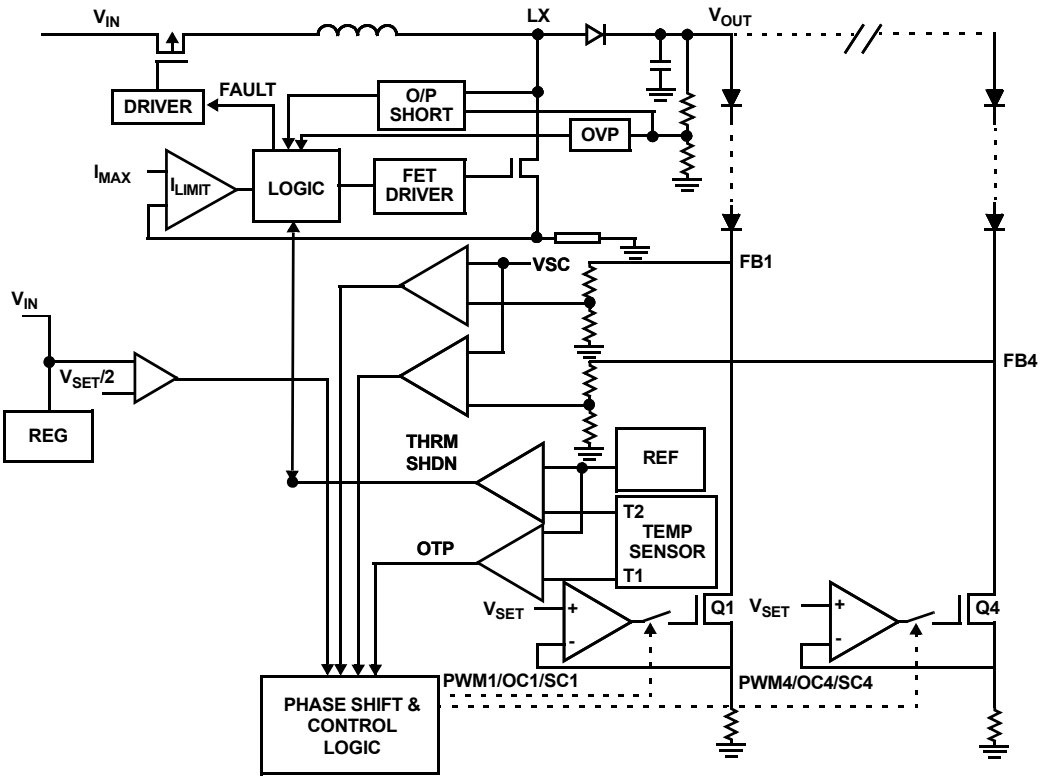


FIGURE 25. SIMPLIFIED FAULT PROTECTIONS

TABLE 3. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	FB1 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and FB1 < 4V	FB1 ON and burns power.	FB2 through FB4 Normal	Highest VF of FB2 through FB4
2	FB1 Short Circuit	Upper OTP triggered but VFB1 < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further.	Same as FB1	Highest VF of FB2 through FB4
3	FB1 Short Circuit	Upper OTP not triggered but FB1 > 4V	FB1 disabled after 6 PWM cycle timeout.	FB2 through FB4 Normal	Highest VF of FB2 through FB4
4	FB1 Open Circuit with infinite resistance	Upper OTP not triggered and FB1 < 4V	V_{OUT} will ramp to OVP. FB1 will time-out after 6 PWM cycles and switch off. V_{OUT} will drop to normal level.	FB2 through FB4 Normal	Highest VF of FB2 through FB4
5	FB1 LED Open Circuit but has paralleled Zener	Upper OTP not triggered and FB1 < 4V	FB1 remains ON and has highest VF, thus V_{OUT} increases.	FB2 through FB4 ON, Q2 through Q4 burn power	VF of FB1
6	FB1 LED Open Circuit but has paralleled Zener	Upper OTP triggered but FB1 < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further	Same as FB1	VF of FB1

TABLE 3. PROTECTIONS TABLE (Continued)

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
7	FB1 LED Open Circuit but has paralleled Zener	Upper OTP not triggered but FBx > 4V	FB1 remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases, then FB-X switches OFF after 6 PWM cycles. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of FB1
8	Channel-to-Channel ΔVF too high	Lower OTP triggered but FBx < 4V	Any channel at below the target current will fault out after 6 PWM cycles. Remaining channels driven with normal current.		Highest VF of FB1 through FB4
9	Channel-to-Channel ΔVF too high	Upper OTP triggered but FBx < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further		Highest VF of FB1 through FB4
10	Output LED stack voltage too high	V_{OUT} > VOVP	Any channel that is below the target current will time-out after 6 PWM cycles, and V_{OUT} will return to the normal regulation voltage required for other channels.		Highest VF of FB1 through FB4
11	V_{OUT}/LX shorted to GND at start-up or V_{OUT} shorted in operation	LX current and timing are monitored. OVP pins monitored for excursions below 20% of OVP threshold.	The chip is permanently shutdown 31ms after power-up if V_{OUT}/Lx is shorted to GND.		

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On-time is equal to the change of inductor current during the switching regulator Off-time. Since the voltage across an inductor is:

$$V_L = L \times \Delta I_L / \Delta t \quad \text{(EQ. 13)}$$

and $\Delta I_L @ T_{ON} = \Delta I_L @ T_{OFF}$, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \quad \text{(EQ. 14)}$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is Schottky diode forward voltage which can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as:

$$V_O/V_I = 1/(1 - D) \quad \text{(EQ. 15)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 16)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

In boost mode, input current flows continuously into the inductor; AC ripple component is only proportional to the rate of the inductor charging, thus, smaller value input capacitors may be used. It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability.

The inductor's maximum current capability must be large enough to handle the peak current at the worst case condition. If an inductor core is chosen with a lower current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the off period, as expressed in Equation 17:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_{SW})] \quad \text{(EQ. 17)}$$

The choice of 85% is just an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and f_{SW}. As a result, for a given switching frequency, minimum input voltage must be used to calculate the input/inductor current as shown in Equation 17. Fora given inductor size, the larger the inductance value, the higher the series resistance because of the extra number of turns required, thus, higher conductive losses. The ISL97675 current limit should be less than the inductor saturation current.

Output Capacitors

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor during the FET ton period and the voltage drop due to load current flowing through the ESR of the output capacitor. The ripple voltage is shown in Equation 18:

$$\Delta V_{CO} = (I_O / C_O \times D / f_S) + ((I_O \times ESR)) \quad \text{(EQ. 18)}$$

Equation 18 shows the importance of using a low ESR output capacitor for minimizing output ripple.

The choice of X7R over Y5V ceramic capacitors is highly recommended because the former capacitor is less sensitive to capacitance change over voltage as shown in Figure 26. Y5V's absolute capacitance can be reduced to 10%~20% of its rated capacitance at the maximum voltage. In any case, Y5V type of ceramic capacitor should be avoided.

Here are some recommendations for various applications:

For 20mA applications with V_{IN} > 7V, 1 x 4.7µF (X7R type) is sufficient.

For 20mA applications with V_{IN} < 7V, 2 x 4.7µF (X7R type) is required in some configurations.

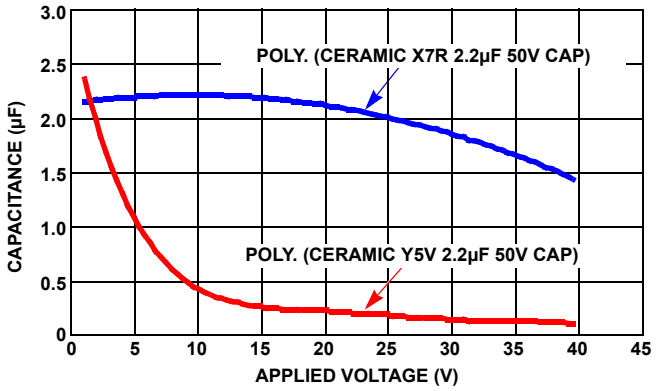


FIGURE 26. X7R AND V5Y TYPES CERAMIC CAPACITORS

Channel Capacitor

It is recommended to use at least 1.5nF capacitors from CH pins to V_{OUT}. Larger capacitors will reduce LED current ripple at boost frequency, but will degrade transient performance at high PWM frequencies. The best value is dependant on PCB layout. Up to 4.7nF is sufficient for most configurations.

Output Ripple

ΔV_{Co}, can be reduced by increasing Co or f_{SW}, or using small ESR capacitors as shown in Equation 18. In general, Ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

A larger output capacitor will also ease the driver response during PWM dimming off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost as much on the next on period which minimizes transient current. The output capacitor is also needed for compensation, and, in general one to two 4.7µF/50V ceramic capacitors are needed for netbook or notebook display backlight applications.

Schottky Diode

A high speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current will minimize losses, making Schottky diodes the preferred choice. Although the Schottky diode turns on only during the boost switch off period, it carries the same peak current as the inductor, therefore, a suitable current rated Schottky diode must be used.

Applications

High Current Applications

Each channel of the ISL97675 can support up to 40mA. For applications that need higher current, multiple channels can be grouped to achieve the desirable current. For example, the cathode of the last LED can be connected to FB1 to FB2, this configuration can be treated as a single string with 80mA current driving capability.

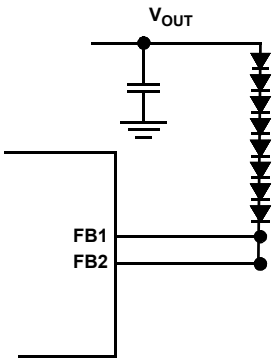


FIGURE 27. GROUPING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
9/13/17	FN7630.2	Applied new header/footer. Added Related Literature. Updated Note 1. Added VHEADROOM_RANGE spec to EC table. Added Note 10. In “Current Matching and Current Accuracy” on page 12 updated 2nd sentence in paragraph 2 for clarification. Replaced Products section with About Intersil.
9/14/11	FN7630.1	On page 3 in “Pin Descriptions”: Changed pin 3 description from: “FSW = 0 ~ 0.25 * VDDIO, Boost Switching Frequency = 600kHz with phase shift. FSW = 0.25 * VDDIO ~ 0.5 * VDDIO, Boost Switching Frequency = 600kHz without phase shift. FSW = 0.5 * VDDIO ~ 0.75 * VDDIO, Boost Switching Frequency = 1.2MHz without phase shift. FSW = 0.75 * VDDIO ~ VDDIO, Boost Switching Frequency = 1.2MHz with phase shift.” to “FSW = 0 ~ 0.25 * VDDIO, Boost Switching Frequency = 1.2MHz with phase shift. FSW = 0.25 * VDDIO ~ 0.5 * VDDIO, Boost Switching Frequency = 1.2MHz without phase shift. FSW = 0.5 * VDDIO ~ 0.75 * VDDIO, Boost Switching Frequency = 600KHz without phase shift. FSW = 0.75 * VDDIO ~ VDDIO, Boost Switching Frequency = 600KHz with phase shift.” On page 14 in Table 2: Changed “Switching Frequency” in first 2 rows from 600khz to 1.2Mhz Changed “Switching Frequency” in last 2 rows from 1.2MHz to 600kHz Updated Tape & Reel note in Ordering Information to add "Add “-T*” suffix for tape and reel." The "*" covers all possible tape and reel options
5/19/10	FN7630.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

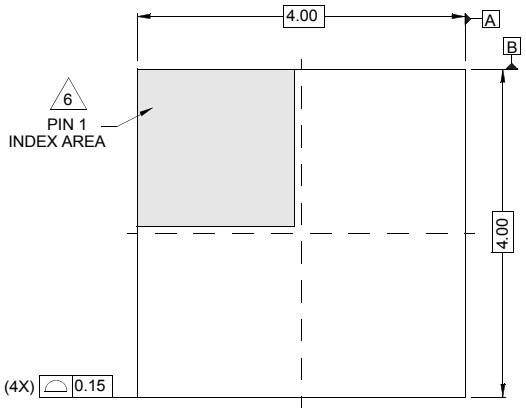
For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

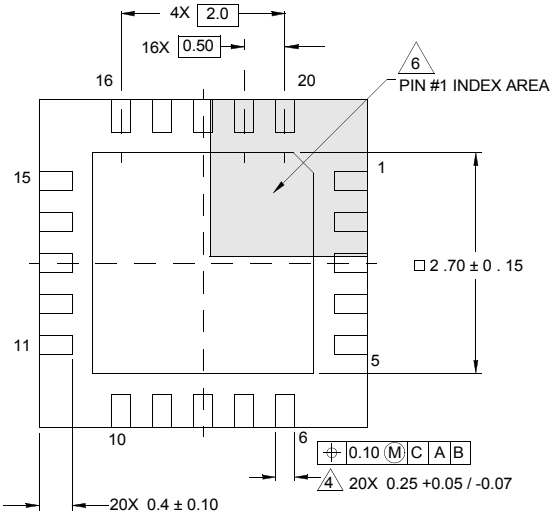
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing
L20.4x4C
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 11/06

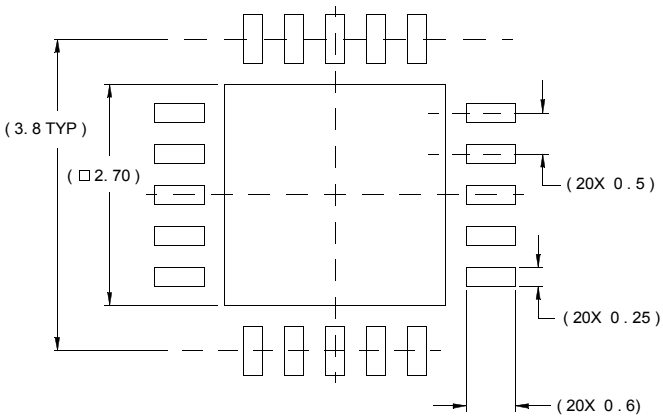
For the most recent package outline drawing, see L20.4x4C.



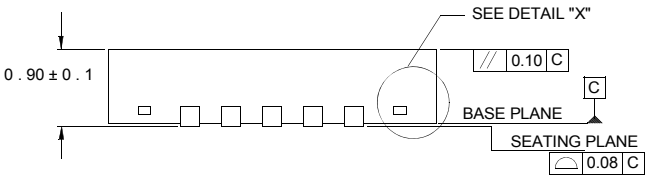
TOP VIEW



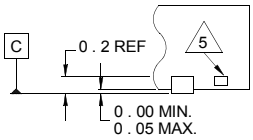
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.