

LTC3588-1/LTC3108/LTC3105/ LTC3459/LTC2935-2/LTC2935-4 Energy Harvesting (EH) Multisource Demo Board

DESCRIPTION

The **DC2042A** is a versatile energy harvesting demo board that is capable of accepting piezoelectric, solar, 4mA to 20mA loops, thermal-powered energy sources or any high impedance AC or DC source. The board contains four independent circuits consisting of the following EH ICs:

- **LTC[®]3588-1**: Piezoelectric Energy Harvesting Power Supply.
- **LTC3108**: Ultralow Voltage Step-Up Converter and Power Manager.
- **LTC3105**: Step-Up DC/DC Converter with Power Point Control and LDO Regulator.
- **LTC3459**: 10V Micropower Synchronous Boost Converter.
- **LTC2935-2/LTC2935-4**: Ultralow Power Supervisor with Power-Fail Output Selectable Thresholds.

The board supports the following interconnects:

- Direct connection with the Dust Mote demo boards, the DC9003A-B Mote on a chip or the DC9003A-A Manager on a chip.
- Energy Micro STK development kit.

In addition, many turrets are provided and one transducer header is available to make it easy to connect transducers to the board.

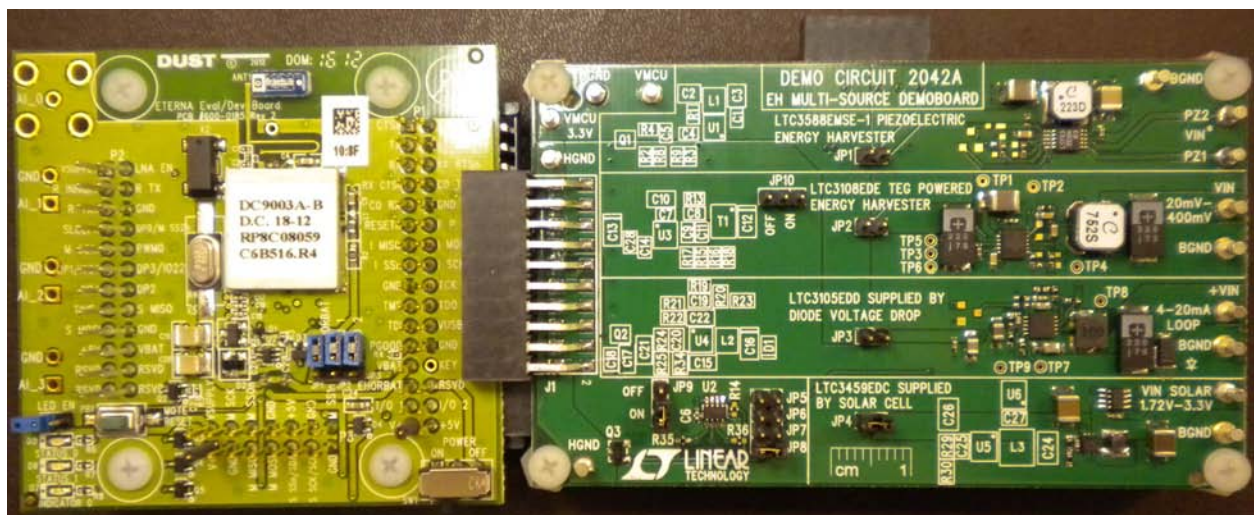
The board contains multiple jumpers that allow the board to be configured in various ways. The standard build for the board has three jumpers installed out of the possible 10 jumpers. The board is very customizable to the end users' needs. This compatibility makes it a perfect evaluation tool for any low power energy harvesting system

Please refer to the individual data sheets for the operation of each power management circuit. The application section of this demo manual describes the system level functionality of this board and the various ways it can be used in early design prototyping.

Design files for this circuit board are available at <http://www.linear.com/demo>

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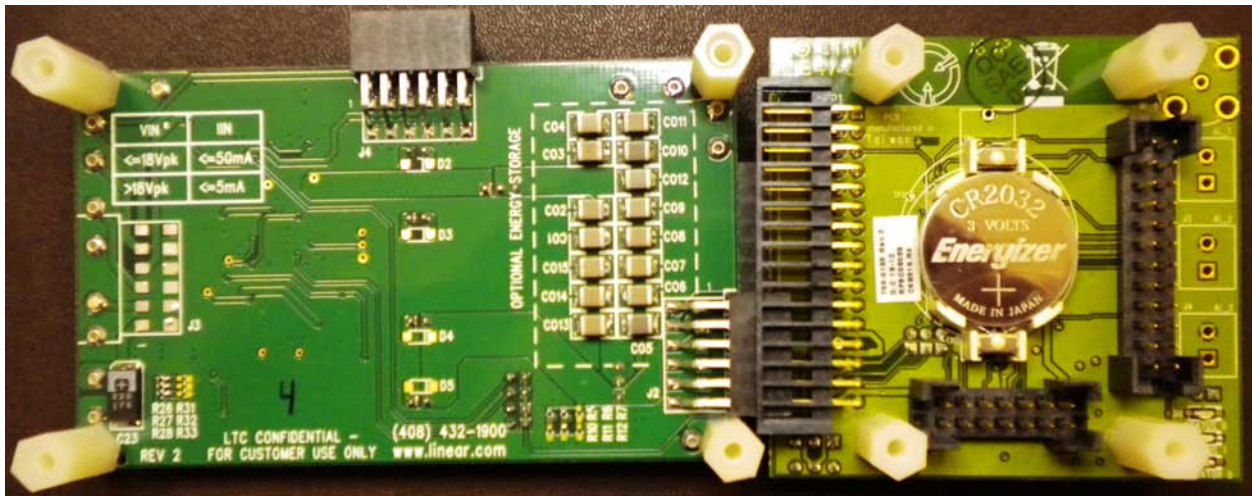
DC2042A Connected to DC9003A-B Dust Mote (Top View)



dc2042af

DESCRIPTION

DC2042A Connected to DC9003A-B Dust Mote (Bottom View)



QUICK START PROCEDURE

Refer to Figures 2 through 6 for the proper measurement equipment setup and jumper settings for the following test procedure.

1. Note the Header KEY locations that guarantee proper interconnect of compatible adaptor boards.
J1 (Energy Micro STK Header) does not have a KEY.
J2 (Dust Mote Header) has a KEY in position 5.
J3 (Horizontal Transducer Header, NOT INSTALLED on standard build) has a KEY in position 12.

J4 (Vertical Transducer Header) has a KEY in position 12.

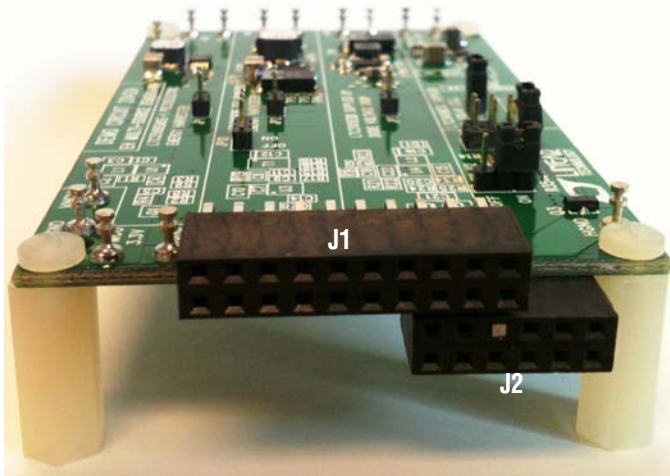


Figure 1a. J1, Energy Micro Header and J2, Dust Mote Header

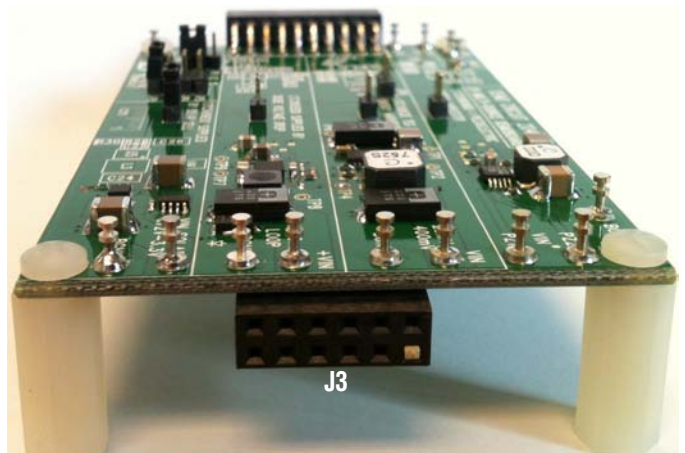


Figure 1b. J3, Horizontal Transducer Header

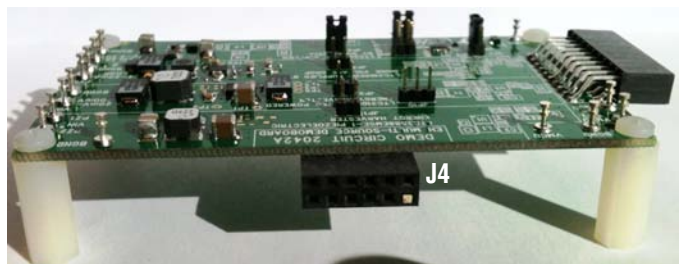


Figure 1c. J4, Vertical Transducer Header

QUICK START PROCEDURE

2. Configure the test equipment and jumpers as shown in Figure 2. Verify the jumper settings are as follows:
 - JP1.** OPEN
 - JP2.** OPEN
 - JP3.** OPEN
 - JP4.** OPEN
 - JP5.** OPEN
 - JP6.** OPEN
 - JP7.** OPEN
 - JP8.** INSTALLED
 - JP9.** INSTALLED in “ON” Position
 - JP10.** OPEN
3. Slowly increase PS1 and observe the voltage at which VM2 turns on. VM1 should be equal to approximately 3.15V.
4. Slowly decrease PS1 towards zero. Observe the voltage on VM1 at which VM2 drops rapidly to 0V. VM1 should be equal to approximately 2.25V.
5. Turn off PS1
6. Install JP4 and reconfigure the test equipment as shown in Figure 3 (Solar Circuit testing).
7. Disconnect PS2 and Set PS2 to 3.0V. Turn off PS2. Reconnect PS2 and turn on PS2.
8. Observe the voltage on VM1 and VM2. The voltage on VM1 should be approximately 2.49V and on VM2 should be 3.3V.
9. Turn off PS2
10. **MOVE JP4 to JP1.** Disconnect PS2 from the board. Set PS3 equal to 6.0V. Reconfigure the test equipment as shown in Figure 4.
11. Turn on PS3. Observe the voltage on VM1 and VM2. The voltage on VM1 should be approximately 5.77V and on VM2 should be 3.3V.
12. Use VM3 to observe the voltage on JP5-2. The voltage should be equal to the same level observed on VM2.
13. Turn off PS3
14. **MOVE JP1 to JP3.** Disconnect PS3 from the board and set PS4 equal to 5.0V. Reconfigure the test equipment as shown in Figure 5.
15. Turn on PS4. Observe the voltage on VM1 and VM2. The voltage on VM1 should be approximately 0.34V and on VM2 should be 3.3V.
16. Use VM3 to observe the voltage on JP7-2. The voltage should be approximately equal to the level observed on VM2.
17. Turn off PS4
18. **MOVE JP3 to JP2.** Disconnect PS4 from the board and set PS5 equal to 0.32V. Reconfigure the test equipment as shown in Figure 6.
19. Turn on PS5. Observe the voltage on VM1 and VM2. The voltage on VM1 should be approximately 0.14V and VM2 should be 3.3V.
20. Use VM3 to observe the voltage on JP6-2. The voltage should be approximately 2.0V.
21. Use VM3 to observe the voltage on JP10-1. The voltage should be approximately 5.0V.
22. Turn off PS5.
23. Reset the Jumpers as shown on Figure 7a.
 - JP1.** OPEN
 - JP2.** OPEN
 - JP3.** OPEN
 - JP4.** INSTALLED
 - JP5.** OPEN
 - JP6.** OPEN
 - JP7.** OPEN
 - JP8.** INSTALLED
 - JP9.** INSTALLED in “ON” Position
 - JP10.** OPEN

QUICK START PROCEDURE

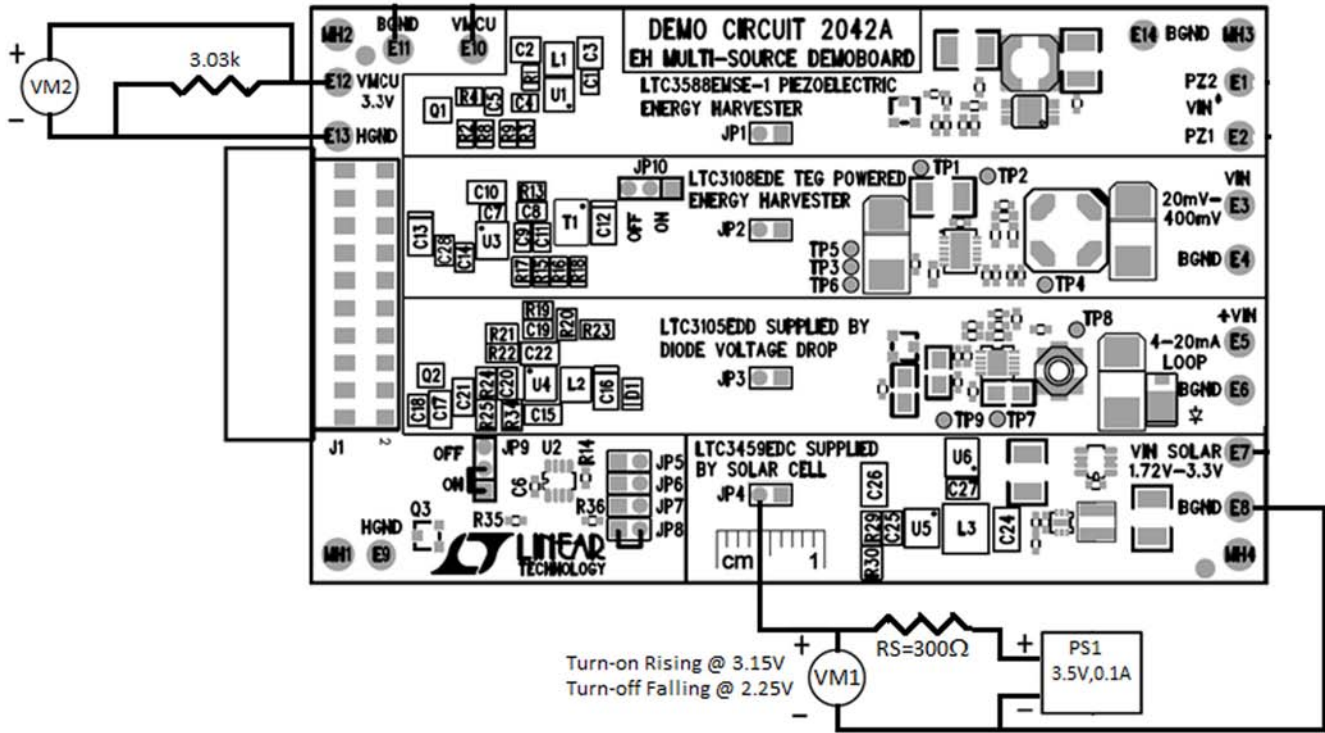


Figure 2. VMCU Power Switchover Test Setup (Test Steps 2 to 5)

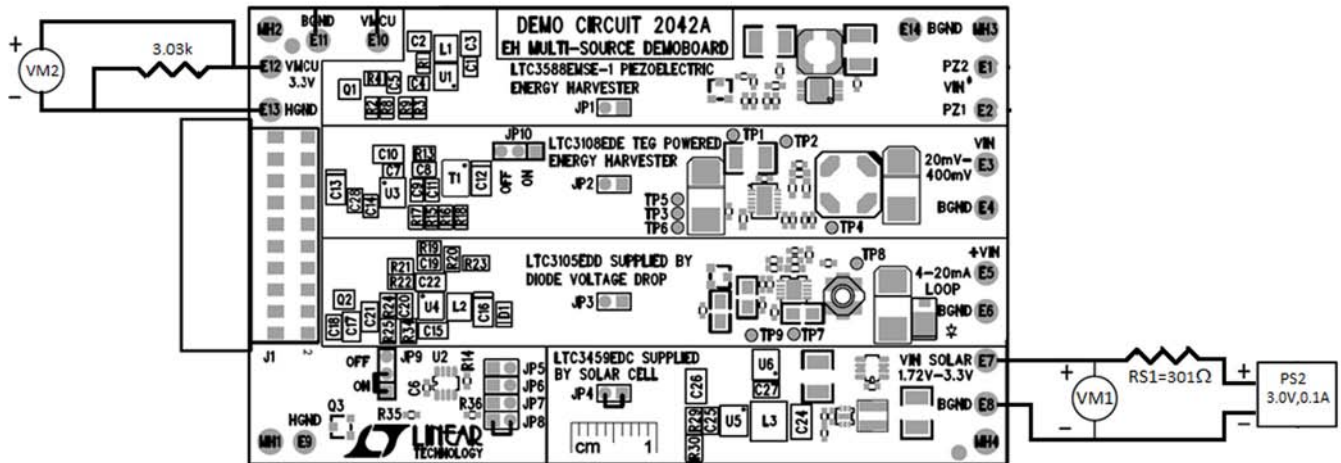


Figure 3. Solar Circuitry Test Setup (Test Steps 6 to 9) Proper Measurement Equipment Setup for DC2042A Solar Circuit Testing

QUICK START PROCEDURE

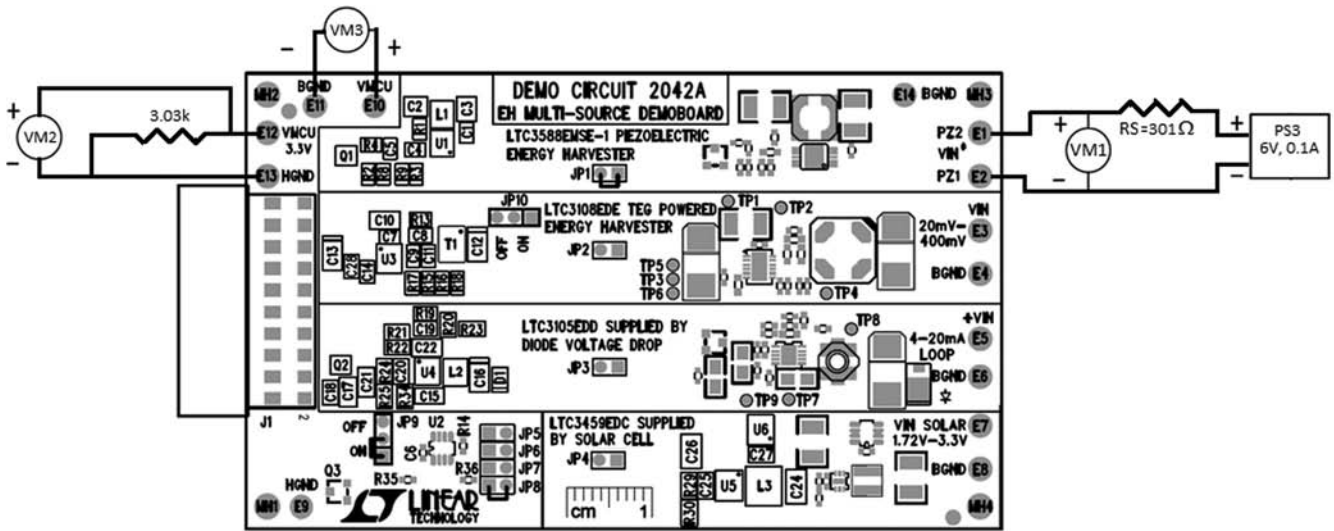


Figure 4. Piezoelectric Circuitry Test Setup (Test Steps 10 to 13)
 Proper Measurement Equipment Setup for DC2042A Piezoelectric Circuit Testing

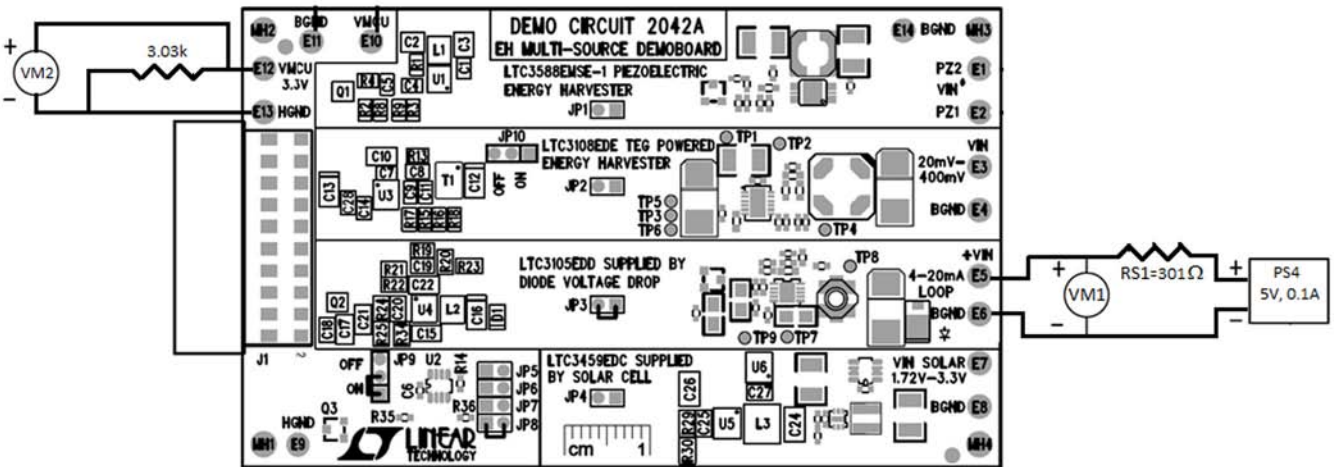


Figure 5. 4mA to 20mA Loop Circuitry Test Setup (Test Steps 14 to 17)
 Proper Measurement Equipment Setup for DC2042A 4mA to 20mA Loop Circuit Testing

QUICK START PROCEDURE

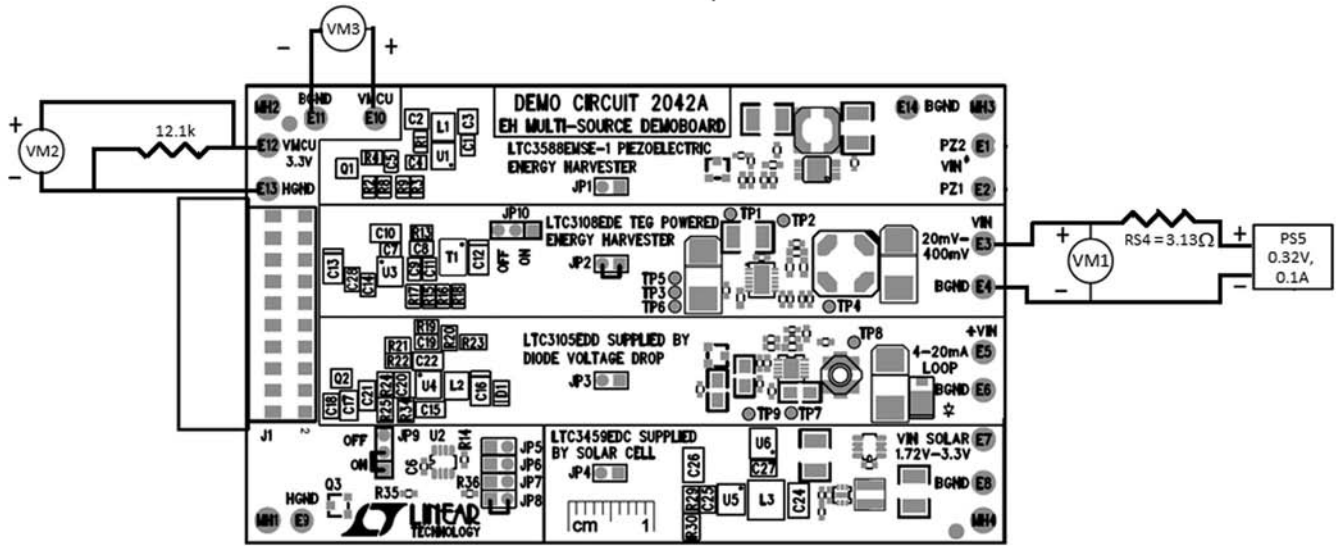


Figure 6. TEG-Powered Circuitry Test Setup (Test Steps 18 to 22)
Proper Measurement Equipment Setup for DC2042A TEG Circuit Testing

QUICK START PROCEDURE

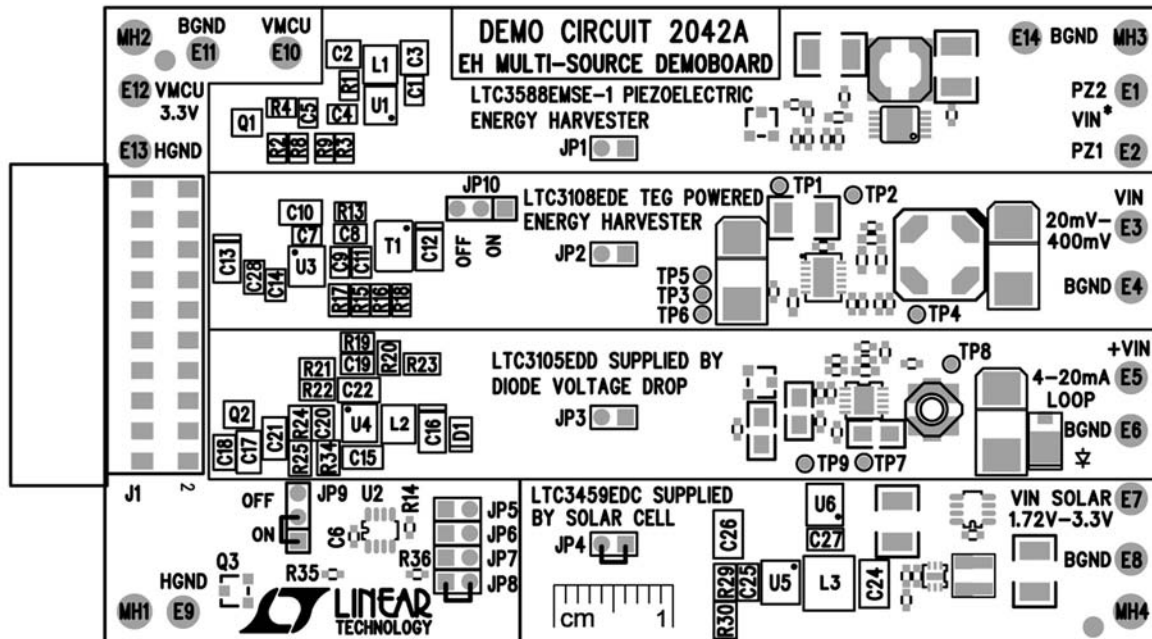


Figure 7a. DC2042A Top Assembly Drawing

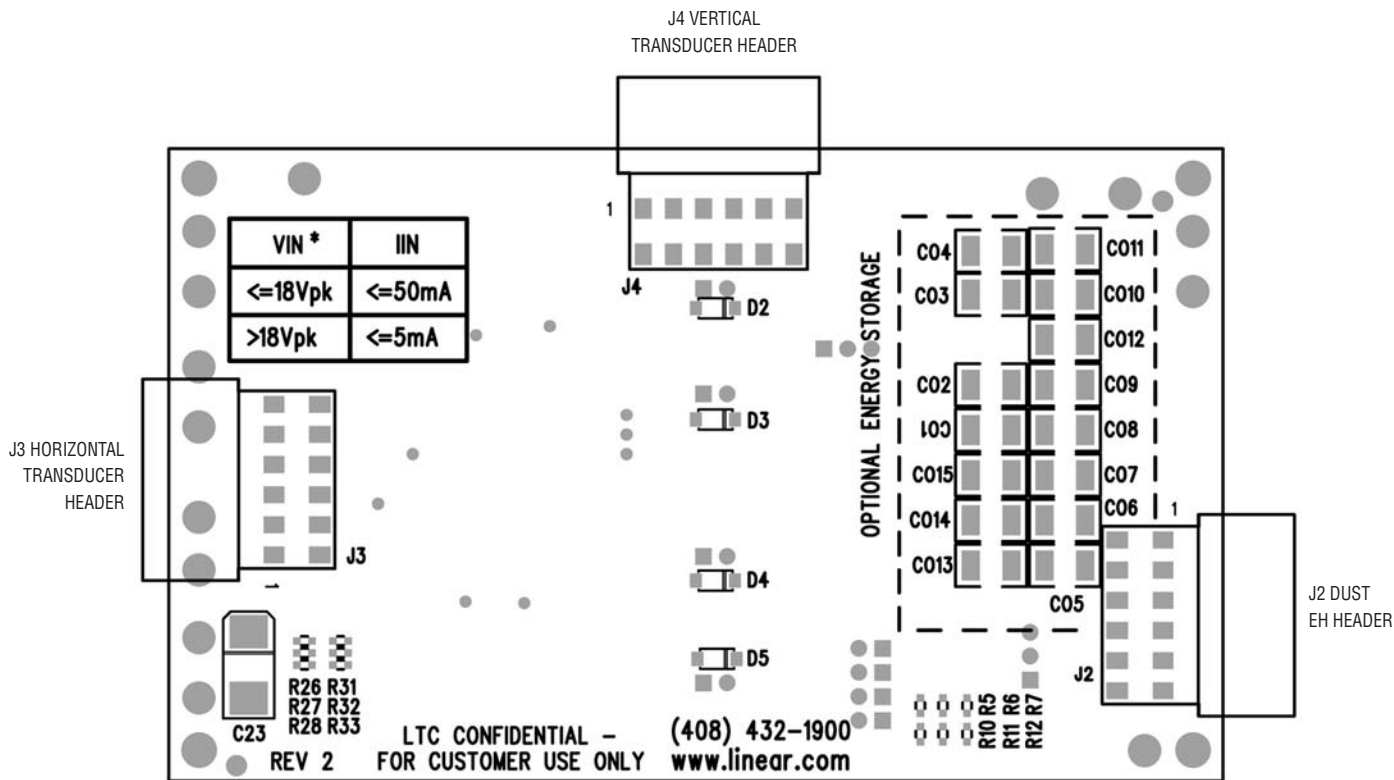


Figure 7b. DC2042A Bottom Assembly Drawings

APPLICATION INFORMATION

JUMPER FUNCTIONS

JP1: Power selection jumper used to select the LTC3588-1, piezoelectric energy harvesting power supply.

JP2: Power selection jumper used to select the LTC3108, TEG-powered energy harvester.

JP3: Power selection jumper used to select the LTC3105, powered by a diode voltage drop in a 4mA to 20mA loop.

JP4: Power selection jumper used to select the LTC3459, powered by a solar panel

JP5: Routes the LTC3588-1 PGOOD signal to the Dust Header PGOOD output. The LTC3588-1 PGOOD comparator produces a logic high referenced to VOUT on the PGOOD pin the first time the converter reaches the sleep threshold of the programmed VOUT, signaling that the output is in regulation. The PGOOD pin will remain high until VOUT falls to 92% of the desired regulation voltage. Additionally, if PGOOD is high and VIN falls below the UVLO falling threshold, PGOOD will remain high until VOUT falls to 92% of the desired regulation point. This allows output energy to be used even if the input is lost.

JP6: Routes the LTC3108 PGOOD signal to the Dust Header PGOOD output.

JP7: Routes the LTC3105 PGOOD signal to the Dust Header PGOOD output.

JP8: Routes the LTC3459 PGOOD signal to the Dust Header PGOOD output.

JP9: Connects the fifteen optional energy storage capacitors directly to VOUT (VSUPPLY of the Dust Header) to be used by the load to store energy at the output voltage level. The 100 μ F capacitors have a voltage coefficient of 0.61 of their labeled value at 3.3V and 0.47 at 5.25V. **Caution: Only JP9 or JP10 may be connected at any one time. Do not populate both JP9 AND JP10.**

JP10: Connects the fifteen optional energy storage capacitors directly to VSTORE of the LTC3108 TEG-powered energy harvester circuit, which is the output for the Storage capacitor or battery. A large capacitor may be connected from VSTORE to GND for powering the system in the event the input voltage is lost. It will be charged up to the maximum VAUX clamp voltage, typically 5.25V.

The 100 μ F capacitors have a voltage coefficient of 0.47 at 5.25V. **Caution: Only JP9 or JP10 may be connected at any one time. Do not populate both JP9 and JP10.**

Note: For this board to properly interface with a Dust Mote (DC9003A-B) or a Manager (DC9003A-A) board and switch the power from the battery to the energy harvesting source, resistor R3 on the Dust Mote board must be changed to 750k Ω and R4 must be changed to 5.1M Ω .

TURRET FUNCTIONS

PZ1 (E1): Input connection for piezoelectric element or other AC source (used in conjunction with PZ2). A high impedance DC source may be applied between this pin and BGND to power the LTC3588-1 circuit. **Caution: The maximum current into this pin is 50mA.**

PZ2 (E2): Input connection for piezoelectric element or other AC source (used in conjunction with PZ1). A high impedance DC source may be applied between this pin and BGND to power the LTC3588-1 circuit. **Caution: The maximum current into this pin is 50mA.**

VIN, 20mV to 400mV (E3): Input to the LTC3108, TEG-powered energy harvester. The input impedance of the LTC3108 power circuit is approximately 3 Ω , so the source impedance of the TEG should be less than 10 Ω to have good power transfer. TEGs with approximately 3 Ω will have the best power transfer. The input voltage range is 20mV to 400mV.

BGND (E4, E6, E8, E11, E14): This is the board ground. BGND is connected to all the circuits on the board except the headers. BGND and HGND, the header ground, are connected through Q3 when the VMCU voltage with respect to BGND reaches the rising RESET threshold of U2 and disconnected when VMCU falls to the falling reset threshold. The board is configured from the factory to connect BGND and HGND when VMCU equals 3.15V and disconnect them when VMCU equals 2.25V.

+VIN, 4mA to 20mA Loop (E5): Input to the LTC3105 supplied by a diode voltage drop. The current into this terminal must be limited to between 4mA and 20mA. The current into this turret flows through diode D1 to generate the diode voltage drop and into the LTC3105 power management circuit.

APPLICATION INFORMATION

VIN SOLAR (E7): Input to the LTC3459, solar-powered circuit with maximum power point control provided by the LTC2935-4. The input regulation point for the MPPC function is 1.73V. The input range is 1.72V to 3.3V.

HGND (E9, E13): This is the header ground. HGND is the switched ground to the headers that ensures the load is presented with a quickly rising voltage. BGND and HGND are connected through Q3 when the VMCU voltage with respect to BGND reaches the rising RESET threshold of U2 and disconnected when VMCU falls to the falling reset threshold. The board is configured from the factory to connect BGND and HGND when VMCU equals 3.15V and disconnect them when VMCU equals 2.25V.

VMCU (E10, E12): Regulated output of all the active energy harvester power management circuits, referenced to BGND. When VMCU is referenced to HGND it is a switched output that is passed through the headers, J1 and J2, to power the load.

J2 DUST HEADER SIGNALS

Pin 1 (VSUPPLY): Switched power from EH multisource demo board. As configured from the factory via the LTC2935-2 circuitry, this voltage is switched on at 3.15V and off at 2.25V. On the board this node is labeled VMCU.

Pin 2 (NC): No connect on EH multisource demo board.

Pin 3 (GND): Switched GND when VSUPPLY is greater than 3.15V, rising and 2.25V, falling. On the board this signal is labeled HGND.

Pin 4 (PGOOD): PGOOD signal from EH multisource demo board. When this signal is high, the SPDT switch on the DUST demo board will switch from the battery to the energy harvested source.

Pin 5 (KEY): Metal insert in header to ensure proper insertion location and orientation. No electrical connection.

Pin 6 (VBAT): Raw battery voltage from (to) DUST board.

Pin 7 (RSVD): Reserved for future use, no connection on EH multisource board.

Pin 8 (EHORBAT): Signal indicating if the battery or the energy harvester is providing power to the system. Refer to the individual device data sheet for the interpretation of the polarity.

Pin 9 (I/O 2): Connected to general purpose I/O input on DUST DC9003A-X.

Pin 10 (I/O 1): Connected to general purpose I/O input on DUST DC9003A-X.

Pin 11 (+5V): 5V input provided by DC9006A board, not anticipated to be used by or provided from EH board.

Pin 12 (V+): 12V input provided by DC9006A board, not anticipated to be used by or provided from eh board.

J3 AND J4 TRANSDUCER HEADER SIGNALS

Pin 1 (VIN_LTC3459): Solar panel input. The allowable range for this input voltage is 1.72V to 3.3V.

Pins 2, 4, 6, 8, 10 (GND): Connected to board ground "BGND" to power the power management circuits.

Pin 3 (VIN_LTC3105): Connect in series with 4mA to 20mA loop. The Loop current will flow into this pin and out a board GND connection.

Pin 5 (VIN_LTC3108): Thermal electric generator input, input to step-up transformer. The allowable range for this input voltage is 20mV to 400mV. The source impedance of the TEG should be less than 10Ω for good power matching.

Pin 7 (VIN_LTC3588-1): Rectified AC voltage, direct input to LTC3588-1 DC/DC. The allowable range for this input voltage is 5V to 18V. If the DC source is greater than 18V, the maximum current allowed into this pin is 5mA.

Pin 9 (PZ1): Raw battery voltage from (to) the DC9003A-X DUST board.

Pin 11 (PZ2): Reserved for future use, no connection on EH multisource board.

Pin 12 (KEY): Metal insert in header to ensure proper insertion location and orientation. No electrical connection.

APPLICATION INFORMATION

LTC3588-1: PIEZOELECTRIC ENERGY HARVESTING POWER SUPPLY (VIBRATION OR HIGH IMPEDANCE AC SOURCE)

The LTC3588-1 piezoelectric energy harvesting power supply is selected by installing the power selection jumper, JP1. The PGOOD signal can be routed to the Dust Header by installing jumper JP5. The Dust Eterna board will switch from battery power to energy harvester power whenever the PGOOD signal is high, **provided that resistor R3 on the Dust Mote board (DC9003A-B) is changed to 750kΩ and R4 is changed to 5.1MΩ.**

If the application requires a wide hysteresis window for the PGOOD signal, the board has the provision to use the independent PGOOD signal, shown in Figure 12, generated by the LTC2935-2 and available on JP8. This signal is labeled as the PGOOD signal for the LTC3459 circuit (PGOOD_LTC3459), because the LTC3459 does not have its own PGOOD output. The PGOOD_LTC3459 signal can be used in place of any of the PGOOD signals generated by the harvester circuits. **The board is configured from the factory to use the PGOOD_LTC3459 signal as the PGOOD signal to switch from battery power to energy harvesting power.**

The PGOOD_LTC3459 signal is always used to switch the output voltage on the header. Some loads do not like to see a slowly rising input voltage. Switch Q3 ensures that VSUPPLY and VMCU on the headers are off until the energy harvested output voltage is high enough to power the load. The LTC2935-2 is configured to turn on Q3 at 3.15V and turn off Q3 at 2.25V. With this circuit, the load will see a fast voltage rise at start-up and be able to utilize all the energy stored in the output capacitors between the 3.15V and 2.25V levels.

The optional components R1, R4, Q1 and C5 shown on the schematic are not populated for a standard assembly. The function of R1, R4, Q1 and C5 is to generate a short PGOOD pulse that will indicate when the output capacitor is charged to its maximum value. The short pulse occurs every time the output capacitor charges up to the “output sleep threshold,” which for a 3.3V output is 3.312V. By populating these components the application can use this short pulse as a sequence timer to step through the program sequence or as an indication of when it can perform energy-intensive functions, such as a sensor read or a wireless transmission and/or receive, knowing precisely how much charge is available in the output capacitors. When this optional circuit is not used, the amount of charge in the output capacitors is anywhere between the maximum ($C_{OUT} \cdot V_{OUT_SLEEP}$) to eight percent low. In the case where the energy harvesting source can support the average load continuously, this optional circuit is not needed.

Diode D2 is an optional component used to “Diode-OR” multiple energy harvesting sources together. This diode would be used in conjunction with one or more of the other Oring diodes, D3, D4 or D5. When the Oring diodes are installed the parallel jumper would not be populated. The diode drop will be subtracted from the output voltage regulation point, so it is recommended to change the feedback resistors or select a higher output voltage setpoint to compensate for the diode drop. When more than one of these diodes is installed and the associated energy harvester inputs are powered, the board will switch between energy harvester power circuits as needed to maintain the output voltage.

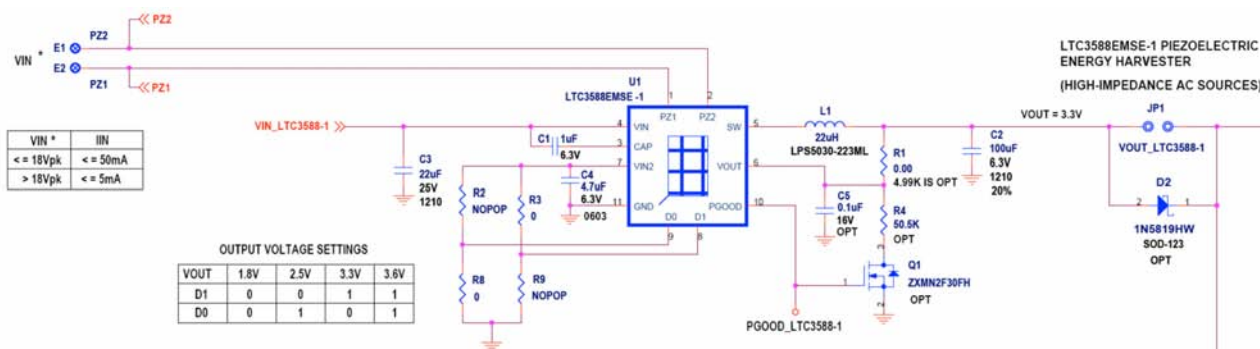


Figure 8. Detailed Schematic of LTC3588-1 Piezoelectric Energy Harvesting Power Supply

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APPLICATION INFORMATION

LTC3108: TEG-POWERED ENERGY HARVESTER

The LTC3108 TEG-powered energy harvester is selected by installing the power selection jumper JP2. The PGOOD signal, PGOOD_LTC3108, can be routed to the Dust Header by installing jumper JP6. The LTC3108 PGOOD signal is pulled up to the on-chip 2.2V LDO through a 1MΩ pull-up resistor. The Dust Eterna board will switch from battery power to energy harvester power whenever the PGOOD_LTC3108 signal is high. **Provided that, R4, on the Dust Mote demo board, DC9003A-B, is changed to 5.1MΩ.**

If the application requires a wide hysteresis window for the PGOOD signal, please refer to the above section for a complete operational description of and how to use the independent PGOOD signal (PGOOD_LTC3459), shown in Figure 12, generated by the LTC2935-2 and available on JP8.

The PGOOD_LTC3459 signal is always used to switch the output voltage on the header. Some loads do not like to see a slowly rising input voltage. Switch Q3 ensures that VSUPPLY and VMCU on the headers are off until the energy harvested output voltage is high enough to power the load.

When the PGOOD signal from the LTC3108 is used as the header signal, the setpoint for the LTC2935-2 circuit

needs to be changed so the turn-on threshold is below the PGOOD_LTC3108 turn-on threshold of 3.053V. For example, by changing R36 to a 0Ω jumper and R5 to “NOPOP”, the turn-on threshold for Q3 will be 2.99V rising and 2.25V falling.

The single supply SPDT analog switch, ISL43L210, on the Dust Mote needs a digital input voltage greater than 1.4V to consider it a “Logic 1” and switch from the battery to the energy harvester-powered source. When using the PGOOD signal from the LTC3108, the pull-down resistor, R4, on the Dust Mote demo board, DC9003A-B, should be changed to 5.1MΩ to avoid creating a resistor divider with the internal 1MΩ LTC3108 PGOOD pull-up resistor.

Diode D3 is an optional component used to “Diode-OR” multiple energy harvesting sources together. This diode would be used in conjunction with one or more of the other Oring diodes, D2, D4 or D5. When the Oring diodes are installed the parallel jumper would not be populated. The diode drop will be subtracted from the output voltage setpoint, so it is recommended to change the feedback resistors or select a higher output voltage setpoint to compensate for the diode drop. When more than one of these diodes is installed and the associated energy harvester inputs are powered, the board will switch between energy harvester power circuits as needed to maintain the output voltage.

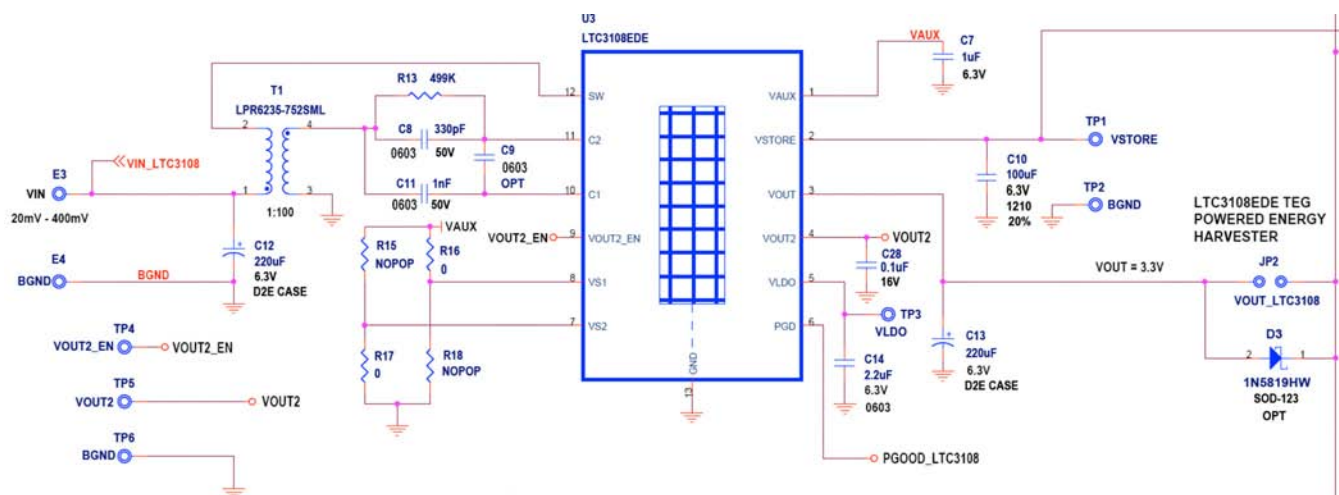


Figure 9. Detailed Schematic of LTC3108 TEG-Powered Energy Harvester

APPLICATION INFORMATION

LTC3105: SUPPLIED BY DIODE VOLTAGE DROP IN 4mA TO 20mA LOOP

The LTC3105 4mA to 20mA loop, diode voltage drop-powered energy harvester is selected by installing the power selection jumper, JP3. The PGOOD signal, PGOOD_LTC3105, can be routed to the Dust Header by installing jumper JP7. The PGOOD_LTC3105 signal is an open-drain output. The pull-down is disabled at the beginning of the first sleep event after the output voltage has risen above 90% of its regulation value. PGOOD_LTC3105 remains asserted until VOUT drops below 90% of its regulation value at which point PGOOD_LTC3105 will pull low. The pull-down is also disabled while the IC is in shutdown or start-up mode. The Dust Eterna board will switch from battery power to energy harvester power whenever the PGOOD signal is high (>1.4V). Again a resistor divider is generated by the pull-up resistor R23 on the DC2042A and R4, the pull-down resistor on the DC9003A-A or DC9003A-B. Provided that R4 is changed as described above to 5.1MΩ, the voltage seen by the analog switch will be sufficient to register as a “Logic 1” and switch the Mote or Manager from the battery to the energy harvested source.

If the application would benefit from a wider PGOOD hysteresis window than the LTC3105 provides (sleep to V_{OUT} minus 10%), please refer to the above section for a complete operational description of and how to use the independent PGOOD signal (PGOOD_LTC3459), shown in Figure 12, generated by the LTC2935-2 and available on JP8.

The PGOOD_LTC3459 signal is always used to switch the output voltage on the Header. Some loads do not like to see a slowly rising input voltage. Switch Q3 ensures that VSUPPLY and VMCU on the headers are off until the energy harvested output voltage is high enough to power the load.

The PGOOD_LTC3459 signal can be used in place of any of the PGOOD signals generated by the harvester circuits.

The optional components shown on the schematic are not populated for a standard assembly. The function of R22 and Q2 is to generate a short PGOOD pulse that will indicate when the output capacitor is charged to its maximum value. The short pulse occurs every time the output capacitor charges up to the “output sleep threshold”, which for a 3.3V output is 3.312V. By populating these components the application can use this short pulse as a sequence timer to step through the program sequence or as an indication of when it can perform energy intensive functions, such as a sensor read or a wireless transmission and/or receive, knowing precisely how much charge is available in the output capacitors. When this optional circuit is not used, the amount of charge in the output capacitors is anywhere between the maximum ($C_{OUT} \cdot V_{OUT_SLEEP}$) to ten percent low. In the case where the energy harvesting source can support the average load continuously, this optional circuit is not needed.

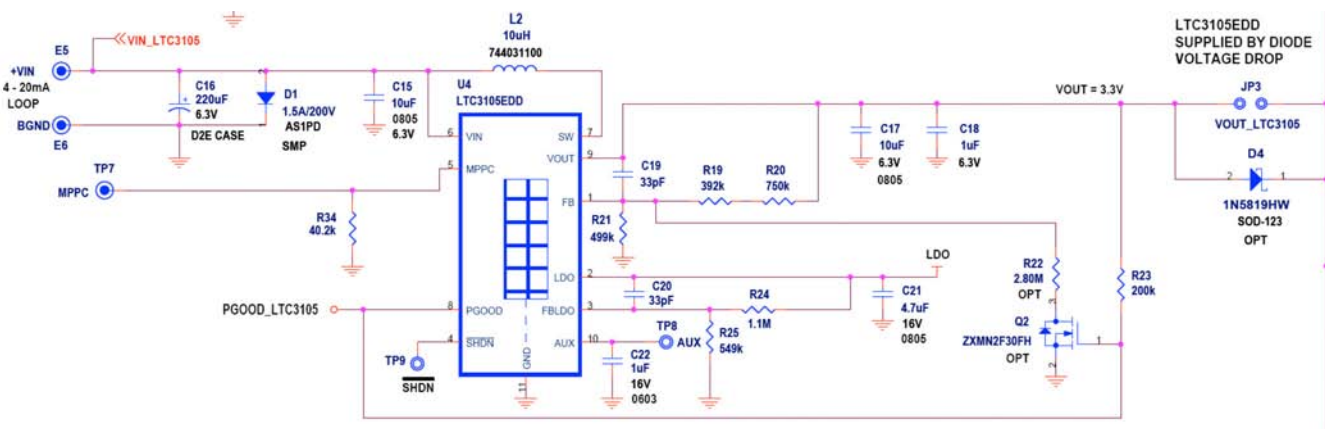


Figure 10. Detailed Schematic of LTC3105 4mA to 20mA Loop, Diode Voltage Drop Energy Harvester

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APPLICATION INFORMATION

Diode D4 is an optional component used to “Diode-OR” multiple energy harvesting sources together. This diode would be used in conjunction with one or more of the other Oring diodes, D2, D3 or D5. When the Oring diodes are installed the parallel jumper would not be populated. The diode drop will be subtracted from the output voltage setpoint so it is recommended to change the feedback resistors or select a higher output voltage setpoint to compensate for the diode drop. When more than one of these diodes is installed and the associated energy harvester inputs are powered, the board will switch between energy harvester power circuits as needed to maintain the output voltage.

LTC3459 SUPPLIED BY SOLAR CELL

The LTC3459 solar-powered energy harvester is selected by installing the power selection jumper, JP4. The PGOOD signal, PGOOD_LTC3459, can be routed to the Dust Header by installing jumper JP8.

The LTC2935-4 adds a hysteretic input voltage regulation function to the LTC3459 application circuit. The PFO output of the LTC2935-4 is connected to the $\overline{\text{SHDN}}$ input on the LTC3459, which means that the LTC3459 will be off until VIN_LTC3459 rises above 1.743V (1.72V + 2.5%) and will then turn off when VIN_LTC3459 falls below 1.72V. The result is that the input voltage to the LTC3459 circuit will be regulated to 1.73V, the average of the LTC2934-4 rising and falling PFO thresholds. The threshold can be adjusted for the peak operating point of the solar panel selected. In this design, because the LTC3459 output is set to 3.3V and is a boost topology, the input voltage is limited to 3.3V.

The LTC3459 does not have an internally generated PGOOD signal so the LTC2935-2 was used to generate a PGOOD function with an adjustable hysteresis window. The NOPOP and 0 Ω resistors around the LTC2935-2 allow

for customization of the PGOOD thresholds and hysteresis window. By using R14, R35 and R36 the inputs can be changed after the rising threshold is reached, creating a large hysteresis window.

The PGOOD_LTC3459 signal can be used in place of any of the PGOOD signals generated by the harvester circuits. The PGOOD_LTC3459 signal is always used to switch the output voltage on the header. **The board is configured from the factory to use the PGOOD_LTC3459 signal as the PGOOD signal to switch from battery power to energy harvesting power.**

The PGOOD_LTC3459 signal is always used to switch the output voltage on the header. Some loads do not like to see a slowly rising input voltage. Switch Q3 ensures that VSUPPLY and VMCU on the headers are off until the energy harvested output voltage is high enough to power the load. The LTC2935-2 is configured to turn on Q3 at 3.15V and turn off Q3 at 2.25V. With this circuit, the load will see a fast voltage rise at start-up and be able to utilize all the energy stored in the output capacitors between the 3.15V and 2.25V levels.

Diode D4 is an optional component used to “Diode-OR” multiple energy harvesting sources together. This diode would be used in conjunction with one or more of the other Oring diodes, D2, D3 or D5. When the Oring diodes are installed the parallel jumper would not be populated. The diode drop will be subtracted from the output voltage setpoint, so it is recommended to change the feedback resistors or select a higher output voltage setpoint to compensate for the diode drop. When more than one of these diodes is installed and the associated energy harvester inputs are powered, the board will switch between energy harvester power circuits as needed to maintain the output voltage.

APPLICATION INFORMATION

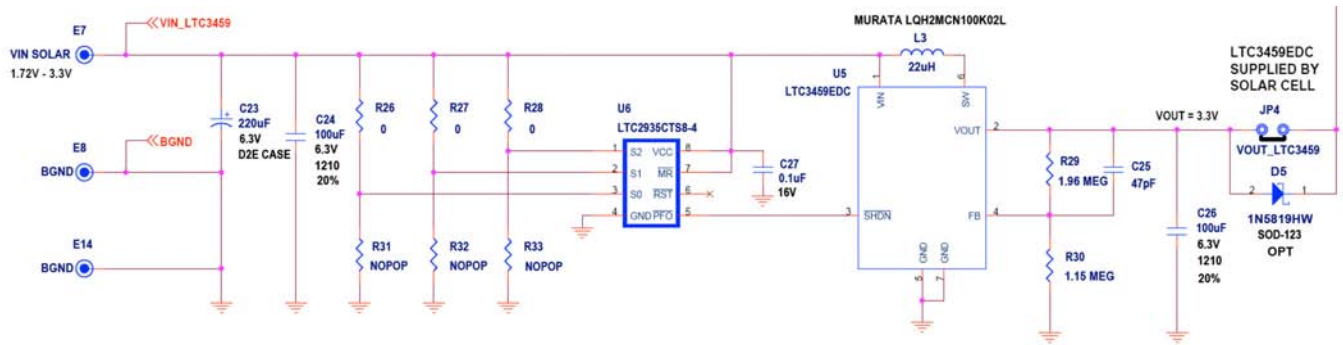


Figure 11: Detailed Schematic of LTC3459 Supplied by a Solar Cell

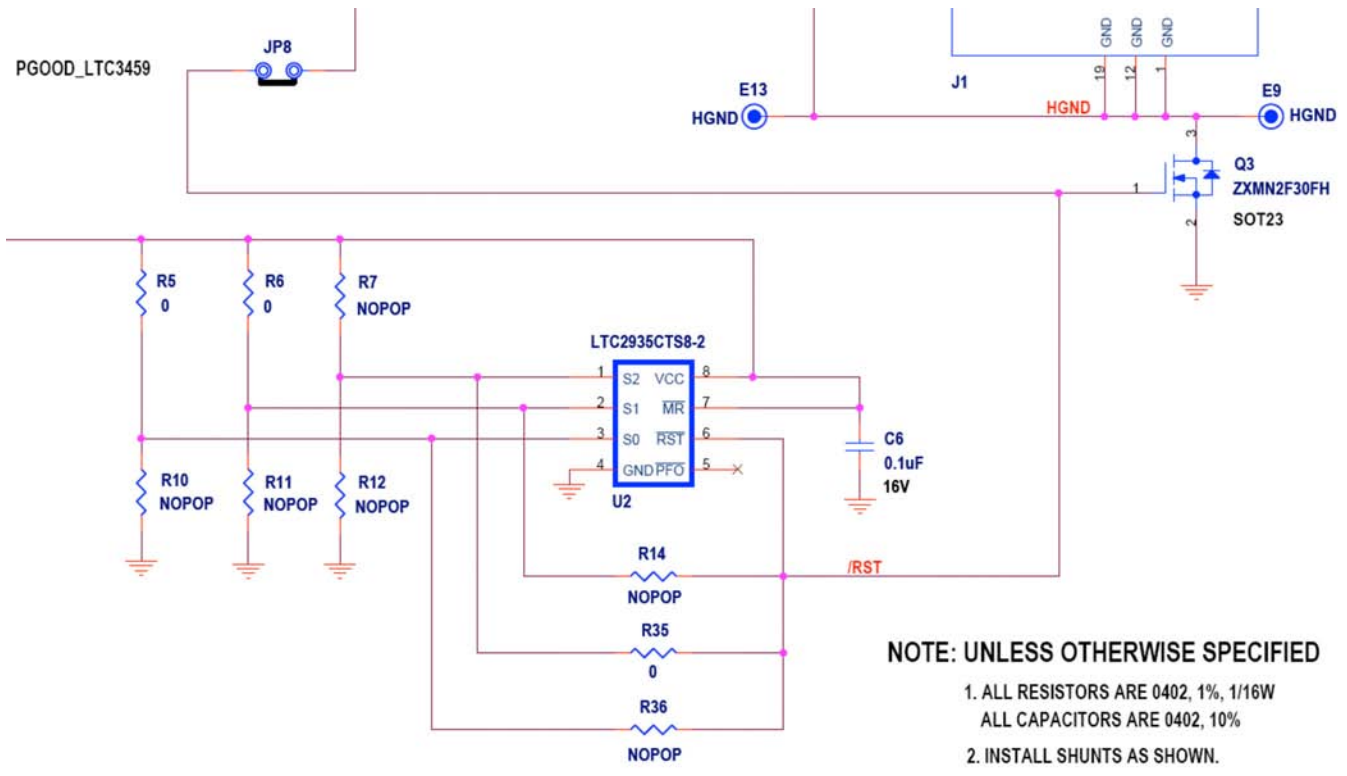


Figure 12: Detailed Schematic of PGOOD_LTC3459 Circuit Using LTC2935-2

APPLICATION INFORMATION

SAMPLE OPERATION OF THE LTC3459 CIRCUIT WITH VARYING LIGHT LEVELS IN A WIRELESS MESH NETWORK APPLICATION.

Figure 13 shows a demonstration system using the DC2042A EH multisource demo board connected to a DC9003A-B Dust Mote, all powered by a G24i, Indy4100 solar panel and a CR2032 primary cell lithium-ion battery. The G24i Indy4100 solar panel has four lanes and is 100mm long. The system will duty cycle the battery use as needed when the light level is insufficient to power the wireless sensor node continuously. The scope photos show in Figures 14 through 17 how the supply voltage on the DC9003A-B is switched between the energy harvested power (3.312V – 2.25V) and the battery voltage (3.0V). In this way the life of the battery is extended as much as possible.

Legend for (Figures 14 to 17):

- 1) The ground for the probes is referenced to the GND on the mote board.
- 2) Probe Signals:
 - a) GREEN = VMCU on the EH Board (J2-1 on DC2042A)
 - b) YELLOW = PGOOD_LTC3459 (J2-4 on DC2042A)
 - c) BLUE = VBAT on Mote Board or (J2-6 on DC2042A)
 - d) PINK = VSUPPLY (P2 -1 on Mote Board)



Figure 13. Solar Powered DC2042A in a MESH Wireless Sensor Network

APPLICATION INFORMATION

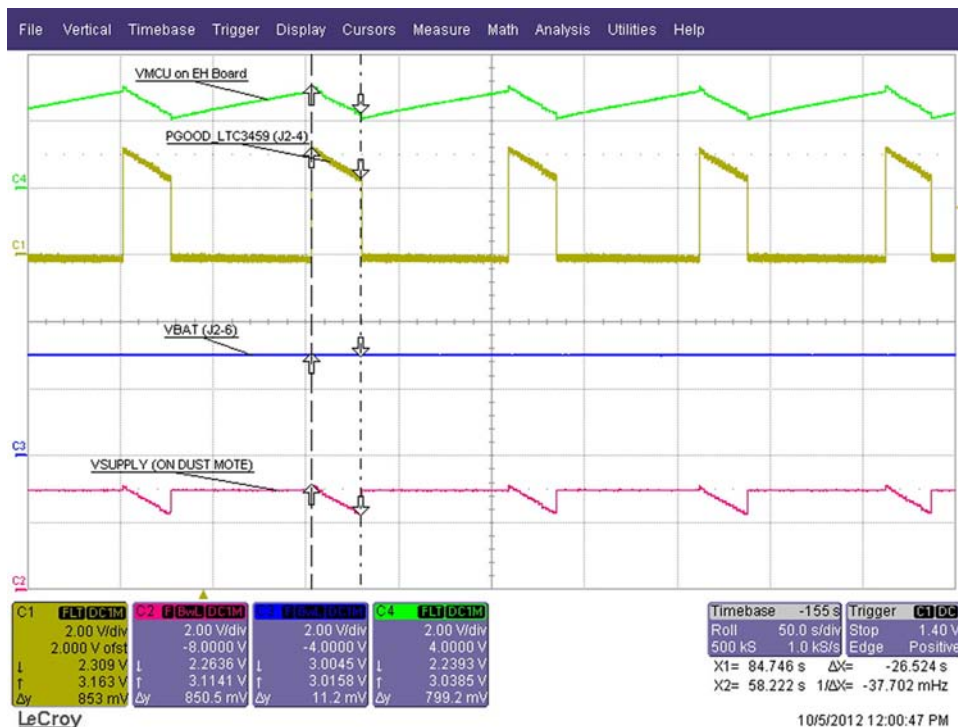


Figure 14: DC2042A LTC3459 Operation at 100 lux with Indy4100 Solar Panel

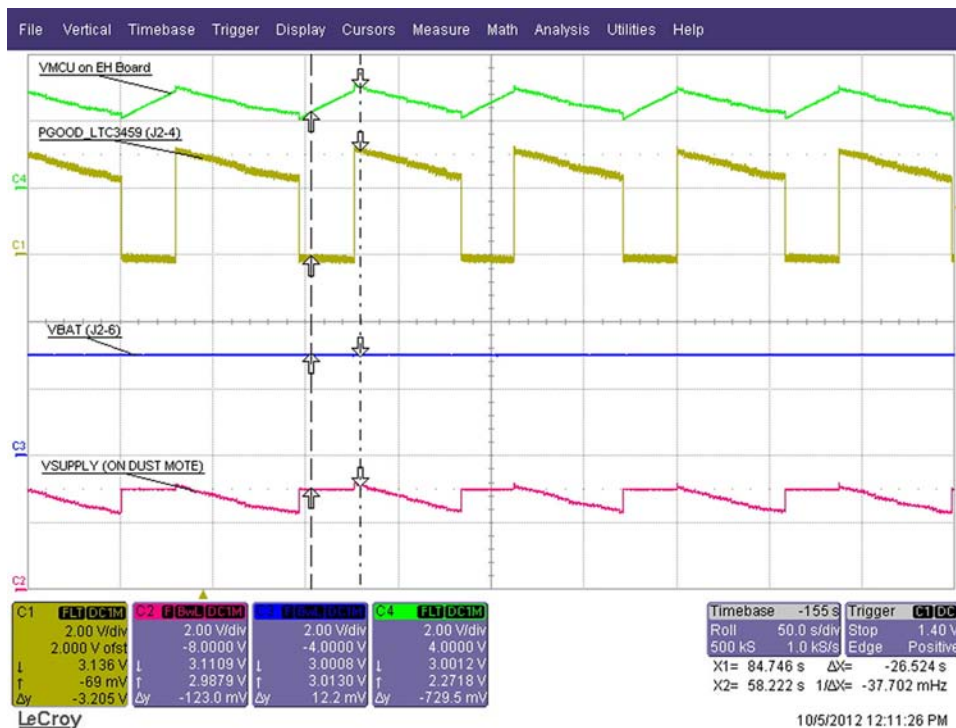


Figure 15: DC2042A LTC3459 Operation at 210 lux with Indy4100 Solar Panel

APPLICATION INFORMATION



Figure 16. DC2042A LTC3459 Operation at 275 lux with Indy4100 Solar Panel

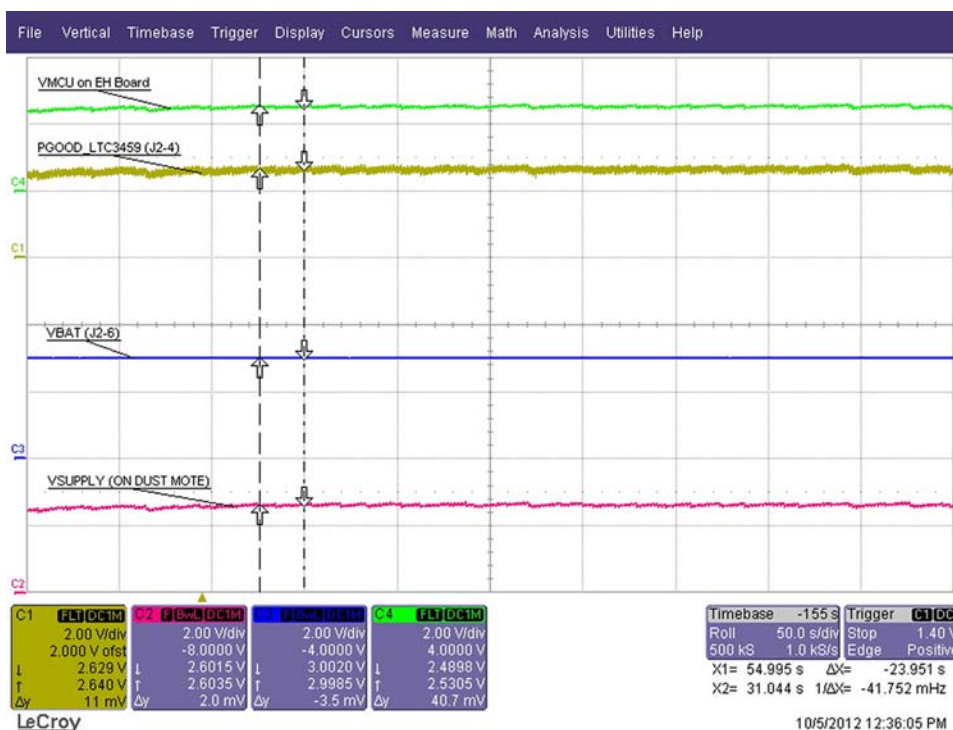


Figure 17. DC2042A LTC3459 Operation at 300 lux with Indy4100 Solar Panel

DEMO MANUAL DC2042A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	3	C1, C7, C18	CAP, CHIP, X5R, 1 μ F, 10%, 6.3V, 0402	TDK, C1005X5R0J105KT
2	4	C2, C10, C24, C26	CAP, CHIP, X5R, 100 μ F, 20%, 10V, 1210	TAIYO YUDEN, LMK325ABJ107MM
	15	C01-C015 (OPTIONAL ENERGY STORAGE)		
3	1	C3	CAP, CHIP, X5R, 22 μ F, 10%, 25V, 1210	AVX, 12103D226KAT2A
4	1	C4	CAP, CHIP, X5R, 4.7 μ F, 10%, 6.3V, 0603, Height = 0.80mm	TDK, C1608X5R0J475K/0.80
5	3	C6, C27, C28	CAP, CHIP, X7R, 0.1 μ F, 10%, 16V, 0402	MURATA, GRM155R71C104KA88D
6	1	C8	CAP, CHIP, X7R, 330pF, 50V, 10%, 0603	MURATA, GRM188R71H331KA01D
7	1	C11	CAP, CHIP, X7R, 1000pF, 50V, 10%, 0603	MURATA, GRM188R71H102KA01D
9	4	C12, C13, C16, C23	CAP, POLYMER SMD, 220 μ F, 6.3V, 18m Ω , 2.8Arms, D2E CASE	SANYO, 6TPE220MI
10	1	C14	CAP, CHIP, X5R, 2.2 μ F, 16V, 10%, 0603	MURATA, GRM188R61C225KE15D
11	2	C15, C17	CAP, CHIP, X5R, 10 μ F, 10%, 6.3V, 0805	AVX, 08056D106KAT2A
12	2	C19, C20	CAP, CHIP, NPO, 33pF, 5%, 25V, 0402	AVX, 04023A330JAT2A
13	1	C21	CAP, CHIP, X5R, 4.7 μ F, 10%, 16V, 0805	TAIYO YUDEN, EMK212BJ475MG-T
14	1	C22	CAP, CHIP, X5R, 1 μ F, 10%, 16V, 0603	AVX, 0603YD105KAT2A
15	1	C25	CAP, CHIP, NPO, 47pF, 5%, 25V, 0402	AVX, 04023A470JAT2A
16	1	D1	DIODE, STANDARD, 200V, 1.5A, SMP	VISHAY, AS1PD-M3/84A
17	1	L1	INDUCTOR, 22 μ H, 0.78A, 190m Ω , 4.8mm x 4.8mm	COILCRAFT, LPS5030-223MLB
18	0	L1 (OPT)	INDUCTOR, 22 μ H, 0.70A, 185m Ω , 4.8mm x 4.8mm	WURTH, 744043220
19	1	L2	INDUCTOR, 10 μ H, 560mA, 0.205 Ω , 3.8mm x 3.8mm	WURTH, 744031100
20	0	L2 (OPT)	INDUCTOR, 10 μ H, 650mA, 0.205 Ω , 3.8mm x 3.8mm	SUMIDA, CDRH3D18NP-100N
21	1	L3	INDUCTOR, 22 μ H, 185mA, 2.1 Ω , 0806	MURATA, LQH2MCN220K02L
22	0	L3 (OPT)	INDUCTOR, 22 μ H, 270mA, 1.48 Ω , 2.8mm x 2.87mm	WURTH, 744028220
23	1	T1	TRANSFORMER, 100:1 TURNS RATIO	COILCRAFT, LPR6235-752SMLC
24	0	T1 (OPT)	TRANSFORMER, 100:1 TURNS RATIO	WURTH, 74488540070
25	1	Q3	N-CHANNEL MOSFET, 20V, SOT23	DIODES/ZETEX, ZXMN2F30FHFA
27	11	R1, R3, R5, R6, R8, R16, R17, R26, R27, R28, R35	RES, CHIP, 0 Ω JUMPER, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
28	2	R13, R21	RES, CHIP, 499k, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW0402499KFKED
29	1	R19	RES, CHIP, 392K Ω , \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW0402392KFKED
30	1	R20	RES, CHIP, 750k, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW0402750KFKED
31	1	R23	RES, CHIP, 200k, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW0402200KFKED
32	1	R24	RES, CHIP, 1.10M, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW04021M10FKED
33	1	R25	RES, CHIP, 549k, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW0402549KFKED
34	1	R29	RES, CHIP, 1.96M, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW04021M96FKED
35	1	R30	RES, CHIP, 1.15M, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW04021M15FKED
36	1	R34	RES, CHIP, 40.2k, \pm 1%, 1/16W, 0402, \pm 100ppm/ $^{\circ}$ C	VISHAY, CRCW040240K2FKED
37	1	U1	PIEZOELECTRIC ENERGY HARVESTING POWER SUPPLY, DFN 3mm x 3mm	LINEAR TECH., LTC3588EMSE-1
38	1	U2	IC, ULTRALOW POWER SUPERVISOR WITH POWER-FAIL OUTPUT, TSOT-23, 8-PIN	LINEAR TECH., LTC2935CTS8-2

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
39	1	U3	IC, ULTRALOW VOLTAGE STEP-UP CONVERTER AND POWER MANAGER, DFN 3mm x 4mm	LINEAR TECH., LTC3108EDE
40	1	U4	IC, 400mA STEP-UP DC/DC CONVERTER WITH MPPC AND 250mV START-UP, DFN 3mm x 3mm	LINEAR TECH., LTC3105EDD
41	1	U5	IC, 10V MICROPOWER SYNC BOOST CONVERTER, DFN 2mm X 2mm	LINEAR TECH., LTC3459EDC
42	1	U6	IC, ULTRALOW POWER SUPERVISOR WITH POWER-FAIL OUTPUT, TSOT-23, 8-PIN	LINEAR TECH., LTC2935CTS8-4

Additional Demo Board Circuit Components

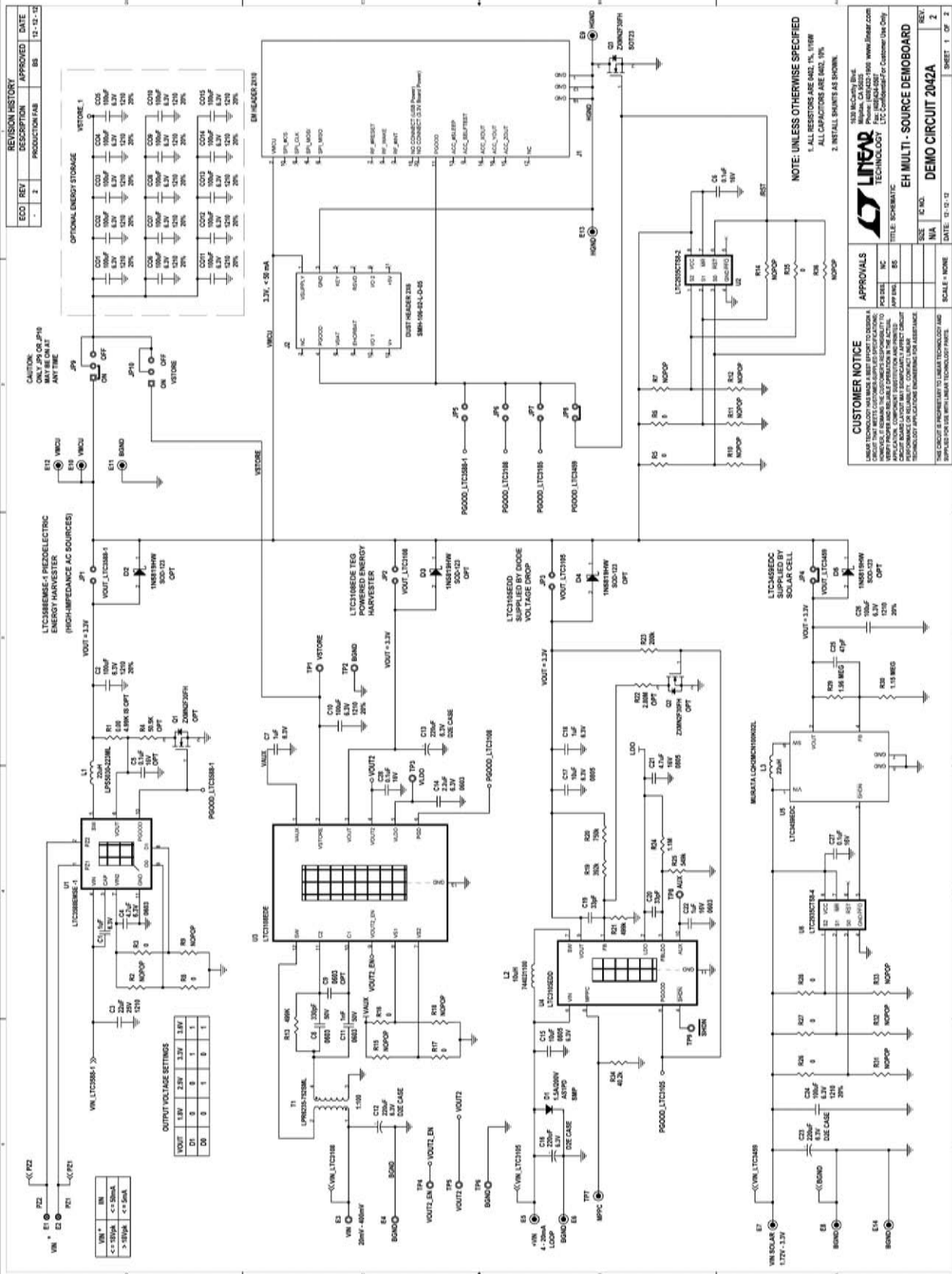
1	0	C5 (OPT)	CAP, CHIP, X7R, 0.1µF, 10%, 16V, 0402	MURATA, GRM155R71C104KA88D
2	0	C9 (OPT)	OPT, 0603	
3	0	D2-D5 (OPT)	DIODE, SCHOTTKY, 40V, 1A, SOD-123	DIODES INC, 1N5819HW-7-F
4	0	Q1, Q2 (OPT)	N-CHANNEL MOSFET, 20V, SOT23	DIODES/ZETEX, ZXMN2F30FHTA
5	0	R1 (OPT)	RES, CHIP, 4.99k, ±1%, 1/16W, 0402, ±100ppm/°C	VISHAY, CRCW04024K99FKED
6	0	R2, R7, R9, R10, R11, R12, R14, R15, R18, R31, R32, R33, R36	RES., CHIP, 0402	NOPOP
7	0	R4 (OPT)	RES, CHIP, 50.5k, ±1%, 1/16W, 0402, ±100ppm/°C	VISHAY, CRCW040250K5FKED
8	0	R22 (OPT)	RES, CHIP, 2.80M, ±1%, 1/16W, 0402, ±100ppm/°C	VISHAY, CRCW04022M80FKED

Hardware For Demo Board Only

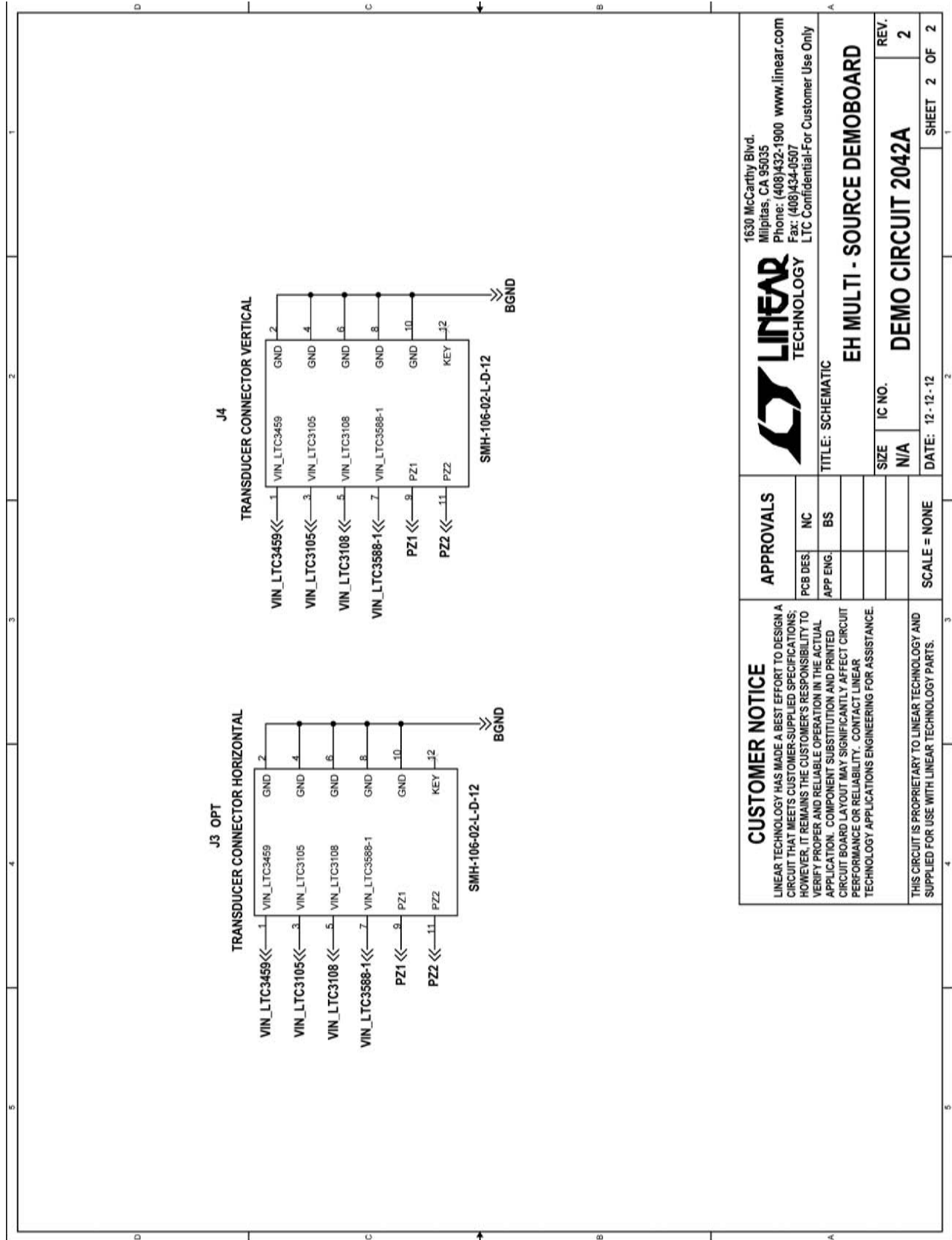
1	14	E1-E14	TURRET, 0.061 DIA	MILL-MAX, 2308-2
2	8	JP1-JP8	HEADER, 2 PINS, 2mm	SAMTEC, TMM-102-02-L-S
3	2	JP9, JP10	HEADER, 3 PINS, 2mm	SAMTEC, TMM-103-02-L-S
4	3	JP4, JP8, JP9	SHUNT 2MM	SAMTEC, 2SN-BK-G
5	0	JP1, JP2, JP3, JP5, JP6, JP7, JP10	SHUNT 2MM, (DO NOT INSTALL)	SAMTEC, 2SN-BK-G
6	1	J1	HEADER, 2 x 10, 20-PIN, SMT HORIZONTAL SOCKET, 0.100"	SAMTEC, SMH-110-02-L-D
7	1	J2	HEADER, 2 x 6, 12-PIN, SMT HORIZONTAL SOCKET w/KEY, 0.100"	SAMTEC, SMH-106-02-L-D-05
7	1	J3 (OPT), J4	HEADER, 2 x 6, 12-PIN, SMT HORIZONTAL SOCKET w/KEY, 0.100"	SAMTEC, SMH-106-02-L-D-12
8	4	STANDOFF	STANDOFF, HEX 0.625" L, 4-40, THR NYLON	KEYSTONE, 1902F
9	4	SCREW	SCREW, MACH, PHIL, 4-40, 0.250 IN, NYLON	B&F FASTENER SUPPLY, NY PMS 440 0025 PH

DEMO MANUAL DC2042A

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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APPROVALS		TITLE: SCHEMATIC	
PCB DES.	NC	SIZE	IC NO.
APP ENG.	BS	N/A	REV. 2
CUSTOMER NOTICE LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.		EH MULTI - SOURCE DEMOBOARD	
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		DEMO CIRCUIT 2042A	
SCALE = NONE		DATE: 12-12-12	
		SHEET 2 OF 2	

dc2042af

DEMO MANUAL DC2042A

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