BGT24MR2

Silicon Germanium 24 GHz Twin IQ Receiver MMIC

Data Sheet

Revision 3.1, 2014-03-25

RF & Protection Devices

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BGT24MR2 Silicon Germanium 24 GHz Twin IQ Receiver MMIC

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Previous Revision: 2013-07-08, Revision 3.1

Page	Subjects (major changes since last revision)
7	update feature list

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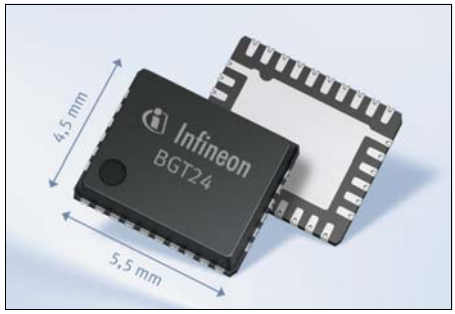
1 Features



- Gilbert based dual homodyne quadrature receiver
- Single ended RF terminals
- Low noise figure: NF_{SSB}: 12 dB
- High conversion gain: 26 dB
- High 1 dB input compression point: -12 dBm
- Low LO input power
- Single supply voltage of 3.3 V
- Integrated temperature sensor for monitoring purposes
- Power consumption 300 mW in continuous operating mode
- 200 GHz bipolar SiGe:C technology b7hf200
- Fully ESD protected device
- VQFN-32-9 leadless plastic package incl. LTI-feature
- Pb-free (RoHS compliant) package

RoHS

Description

The BGT24MR2 is a Silicon Germanium MMIC (dual channel receiver) accommodating two separate homodyne quadrature downconversion chains, operating from 24.0 to 24.25 GHz. It complements Infineons Transceiver MMICs BGT24MTR11 and BGT24MTR12. LO buffer amplifiers are included to relax LO drive requirements and individual LNAs provide low noise figures. RC polyphase filters (PPF) are used for LO quadrature phase generation. The circuit is manufactured in a 0.18µm SiGe:C technology offering a cutoff frequency of 200 GHz. The MMIC is packaged in a 32 pin leadless RoHs compliant VQFN package.

Product Name	Package	Chip	Marking
BGT24MR2	VQFN32-9	T1525	BGT24MR2

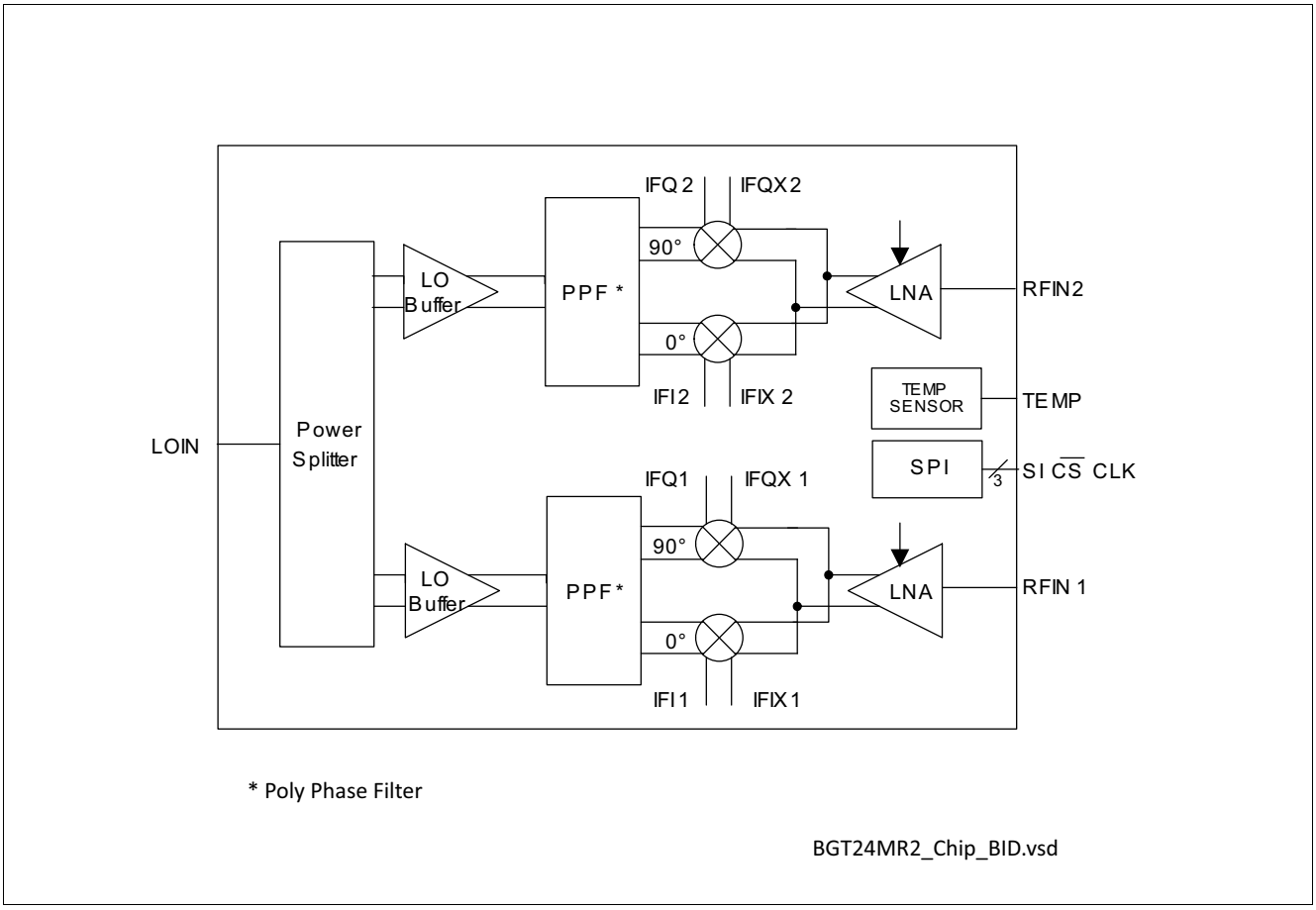


Figure 1 BGT24MR2 Block Diagram

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

T_A = -40 °C to 105 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	-0.3	–	3.6	V	–
DC voltage at Pins RFIN1, RFIN2, LOIN	VDC_{RF}	0	–	0	V	MMIC provides short circuit to GND for all RF Pins
DC voltage at Pins IFI1/2, IFIX1/2, IFQ1/2, IFQX1/2	VDC_{IF}	0	–	Vcc	V	–
DC current into Pins IFI1/2, IFIX1/2, IFQ1/2, IFQX1/2	I_{IF}	-8.5	–	3.5	mA	max. values indicate current due to short circuit to GND and Vcc respectively
DC voltage at Pin TEMP	VDC_{TEMP}	-0.3	–	3.6	V	–
DC current into Pin TEMP	I_{TEMP}	-1	–	1.5	mA	max. values indicate current due to short circuit to GND and Vcc respectively
DC voltage at SPI input Pins SI, CLK, $\overline{CS}$	VDC_{SPIIN}	-0.3	–	3.6	V	–
DC current into SPI input Pins SI, CLK, $\overline{CS}$	I_{SPIIN}	–	–	3	mA	–
RF input power into Pins RFIN1, RFIN2	P_{RF}	–	–	0	dBm	–
LO input power into Pin LOIN	P_{LO}	–	–	10	dBm	–
Total power dissipation	P_{DISS}	–	–	500	mW	With BIST deactivated
Junction temperature	T_J	-40	–	150	°C	–
Ambient temperature range	T_A	-40	–	105	°C	T_A = Package soldering point
Storage temperature range	T_{STG}	-40	–	150	°C	–

Attention: Stresses exceeding the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

1) Not subject to production test, specified by design

2.2 Thermal Resistance

Table 2 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction - soldering point[1)]	R_{thJS}	–	–	40	K/W	–

1) For calculation of R_{thJA} please refer to application note thermal resistance

2.3 ESD Integrity

Table 3 ESD Integrity

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD robustness, HBM[1)]	$V_{ESD-HBM}$	-1	–	1	kV	All pins
ESD robustness, CDM[2)]	$V_{ESD-CDM}$	-500	–	500	V	All pins

1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kΩ, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

2) According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

2.4 Measured RF Characteristics

2.4.1 Power Supply

Table 4 Typical Characteristics T_A = -40 .. 105 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	3.135	3.3	3.465	V	–
Supply current	I_{CC}	70	90	120	mA	–

2.4.2 RX Section

Table 5 Typical Characteristics T_A = -40 .. 105 °C, f = 24.0 .. 24.25 GHz[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RFIN and LOIN frequency range	f_{RFIN}, f_{LOIN}	24.0	–	24.25	GHz	–
RFIN and LOIN port impedance[2)]	Z_{RFIN1} Z_{RFIN2} Z_{LOIN}	–	14.0-j4.8 14.9-j6.3 27.3+j9.9	–	Ω	Typical value at 24.125GHz and VSWR ≤ 2:1
RFIN and LOIN VSWR	$VSWR_{RFIN}$, $VSWR_{LOIN}$	–	–	2:1	–	At source port of off chip compensation network as proposed
IF frequeny range	f_{IF}	0	–	10	MHz	–
IF 1/f corner frequency	f_c	–	10	20	kHz	–
IF port impedance	Z_{IF}	850	1000	1150	Ω	–
Leakage LOIN to RFIN	$L_{LOIN-RFIN}$	–	–	-30	dBm	Parameter based on IFX eval board design
Isolation RFIN1 to RFIN2	$I_{RFIN1-RFIN2}$	30	–	–	dB	Parameter based on IFX eval board design
LOIN input power	P_{LOIN}	-7	–	3	dBm	–
Voltage conversion gain[3)]	G_C	19	26	31	dB	$R_{LOAD,IF}$ > 10kΩ
LNA gain reduction	ΔG_{CLG}	3	5	8	dB	–
SSB Noise figure	NF_{SSB}	–	12	20	dB	Single sideband at 100kHz
1dB input compression	IP_{-1dB}	-17	-12	–	dBm	–
3'rd order input intercept point	$IIP3$	-8	-4	–	dBm	–

Table 5 Typical Characteristics T_A = -40 .. 105 °C, f = 24.0 .. 24.25 GHz[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Quadrature phase imbalance	ε_P	-10	–	10	deg	–
Quadrat. amplitude imbalance	ε_A	-1	–	1	dB	–

1) Performance based on Application Circuit Figure 2 on Page 13, Cross Section of Application Board, Compensation Structures and Application Board Layout Figure 4 on Page 18ff and Footprint Figure 8 on Page 21

2) Guaranteed by device design

3) Lowest gain at high temperature, highest gain at low temperature

2.5 Temperature Sensor

Monitoring of the chip temperature is provided by the on-chip temperature sensor which delivers temperature-proportional voltage to the TEMP output.

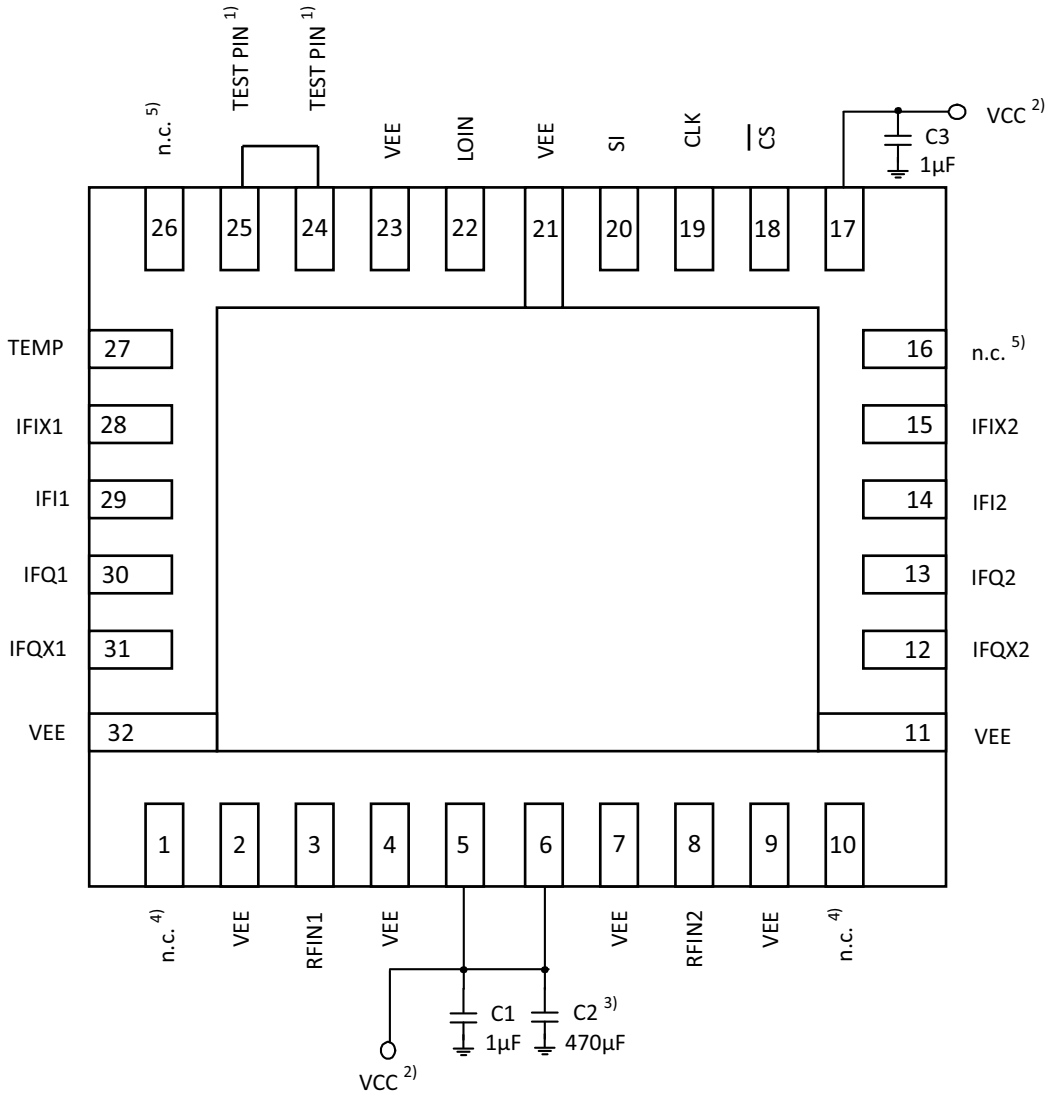
Table 6 Typical Characteristics Temperature Sensor T_A = -40 .. 105 °C[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature range	T_{TSENS}	-40	–	105	°C	–
Output temperature voltage	$V_{OUT,TEMP}$	–	1.50	–	V	@ 25°C
Sensitivity	S_{TSENS}	–	4.5	–	mV/K	–
Overall accuracy error	Err_{TSENS}	–	–	±15	K	–

1) all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

3 Application Circuit and Block Diagram

3.1 Application Circuit Schematic



1) Connect test pin 24 and 25
2) Galvanic connection of VCC pins on silicon (pin 5, 6 and 17)
3) Optional value: according to quality of supply voltage (C2)
4) Recommendation: Connect pin 1 and 10 to VEE for better RF performance
5) Floating pin 16 and 26 - do not connect with any other pin

BGT24MR2_Appl_BID.vsd

Figure 2 Application Circuit with Chip Outline (Top View)

Table 7 Bill of Materials

Part Number	Part Type	Manufacturer	Size	Comment
C1 ... C3	Chip capacitor	Various	Various	–

3.2 Pin Description

Table 8 Pin Definition and Function

Pin No.	Name	Function
1	n.c.	Not connected
2	VEE	Ground
3	RFIN1	RF input downconverter 1
4	VEE	Ground
5	VCC	Supply voltage
6	VCC	Supply voltage
7	VEE	Ground
8	RFIN2	RF input downconverter 2
9	VEE	Ground
10	n.c.	Not connected
11	VEE	Ground
12	IFQX2	Complementary quadrature phase IF output downconverter 2
13	IFQ2	Quadrature phase IF output downconverter 2
14	IFI2	In phase IF output downconverter 2
15	IFIX2	Complementary in phase IF output downconverter 2
16	n.c.	Do not connect; DC coupled pin
17	VCC	Supply voltage
18	$\overline{CS}$	Chip select input SPI (inverted)
19	CLK	Clock input SPI
20	SI	Data input SPI
21	VEE	Ground
22	LOIN	LO input
23	VEE	Ground
24	TEST PIN	Test pin; DC coupled pin
25	TEST PIN	Test pin; DC coupled pin
26	n.c.	Do not connect; DC coupled pin
27	TEMP	Temperature sensor output
28	IFIX1	Complementary in phase IF output downconverter 1
29	IFI1	In phase IF output downconverter 1
30	IFQ1	Quadrature phase IF output downconverter 1
31	IFQX1	Complementary quadratrue phase IF output downconverter 1
32	VEE	Ground

3.3 SPI

1.) Three signals control the serial peripheral interface of the BGT24MR2:

SI (Data); CLK (Clock); $\overline{CS}$ (Chip select)

2.) The data bits SI (MSB first) are read in the shift register with falling edge of the CLK signal.

Please make sure, that the data is present at least 10 ns before and at least 10 ns after the falling edge of the clock signal.

3.) The CLK and $\overline{CS}$ signals are combined internally.

At least 20 ns before first rising edge of the first CLK signal $\overline{CS}$ needs to be in "low" state.

While the Data is read, $\overline{CS}$ has to remain in "low" state.

4.) When Data read in is finished, the shift register content will be written in the latch at the rising edge of the $\overline{CS}$ signal. The time between the last falling edge of the CLK signal and the rising edge of the $\overline{CS}$ must be at least 20 ns.

Table 9 SPI Data Bit Description

Data Bit	Name	Description (Logic High)	Power ON State
15 (MSB)	GS	LNA Gain reduction	low
14	–	Not used	low
13	Test Bit	Test bit, must be low otherwise malfunction	low
12	Test Bit	Test bit, must be low otherwise malfunction	low
11	Test Bit	Test bit, must be low otherwise malfunction	low
10	Test Bit	Test bit, must be high otherwise malfunction	high
9	Test Bit	Test bit, must be high otherwise malfunction	high
8	Test Bit	Test bit, must be high otherwise malfunction	high
7	Test Bit	Test bit, must be low otherwise malfunction	low
6	Test Bit	Test bit, must be low otherwise malfunction	low
5	Test Bit	Test bit, must be low otherwise malfunction	low
4	Test Bit	Test bit, must be high otherwise malfunction	high
3	Test Bit	Test bit, must be low otherwise malfunction	low
2	Test Bit	Test bit, must be high otherwise malfunction	high

Table 9 SPI Data Bit Description (cont'd)

Data Bit	Name	Description (Logic High)	Power ON State
1	Test Bit	Test bit, must be low otherwise malfunction	low
0	Test Bit	Test bit, must be low otherwise malfunction	low

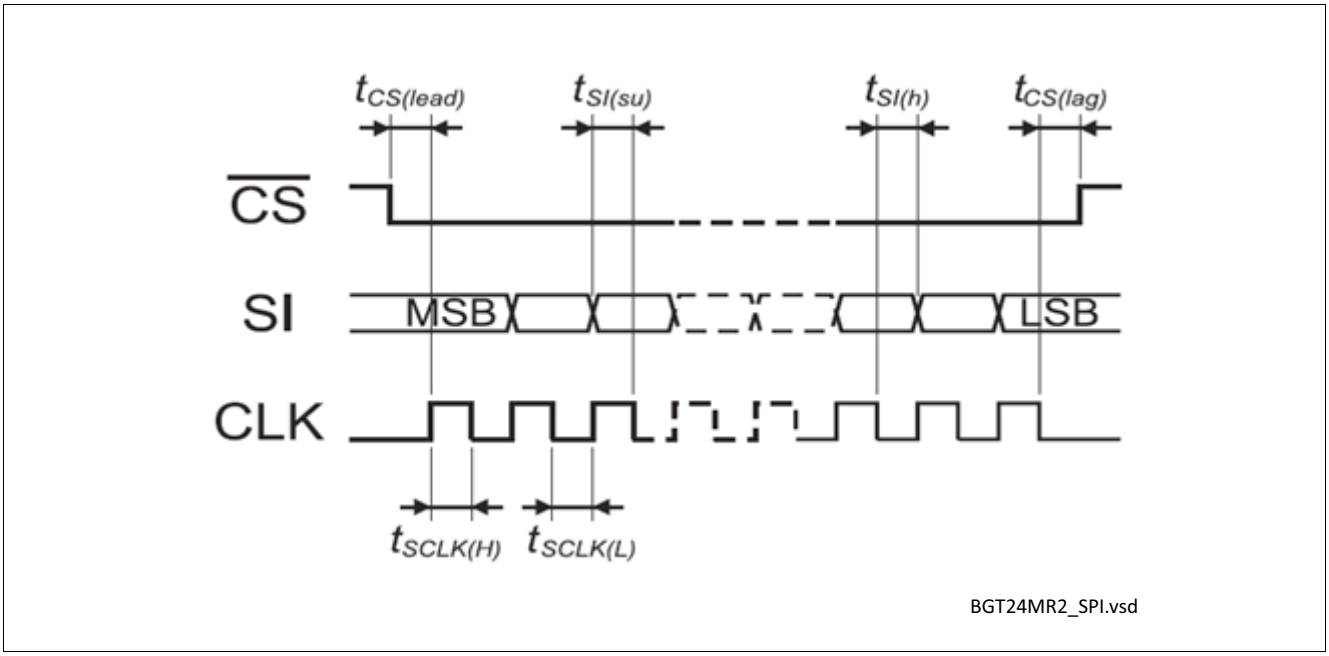


Figure 3 Timing Diagram of the SPI

Table 10 SPI Timing and Logic Levels

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Serial clock frequency	f_{SCLK}	0	–	50	MHz
Serial clock high time	$f_{SCLK(H)}$	10	–	–	ns
Serial clock low time	$t_{SCLK(L)}$	10	–	–	ns
Chip select lead time	$t_{CS(lead)}$	20	–	–	ns
Chip select lag time	$t_{CS(lag)}$	20	–	–	ns
Data setup time	$t_{SI(su)}$	10	–	–	ns
Data hold time	$t_{SI(h)}$	10	–	–	ns
Low level (SI, CLK, $\overline{CS}$)	$V_{IN(L)}$	0	–	0.8	V
High level (SI, CLK, $\overline{CS}$)	$V_{IN(H)}$	2.0	–	V_{CC}	V
Input capacitance (SI, CLK, $\overline{CS}$)	C_{IN}	–	–	2	pF
Input current (SI, CLK, $\overline{CS}$)	I_{IN}	-150	–	150	µA

3.4 Application Board

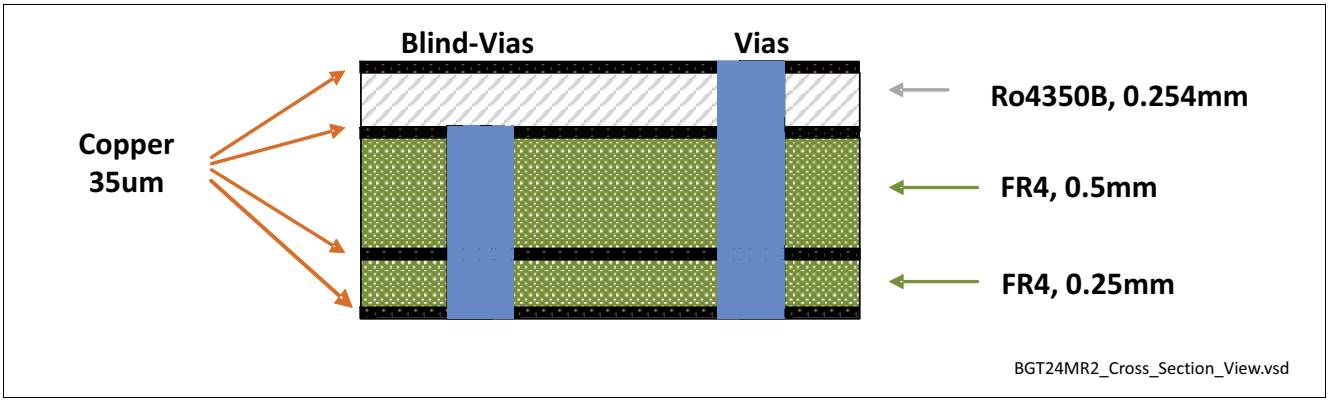


Figure 4 Cross-Section View of Application Board

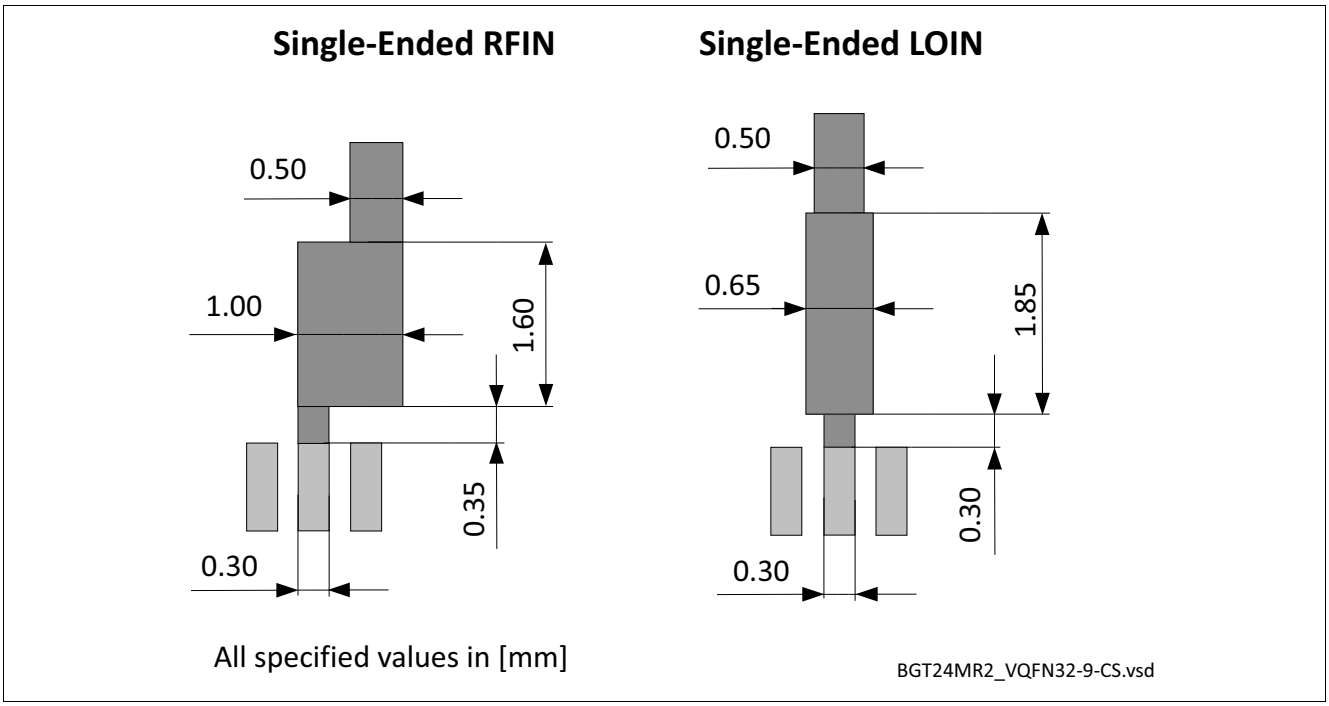


Figure 5 Detail of Compensation Structure (valid for appl. board mat. Ro4350B, 0.254mm acc. to Fig. 4)

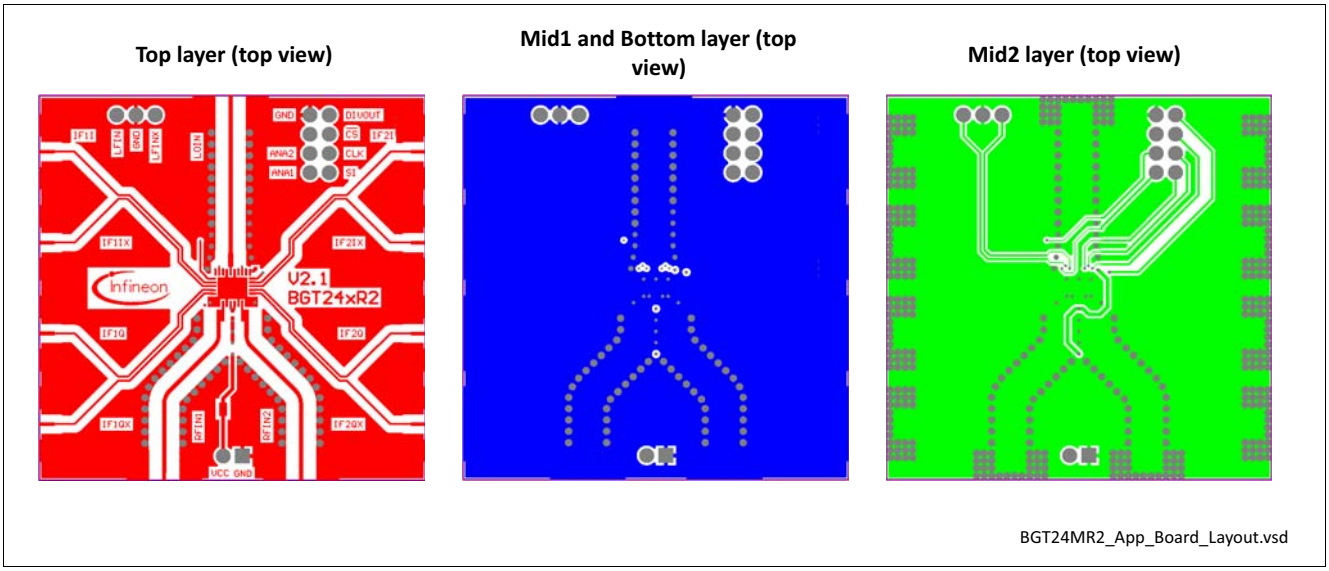


Figure 6 Application Board Layout

Note: In order to achieve the same performance as given in this datasheet please follow the suggested PCB-layout. The compensation structure is critical for RF performance. Via holes as recommended on one of next pages (not shown above).

3.5 Equivalent Circuit Diagram of MMIC Interfaces

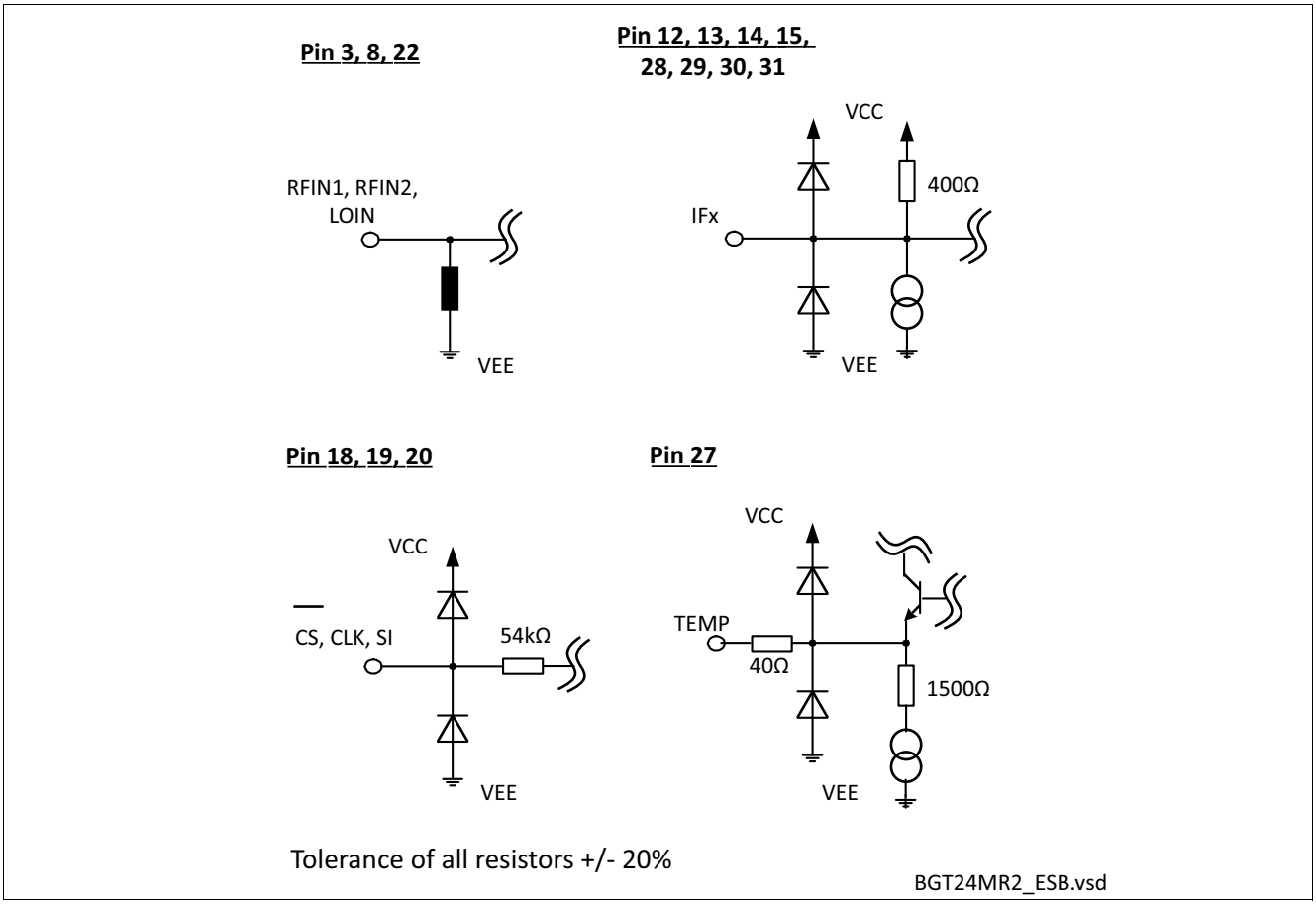


Figure 7 Equivalent Circuit Diagram of MMIC Interfaces

4 Physical Characteristics

4.1 Package Footprint

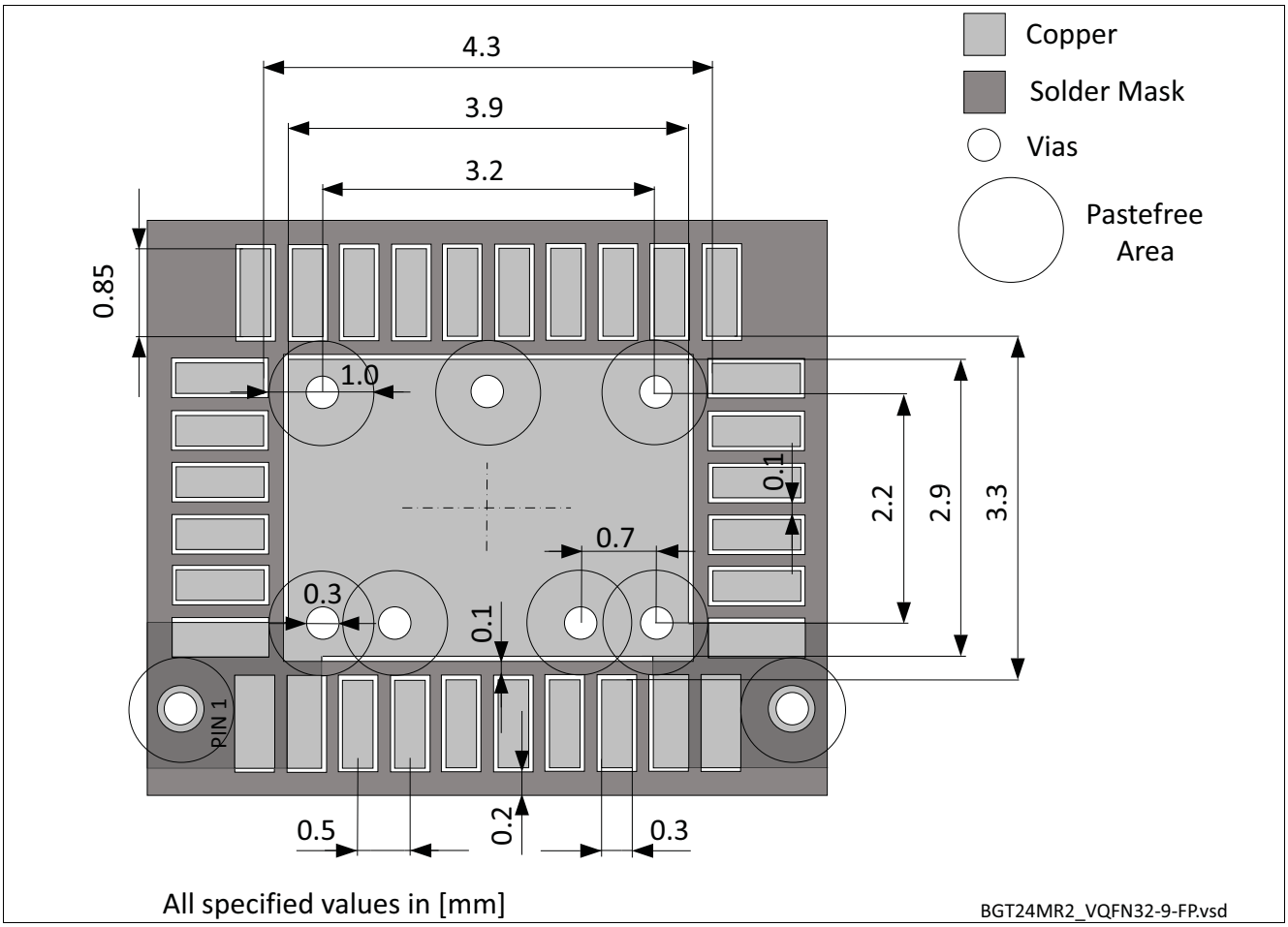


Figure 8 Recommended Footprint and Stencil Layout for the VQFN32-9 Package

4.2 Reflow Profile

Soldering process qualified during qualification with “Preconditioning MSL-3: 30°C. 60%r.h., 192h, according to JEDEC JSTD20”.

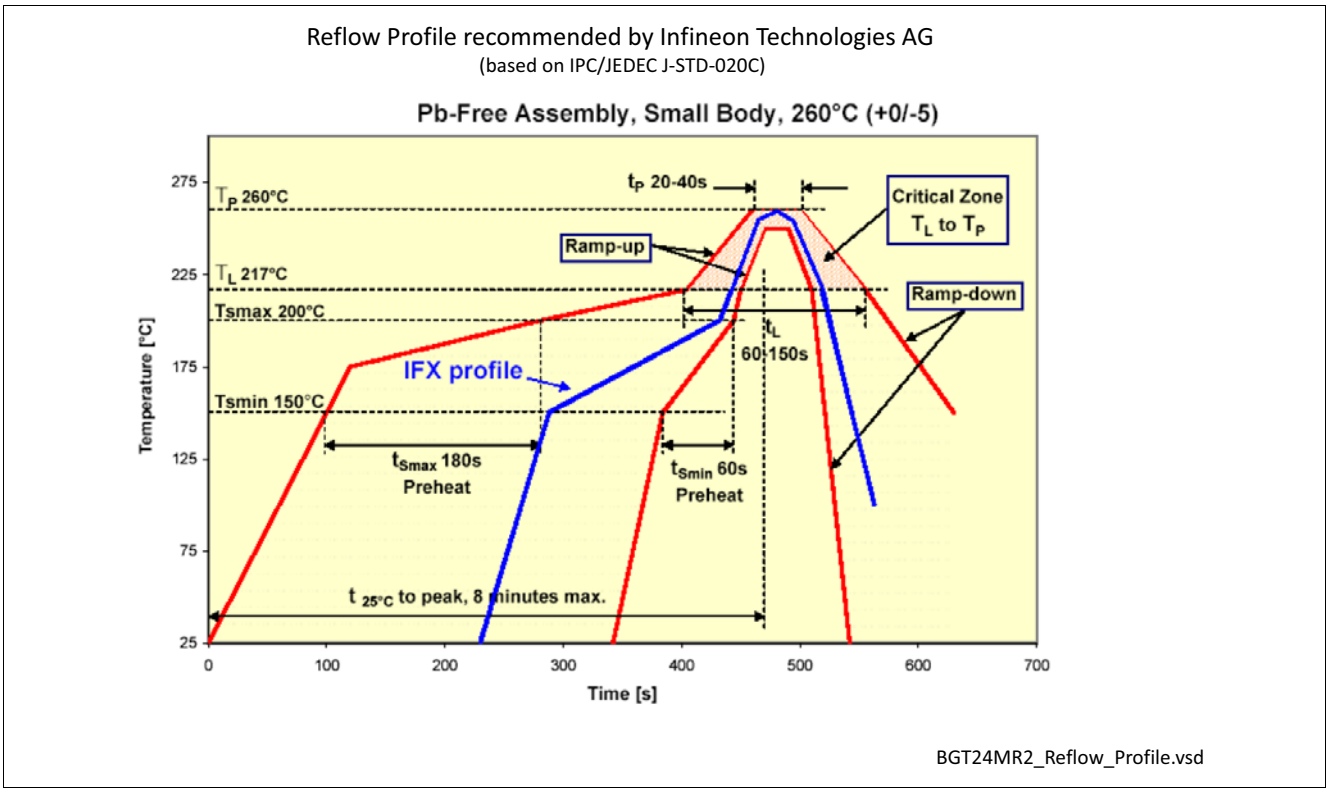


Figure 9 Reflow Profile for BGT24MR2 (VQFN32-9)

4.3 Package Dimensions

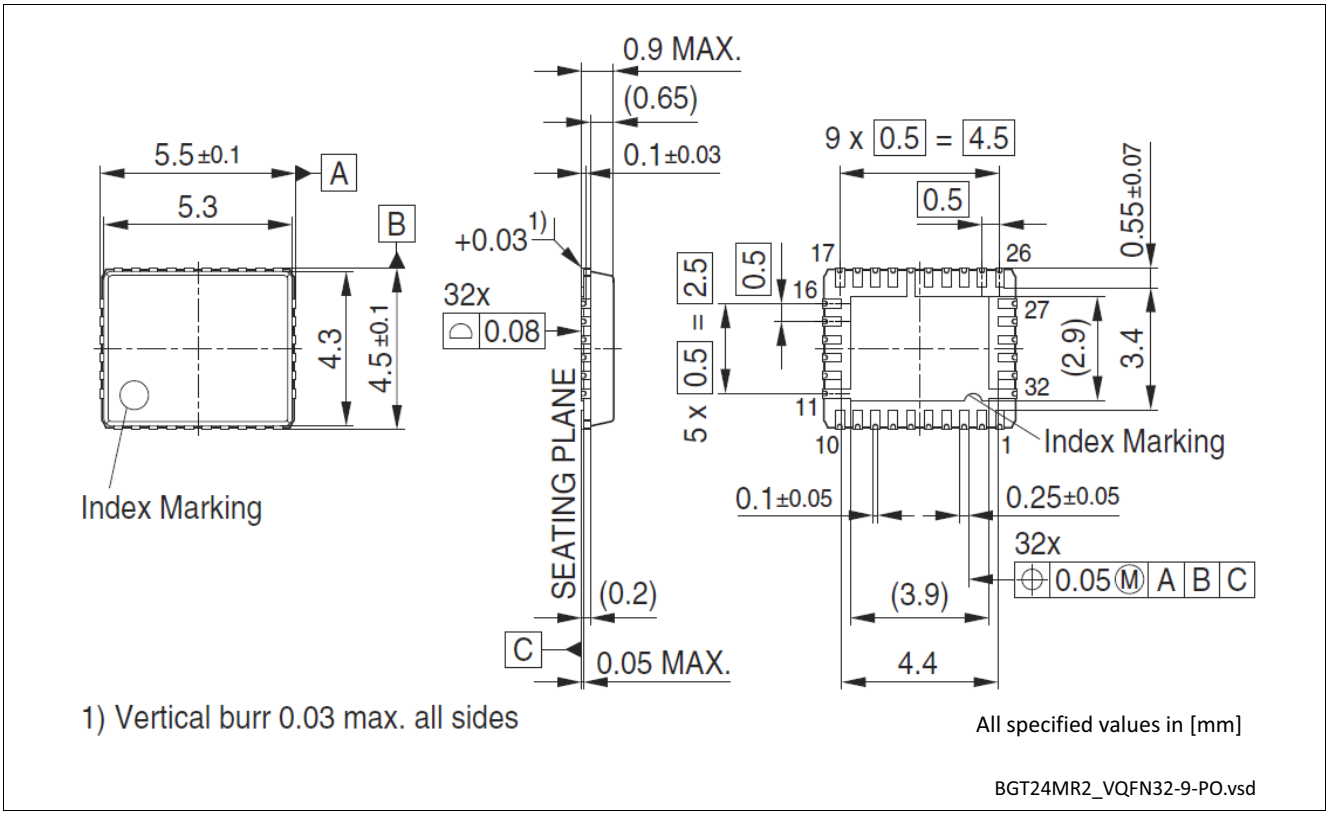


Figure 10 Package Outline (Top, Side and Bottom View)

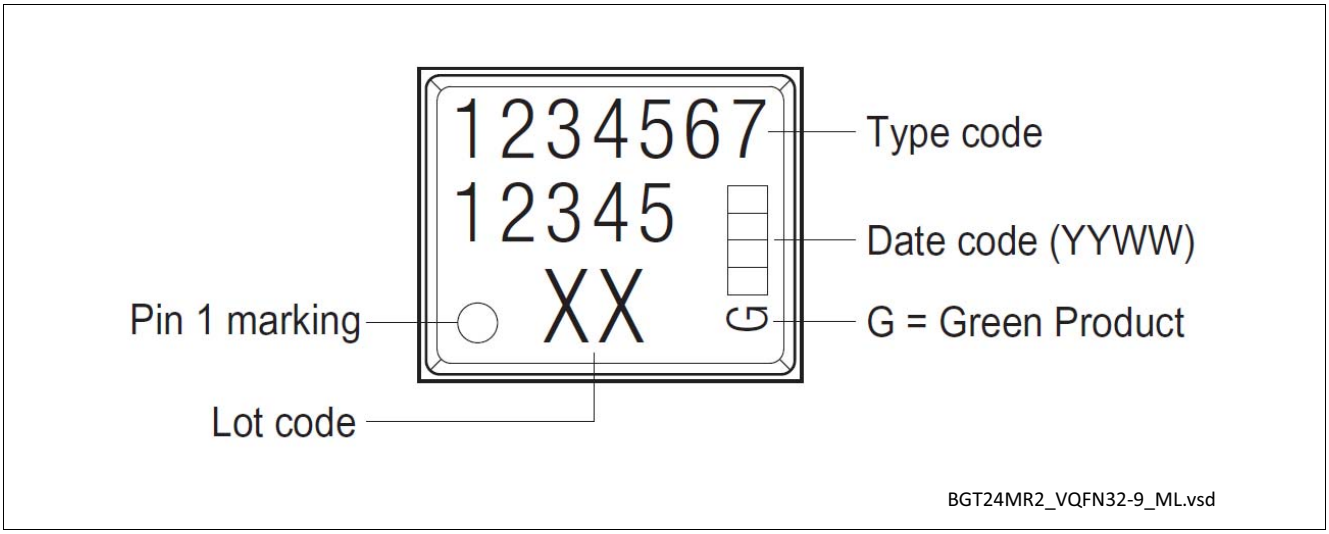


Figure 11 Marking Layout VQFN32-9

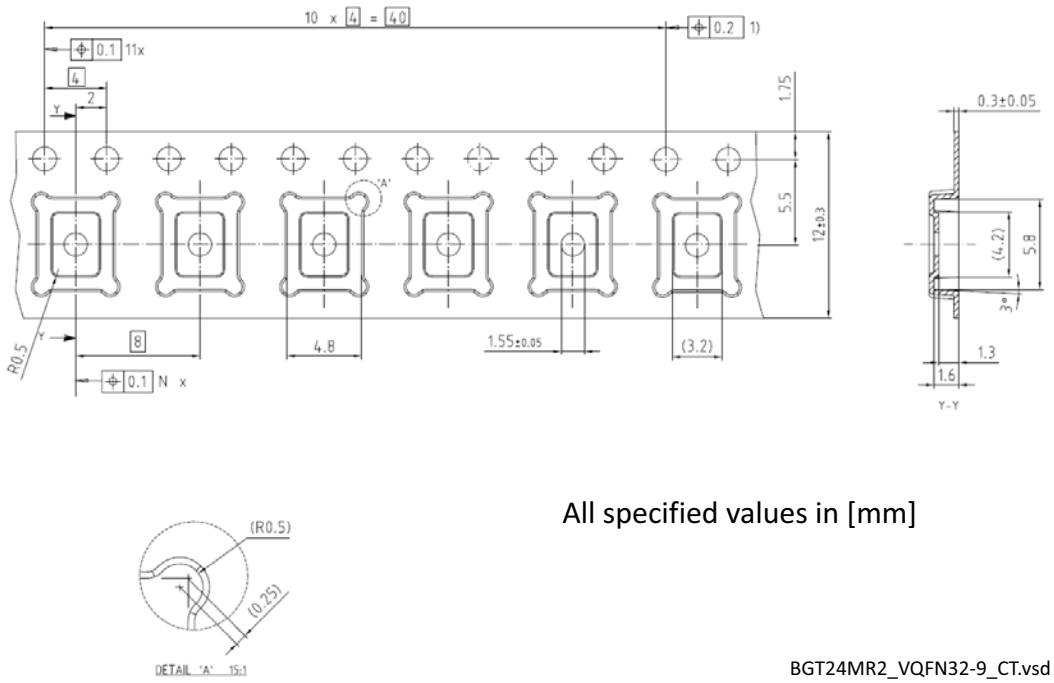


Figure 12 Tape of VQFN32-9

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