

MC74ACT564

Octal D-Type Flip-Flop with 3-State Outputs

The MC74ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}).

The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The MC74ACT564 device is functionally identical to the MC74ACT574, but with inverted outputs.

Features

- Inputs and Outputs on the Opposite Sides of the Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessor
- Functionally Identical to the MC74ACT574 but with Inverted Outputs
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- TTL Compatible Inputs
- These are Pb-Free Devices

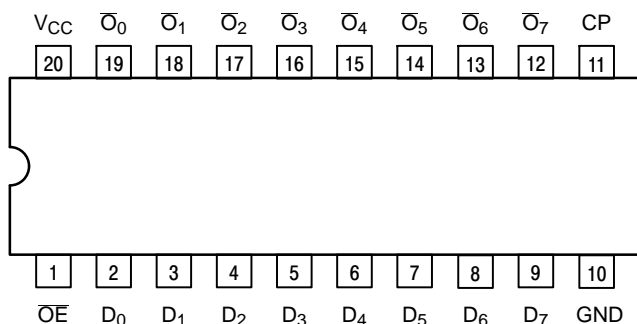


Figure 1. Pinout: 20-Lead Packages Conductors
(Top View)

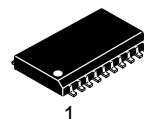
PIN ASSIGNMENT

| PIN | FUNCTION |
|-------------------------------------|-----------------------------|
| D ₀ -D ₇ | Data Inputs |
| CP | Clock Pulse Input |
| \overline{OE} | 3-State Output Enable Input |
| \overline{O}_0 - \overline{O}_7 | 3-State Outputs |



ON Semiconductor[®]

www.onsemi.com



SOIC-20W
DW SUFFIX
CASE 751D

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 5 of this data sheet.

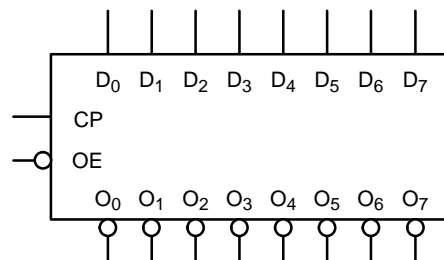
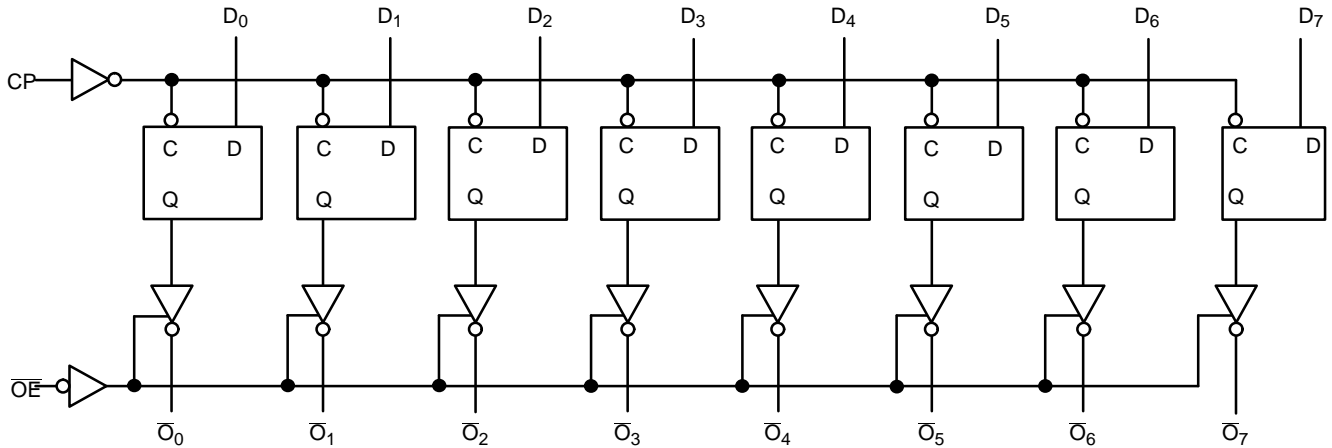


Figure 2. Logic Symbol

MC74ACT564



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

FUNCTION TABLE

| Inputs | | | Internal | Outputs | Function |
|-----------------|------------|---|----------|---------|-------------------|
| \overline{OE} | CP | D | Q | O | |
| H | H | L | NC | Z | Hold |
| H | H | H | NC | Z | Hold |
| H | \uparrow | L | H | Z | Load |
| H | \uparrow | H | L | Z | Load |
| L | \uparrow | L | H | H | Data Available |
| L | \uparrow | H | L | L | Data Available |
| L | H | L | NC | NC | No Change in Data |
| L | H | H | NC | NC | No Change in Data |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 \uparrow = LOW-to-HIGH Transition
 NC = No Change

FUNCTIONAL DESCRIPTION

The MC74ACT564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that

meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

MC74ACT564

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|---|--|-----------------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage (Referenced to GND) (Note 1) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | ± 20 | mA |
| I_{OK} | DC Output Diode Current | ± 50 | mA |
| I_{OUT} | DC Output Sink/Source Current | ± 50 | mA |
| I_{CC} | DC Supply Current, per Output Pin | ± 50 | mA |
| I_{GND} | DC Ground Current, per Output Pin | ± 100 | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | $^{\circ}\text{C}$ |
| T_L | Lead temperature, 1 mm from Case for 10 Seconds | 260 | $^{\circ}\text{C}$ |
| T_J | Junction Temperature Under Bias | 140 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Note 2) | 65.8 | $^{\circ}\text{C}/\text{W}$ |
| MSL | Moisture Sensitivity | Level 1 | |
| F_R | Flammability Rating | Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in | |
| V_{ESD} | ESD Withstand Voltage | Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5) | V |
| $I_{Latchup}$ | Latchup Performance | Above V_{CC} and Below GND at 85 $^{\circ}\text{C}$ (Note 6) | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{OUT} absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|--|-----|-----|----------|--------------------|
| V_{CC} | DC Input Voltage (Referenced to GND) | 4.5 | | 5.5 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | -40 | 25 | +85 | $^{\circ}\text{C}$ |
| t_r, t_f | Input Rise and Fall Time (Note 8) | | | | ns/V |
| | | | | | |
| | | | | | |
| I_{OH} | Output Current – High | | | -24 | mA |
| I_{OL} | Output Current – Low | | | 24 | mA |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
8. V_{in} from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74ACT564

DC CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -40°C to +85°C | | Unit | Conditions |
|--------------------------------------|--|------------------------|------------------------|-------------------|------------------------------------|-------------------|----------|---|
| | | | Typ | Guaranteed Limits | Typ | Guaranteed Limits | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | 2.0 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | 2.0 | | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | 0.8 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | 0.8 | | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | V | I _{OUT} = -50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | | 3.86 | 3.76 | 3.76 | V | *V _{IN} = V _{IL} or V _{IH} I _{OH} -24 mA |
| | | 5.5 | | 4.86 | 4.76 | 4.76 | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | 0.1 | V | I _{OUT} = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | | 0.36 | 0.44 | 0.44 | V | *V _{IN} = V _{IL} or V _{IH} I _{OL} 24 mA |
| | | 5.5 | | 0.36 | 0.44 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | | μA | V _I = V _{CC} , GND |
| ΔI _{CCT} | Additional Max. I _{CC} /Input | 5.5 | 0.6 | | | 1.5 | mA | V _I = V _{CC} - 2.1 V |
| I _{OZ} | Maximum 3-State Current | 5.5 | | ±0.5 | ±5.0 | | μA | V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND |
| I _{OLD} I _{OHD} | †Minimum Dynamic Output Current | 5.5 5.5 | | | | 75 -75 | mA mA | V _{OLD} = 1.65 V Max V _{OHD} = 3.85 V Min |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80 | | μA | V _{IN} = V _{CC} or GND |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS t_r = t_f = 3.0 ns (For Figures and Waveforms, See Figures 4, 5, and 6.)

| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Unit |
|------------------|--|--------------------------|--|-----|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency | 5.0 | 85 | - | - | 75 | - | MHz |
| t _{PLH} | Propagation Delay CP to Q _n | 5.0 | 2.0 | - | 10.5 | 1.5 | 11.5 | ns |
| t _{PHL} | Propagation Delay CP to Q _n | 5.0 | 1.5 | - | 9.5 | 1.5 | 10.5 | ns |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | - | 9.0 | 1.5 | 9.5 | ns |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | - | 8.5 | 1.0 | 9.5 | ns |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | - | 10.5 | 1.5 | 11.5 | ns |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | - | 8.0 | 1.0 | 8.5 | ns |

*Voltage Range 5.0 V is 5.0 V ±0.5 V

MC74ACT564

AC OPERATING REQUIREMENTS

| Symbol | Parameter | V_{CC}^* (V) | $T_A = +25^\circ\text{C}$ $C_L = 50\text{ pF}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$ | | Unit |
|--------|-------------------------|-------------------|---|--------------------|---|-----|------|
| | | | Typ | Guaranteed Minimum | | | |
| t_s | Setup Time, HIGH or LOW | D_n to C_P | 5.0 | – | 2.5 | 3.0 | ns |
| t_h | Hold Time, HIGH or LOW | D_n to C_P | 5.0 | – | 1.0 | 1.0 | ns |
| t_w | C_P Pulse Width | HIGH or LOW | 5.0 | – | 3.0 | 3.5 | ns |

*Voltage Range 3.3 V is 3.3 V \pm 0.3 V.

*Voltage Range 5.0 V is 5.0 V \pm 0.5 V.

CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|----------|-------------------------------|-----------|------|-------------------------|
| C_{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0\text{ V}$ |
| C_{PD} | Power Dissipation Capacitance | 50 | pF | $V_{CC} = 5.0\text{ V}$ |

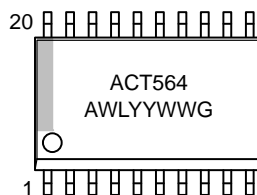
ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-----------------|----------------------|-----------------------|
| MC74ACT564DWR2G | SOIC–20 (Pb–Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

SOIC–20W



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb–Free Package

MC74ACT564

SWITCHING WAVEFORMS

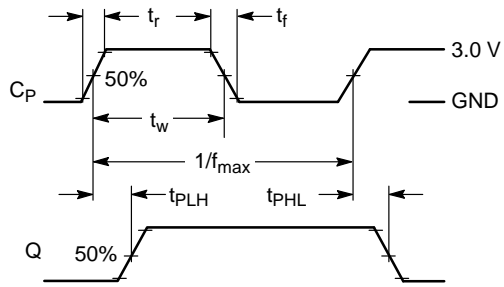


Figure 4.

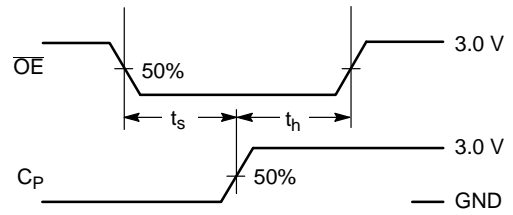


Figure 5.

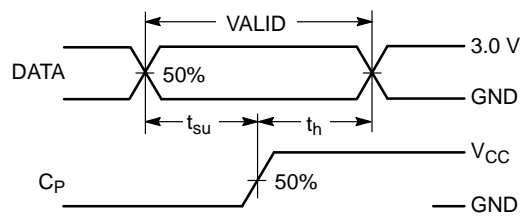
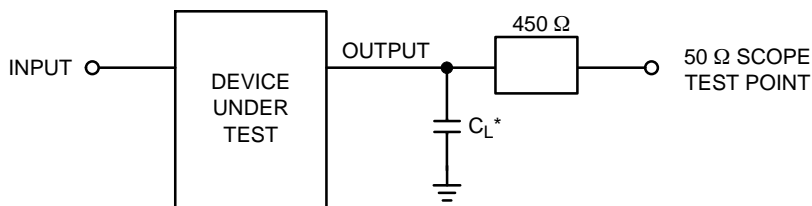


Figure 6.



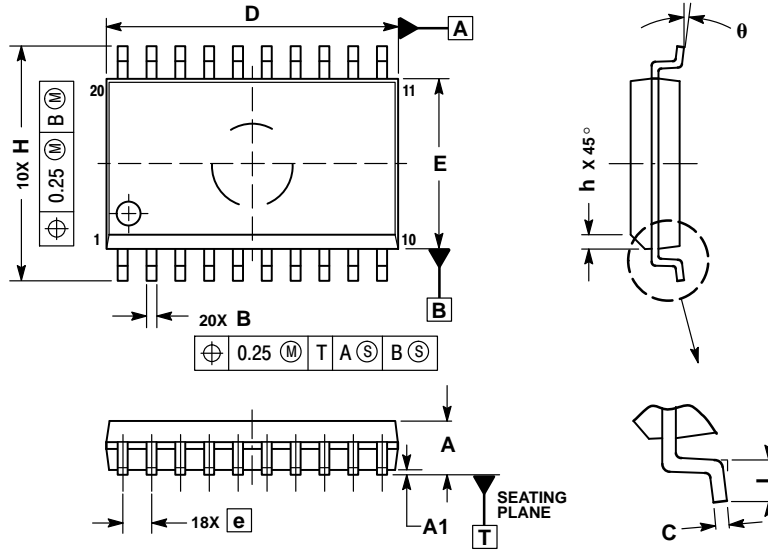
*Includes all probe and jig capacitance

Figure 7. Test Circuit

MC74ACT564

PACKAGE DIMENSIONS

SOIC-20W
DW SUFFIX
CASE 751D-05
ISSUE G



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[MC74ACT564DWR2G](#)