TEXAS INSTRUMENTS

LM2750, LM2750-ADJ

SNVS180N – APRIL 2002 – REVISED APRIL 2016

LM2750 Low-Noise Switched-Capacitor Boost Regulator

1 Features

- Wide Input Voltage Range: 2.7 V to 5.6 V
- Inductorless Solution: Application Requires Only Three Small Ceramic Capacitors
- Fixed 5-V Output and Adjustable Output Voltage Options Available
- 85% Peak Efficiency
  - 70% Average Efficiency Over Li-Ion Input Range (2.9 V to 4.2 V)
- Output Current up to 120 mA With 2.9 V ≤ V_{IN} ≤ 5.6 V
  - Output Current up to 40 mA With 2.7 V ≤ V_{IN} ≤ 2.9 V
- Fixed 1.7-MHz Switching Frequency for a Low-Noise, Low-Ripple Output Signal
- Pre-Regulation Minimizes Input Current Ripple, Keeping the Battery Line (V_{IN}) Virtually Noise-Free
- Shutdown Supply Current Less Than 2 µA
- Tiny WSON Package With Outstanding Power Dissipation: Usually No Derating Required

2 Applications

- White and Colored LED-Based Display Lighting
- Cellular Phone SIM Cards
- Audio Amplifier Power Supplies
- General Purpose Li-Ion-to-5-V Conversion
- EPOS Barcode Scanners
- Industrial Handheld Radios

3 Description

The LM2750 is a regulated switched-capacitor doubler that produces a low-noise output voltage. The 5-V output voltage option (LM2750-5.0) can supply up to 120 mA of output current over a 2.9-V to 5.6-V input range, as well as up to 40 mA of output current when the input voltage is as low as 2.7 V. An adjustable output voltage option with similar output current capabilities is also available (LM2750-ADJ). The LM2750 has been placed in TI's 10-pin WSON, a package with excellent thermal properties that keeps the part from overheating under almost all rated operating conditions.

A perfect fit for space-constrained, battery-powered applications, the LM2750 requires only three external components: one input capacitor, one output capacitor, and one flying capacitor. Small, inexpensive ceramic capacitors are recommended for use. In conjunction with the 1.7-MHz fixed switching frequency of the LM2750, these capacitors yield low output-voltage ripple, which is beneficial for systems requiring a low-noise supply. Pre-regulation minimizes input current ripple, thus reducing input noise to negligible levels.

A tightly controlled soft-start feature limits inrush currents during part activation. Shutdown completely disconnects the load from the input. Output current limiting and thermal shutdown circuitry protect both the LM2750 and other connected devices in the event of output shorts or excessive current loads.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2750 LM2750-ADJ	WSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

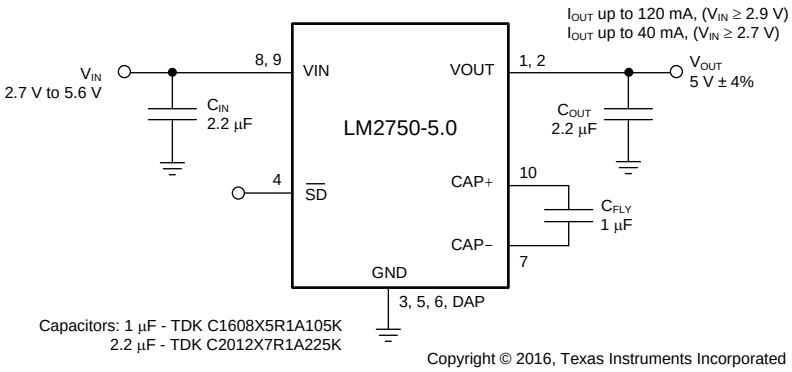


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (June 2015) to Revision N — **Page**

- Added 2 additional *"Applications"* ... 1
- Added additional *Thermal Information*; changed $R_{\theta JA}$ for DSC from 58.7°C/W to 45.6°C/W and for NGY from 32.7°C/W to 62.4°C/W ... 5

Changes from Revision L (May 2013) to Revision M — **Page**

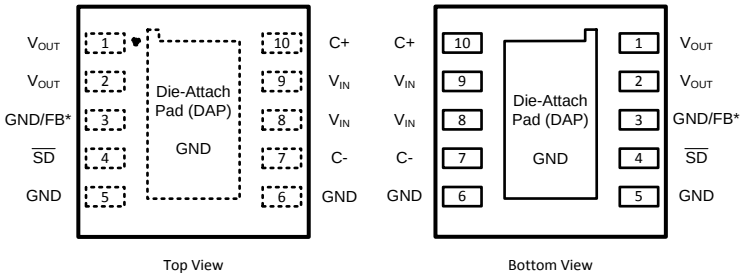
- Added *Device Information* and *Pin Configuration and Functions* sections, ESD Rating table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; added already-released LM2750-ADJ part number to title ... 1

Changes from Revision K (May 2013) to Revision L — **Page**

- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

NGY or DSC Package
10-Pin WSON



* LM2750-5.0: Pin 3 = GND; LM2750-ADJ: Pin 3 = FB

Pin Names and Numbers apply to both NGY0010A and DSC0010A packages.

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	LM2750-5.0	LM2750-ADJ		
CAP+	10	10	P	Flying capacitor positive terminal
CAP–	7	7	P	Flying capacitor negative terminal
FB	—	3	P	Feedback pin
GND	3	—	G	This pin must be connected externally to the ground pins (pins 5, 6, and the DAP).
GND	5, 6	5, 6	G	Ground - These pins must be connected externally.
$\overline{SD}$	4	4	I/O	Active-low shutdown input. A 200-kΩ resistor is connected internally between this pin and GND to pull the voltage on this pin to 0 V, and shut the part down, when the pin is left floating.
VIN	8, 9	8, 9	P	Input voltage - The pins must be connected externally.
VOUT	1, 2	1, 2	P	Output voltage - These pins must be connected externally.
DAP	√	√	GND	The DAP (Exposed Pad) functions as a thermal connection when soldered to a copper plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN pin: Voltage to GND	–0.3	6	V
$\overline{SD}$ pin: Voltage to GND	–0.3	(V_{IN} + 0.3)	V
Junction temperature, $T_{J\text{-}MAX\text{-}ABS}$		150	°C
Continuous power dissipation(3)	Internally limited		
Maximum output current(4)		175	mA
Maximum lead temperature (soldering, 5 seconds)		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) Thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 135°C (typical).
(4) Absolute maximum output current specified by design. Recommended input voltage range for output currents in excess of 120 mA: 3.1 V to 4.4 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
LM2750-5.0 input voltage		2.7	5.6	V
LM2750-ADJ input voltage	3.8 V ≤ V_{OUT} ≤ 4.9 V	2.7	(V_{OUT} + 0.7)	V
	4.9 V ≤ V_{OUT} ≤ 5.2 V	2.7	5.6	V
LM2750-ADJ output voltage		3.8	5.2	V
Recommended output current	2.9 V ≤ V_{IN} ≤ 5.6 V	0	120	mA
	2.7 V ≤ V_{IN} ≤ 2.9 V	0	40	mA
Junction temperature, T_J		–40	125	°C
Ambient temperature, T_A(3)		–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. For performance limits and associated test conditions, see *Electrical Characteristics*.
(2) All voltages are with respect to the potential at the GND pin.
(3) Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by this equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$. For more information on these topics, see *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401) and *Power Efficiency And Power Dissipation*.

6.4 Thermal Information

THERMAL METRIC[1]		LM2750-5.0, LM2750-ADJ		UNIT
		NGY (WSON)	DSC (WSON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.4	45.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.2	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	21.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.2	21.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.7	6.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical values apply for T_J = 25°C; minimum and maximum limits apply over the operating junction temperature range; 2.9 V ≤ V_{IN} ≤ 5.6 V, V_{OUT} = 5 V (LM2750-ADJ), $V_{(\overline{SD})}$ = V_{IN}, C_{FLY} = 1 µF, C_{IN} = 2 × 1 µF, C_{OUT} = 2 × 1 µF, unless otherwise specified [1][2][3].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage (LM2750-5.0)	2.9 V ≤ V_{IN} ≤ 5.6 V, I_{OUT} ≤ 120 mA	4.8 (–4%)	5	5.2 (4%)	V
		2.7 V ≤ V_{IN} ≤ 2.9 V, I_{OUT} ≤ 40 mA, T_J = 25°C	4.8 (–4%)	5	5.2 (4%)	
I_Q	Operating supply current	I_{OUT} = 0mA, T_J = 25°C $V_{IH(MIN)}$ ≤ $V_{(\overline{SD})}$ ≤ V_{IN}		5	10	mA
		I_{OUT} = 0 mA, $V_{IH(MIN)}$ ≤ $V_{(\overline{SD})}$ ≤ V_{IN}			12	
I_{SD}	Shutdown supply current	$V_{(\overline{SD})}$ = 0V			2	µA
V_{FB}	Feedback pin voltage (LM2750-ADJ)	V_{IN} = 3.1 V	1.17	1.232	1.294	V
I_{FB}	Feedback pin input current (LM2750-ADJ)	V_{FB} = 1.4 V		1		nA
V_R	Output ripple	C_{OUT} = 10 µF, I_{OUT} = 100 mA		4		mVp-p
		C_{OUT} = 2.2 µF, I_{OUT} = 100 mA		15		
E_{PEAK}	Peak efficiency (LM2750-5.0)	V_{IN} = 2.7 V, I_{OUT} = 40 mA		87%		
		V_{IN} = 2.9 V, I_{OUT} = 120 mA		85%		
E_{AVG}	Average Efficiency over Li-Ion Input Range (LM2750-5.0) [4]	V_{IN} = 2.9 V to 4.2 V, I_{OUT} = 120 mA		70%		
		V_{IN} = 2.9 V to 4.2 V, I_{OUT} = 40 mA		67%		
f_{SW}	Switching frequency		1	1.7		MHz
I_{LIM}	Current limit	V_{OUT} shorted to GND		300		mA

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers represent the most likely norm.
(3) C_{FLY}, C_{IN}, and C_{OUT} : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics
(4) Efficiency is measured versus V_{IN}, with V_{IN} being swept in small increments from 3 V to 4.2 V. The average is calculated from these measurements results. Weighting to account for battery voltage discharge characteristics (V_{BAT} vs. time) is not done in computing the average.

Electrical Characteristics (continued)

Typical values apply for T_J = 25°C; minimum and maximum limits apply over the operating junction temperature range; 2.9 V ≤ V_{IN} ≤ 5.6 V, V_{OUT} = 5 V (LM2750-ADJ), $V_{(\overline{SD})}$ = V_{IN}, C_{FLY} = 1 µF, C_{IN} = 2 × 1 µF, C_{OUT} = 2 × 1 µF, unless otherwise specified (1)(2)(3).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHUTDOWN PIN ($\overline{SD}$) CHARACTERISTICS						
V_{IH}	Logic-high $\overline{SD}$ input		1.3		V_{IN}	V
V_{IL}	Logic-low $\overline{SD}$ input		0		0.4	V
I_{IH}	$\overline{SD}$ input current (5)	1.3 V ≤ $V_{(\overline{SD})}$ ≤ V_{IN}		15	50	µA
I_{IL}	$\overline{SD}$ input current	$V_{(\overline{SD})}$ = 0 V	–1		1	µA
CAPACITOR CHARACTERISTICS						
C_{IN}	Required input capacitance (6)	I_{OUT} ≤ 60 mA	1			µF
		60 mA ≤ I_{OUT} ≤ 120 mA	2			
C_{OUT}	Required output capacitance (6)	I_{OUT} ≤ 60 mA	1			µF
		60 mA ≤ I_{OUT} ≤ 120 mA	2			

(5) $\overline{SD}$ Input Current (I_{IH}) is due to a 200-kΩ (typical) pulldown resistor connected internally between the $\overline{SD}$ pin and GND.
(6) Limit is the minimum required output capacitance to ensure proper operation. This electrical specification is specified by design.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	V_{OUT} turnon time	V_{IN} = 3 V, I_{OUT} = 100 mA (1)		0.5		ms

(1) Turnon time is measured from when $\overline{SD}$ signal is pulled high until the output voltage crosses 90% of its final value.

6.7 Typical Characteristics

Unless otherwise specified: V_{IN} = 3.6 V, T_A = 25°C, C_{IN} = 2.2 µF, C_{FLY} = 1 µF, C_{OUT} = 2.2 µF. Capacitors are low-ESR multi-layer ceramic capacitors (MLCCs).

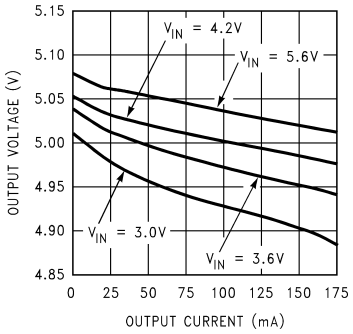


Figure 1. Output Voltage vs. Output Current

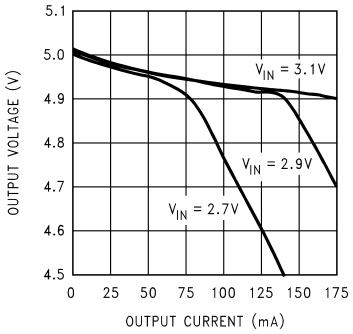


Figure 2. Output Voltage vs. Output Current

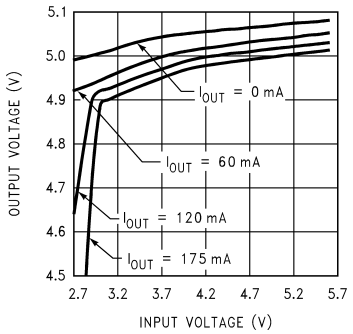


Figure 3. Output Voltage vs. Input Voltage

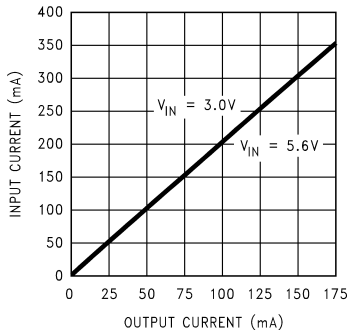


Figure 4. Input Current vs. Output Current

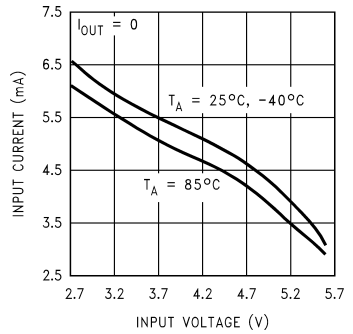


Figure 5. Quiescent Supply Current

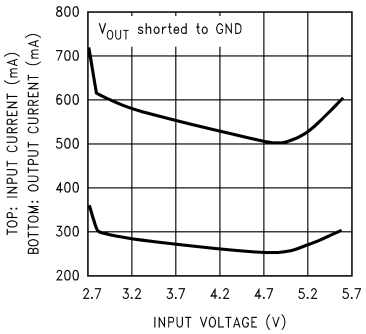


Figure 6. Current Limit Behavior

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.6 V, T_A = 25°C, C_{IN} = 2.2 µF, C_{FLY} = 1 µF, C_{OUT} = 2.2 µF. Capacitors are low-ESR multi-layer ceramic capacitors (MLCCs).

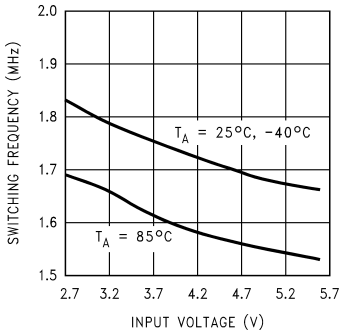


Figure 7. Switching Frequency

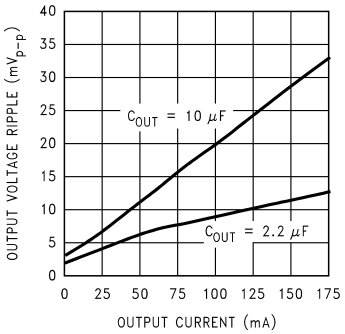
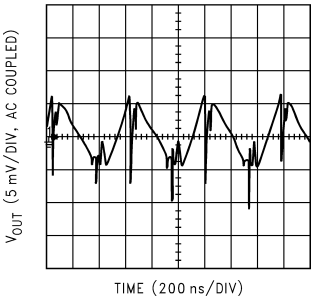


Figure 8. Output Voltage Ripple



I_{OUT} = 120 mA

Figure 9. Output Voltage Ripple

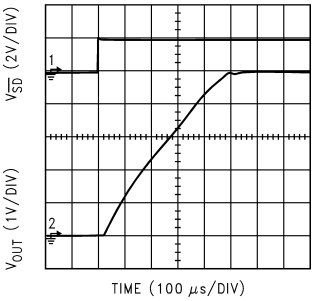


Figure 10. Turnon Behavior

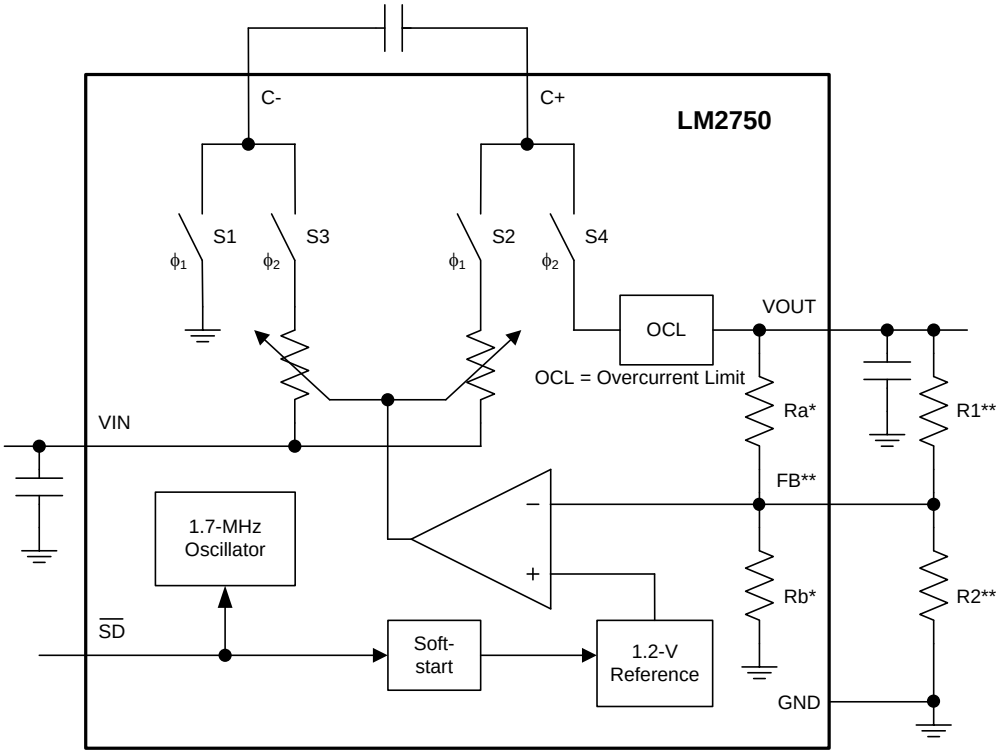
7 Detailed Description

7.1 Overview

The LM2750 is a regulated switched capacitor doubler that, by combining the principles of switched-capacitor voltage boost and linear regulation, generates a regulated output from an extended Li-Ion input voltage range. A two-phase non-overlapping clock generated internally controls the operation of the doubler. During the charge phase (φ1), the flying capacitor (C_{FLY}) is connected between the input and ground through internal pass-transistor switches and is charged to the input voltage. In the pump phase that follows (φ2), the flying capacitor is connected between the input and output through similar switches. Stacked atop the input, the charge of the flying capacitor boosts the output voltage and supplies the load current.

A traditional switched capacitor doubler operating in this manner uses switches with very low on-resistance to generate an output voltage that is 2× the input voltage. The LM2750 regulates the output voltage by controlling the resistance of the two input-connected pass-transistor switches in the doubler.

7.2 Functional Block Diagram



* LM2750-5.0 only
** LM2750-ADJ only

7.3 Feature Description

7.3.1 Pre-Regulation

The very low input current ripple of the LM2750, which results from internal pre-regulation, adds very little noise to the input line. The core of the LM2750 is very similar to that of a basic switched capacitor doubler: it is composed of four switches and a flying capacitor (external). Regulation is achieved by modulating the on-resistance of the two switches connected to the input pin (one switch in each phase). The regulation is done before the voltage doubling, giving rise to the term *pre-regulation*. It is pre-regulation that eliminates most of the input current ripple that is a typical and undesirable characteristic of a many switched capacitor converters.

Feature Description (continued)

7.3.2 Input, Output, and Ground Connections

Making good input, output, and ground connections is essential to achieve optimal LM2750 performance. The two input pads, pads 8 and 9, must be connected externally. It is strongly recommended that the input capacitor (C_{IN}) be placed as close to the LM2750 device as possible, so that the traces from the input pads are as short and straight as possible. To minimize the effect of input noise on LM2750 performance, it is best to bring two traces out from the LM2750 all the way to the input capacitor pad, so that they are connected at the capacitor pad. Connecting the two input traces between the input capacitor and the LM2750 input pads could make the LM2750 more susceptible to noise-related performance degradation. TI also recommends that the input capacitor be on the same side of the PCB as the LM2750, and that traces remain on this side of the board as well (vias to traces on other PCB layers are not recommended between the input capacitor and LM2750 input pads).

The two output pads, pads 1 and 2, must also be connected externally. TI recommends that the output capacitor (C_{OUT}) be placed as close to the LM2750 output pads as possible. It is best if routing of output pad traces follow guidelines similar to those presented for the input pads and capacitor. The flying capacitor (C_{FLY}) must also be placed as close to the LM2750 device as possible to minimize PCB trace length between the capacitor and the device. Due to the pad-layout of the part, it is likely that the trace from one of the flying capacitor pads (C+ or C–) must be routed to an internal or opposite-side layer using vias. This is acceptable, and it is much more advantageous to route a flying capacitor trace in this fashion than it is to place input traces on other layers.

The GND pads of the LM2750 are ground connections and must be connected externally. These include pads 3 (LM2750-5.0 only), 5, 6, and the die-attach pad (DAP). Large, low-impedance copper fills and via connections to an internal ground plane are the preferred way of connecting together the ground pads of the LM2750, the input capacitor, and the output capacitor, as well as connecting this circuit ground to the system ground of the PCB.

7.3.3 Shutdown

When the voltage on the active-low-logic shutdown pin is low, the LM2750 is in shutdown mode. In shutdown, the LM2750 draws virtually no supply current. There is a 200-kΩ pulldown resistor tied between the $\overline{SD}$ pin and GND that pulls the $\overline{SD}$ pin voltage low if the pin is not driven by a voltage source. When pulling the part out of shutdown, the voltage source connected to the $\overline{SD}$ pin must be able to drive the current required by the 200-kΩ resistor. For voltage management purposes required upon start-up, internal switches connect the output of the LM2750 to an internal pulldown resistor (1 kΩ typical) when the part is shut down. Driving the output of the LM2750 by another supply when the LM2750 is shut down is not recommended, as the pulldown resistor was not sized to sink continuous current.

7.3.4 Soft Start

The LM2750 employs soft-start circuitry to prevent excessive input inrush currents during start-up. The output voltage is programmed to rise from 0 V to the nominal output voltage (5 V) in 500 µs (typical). Soft start is engaged when a part, with input voltage established, is taken out of shutdown mode by pulling the $\overline{SD}$ pin voltage high. Soft start also engages when voltage is established simultaneously to the input and $\overline{SD}$ pins.

7.3.5 Output Current Capability

The LM2750-5.0 provides 120 mA of output current when the input voltage is within 2.9 V to 5.6 V. Using the LM2750 to drive loads in excess of 120 mA is possible.

NOTE

Understanding relevant application issues is recommended and a thorough analysis of the application circuit must be performed when using the part outside operating ratings and/or specifications to ensure satisfactory circuit performance in the application. Special care must be paid to power dissipation and thermal effects. These parameters can have a dramatic impact on high-current applications, especially when the input voltage is high. (see *Power Efficiency And Power Dissipation*).

Feature Description (continued)

The schematic of Figure 11 is a simplified model of the LM2750 that is useful for evaluating output current capability. The model shows a linear pre-regulation block (Reg), a voltage doubler (2×), and an output resistance (R_{OUT}). Output resistance models the output voltage droop that is inherent to switched capacitor converters. The output resistance of the LM2750 is 5 Ω (typical), and is approximately equal to twice the resistance of the four LM2750 switches. When the output voltage is in regulation, the regulator in the model controls the voltage V' to keep the output voltage equal to 5 V ± 4%. With increased output current, the voltage drop across R_{OUT} increases. To prevent droop in output voltage, the voltage drop across the regulator is reduced, V' increases, and V_{OUT} remains at 5V. When the output current increases to the point that there is zero voltage drop across the regulator, V' equals the input voltage, and the output voltage is "on the edge" of regulation. Additional output current causes the output voltage to fall out of regulation, and the LM2750 operation is similar to a basic open-loop doubler. As in a voltage doubler, increase in output current results in output voltage drop proportional to the output resistance of the doubler. The out-of-regulation LM2750 output voltage can be approximated by:

$$V_{OUT} = 2 \times V_{IN} - I_{OUT} \times R_{OUT} \quad (1)$$

Again, Equation 1 only applies at low input voltage and high output current where the LM2750 is not regulating. See Figure 1 and Figure 2 in for more details.

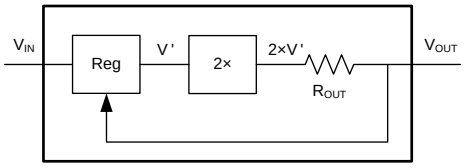


Figure 11. LM2750 Output Resistance Model

A more complete calculation of output resistance takes into account the effects of switching frequency, flying capacitance, and capacitor equivalent series resistance (ESR). See Equation 2:

$$R_{OUT} = 2 \times R_{SW} + \frac{1}{F_{SW} \times C_{FLY}} + 4 \times ESR_{CFLY} + ESR_{COUT} \quad (2)$$

Switch resistance (5 Ω typical) dominates the output resistance equation of the LM2750. With a 1.7-MHz typical switching frequency, the 1/(F×C) component of the output resistance contributes only 0.6 Ω to the total output resistance. Increasing the flying capacitance only provides minimal improvement to the total output current capability of the LM2750. In some applications it may be desirable to reduce the value of the flying capacitor below 1 µF to reduce solution size and/or cost, but this must be done with care so that output resistance does not increase to the point that undesired output voltage droop results. If ceramic capacitors are used, equivalent series resistance (ESR) is a negligible factor in the total output resistance, as the ESR of quality ceramic capacitors is typically much less than 100 mΩ.

7.3.6 Thermal Shutdown

The LM2750 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the part switches into shutdown mode. The LM2750 releases thermal shutdown when the junction temperature of the part is reduced to 130°C (typical).

Thermal shutdown is most-often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. LM2750 power dissipation increases with increased output current and input voltage (see *Power Efficiency And Power Dissipation*). When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped be reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the LM2750. The WSON package has excellent thermal properties that, when soldered to a PCB designed to aid thermal dissipation, allows the LM2750 to operate under very demanding power dissipation conditions.

Feature Description (continued)

7.3.7 Output Current Limiting

The LM2750 contains current limit circuitry that protects the device in the event of excessive output current and/or output shorts to ground. Current is limited to 300 mA (typical) when the output is shorted directly to ground. When the LM2750 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling must be expected (see *Thermal Shutdown*).

7.3.8 Programming the Output Voltage of the LM2750-ADJ

As shown in Figure 12, the output voltage of the LM2750-ADJ can be programmed with a simple resistor divider (see resistors R1 and R2). The values of the feedback resistors set the output voltage, as determined by Equation 3:

$$V_{OUT} = 1.23\ V \times (1 + R1/\ R2) \quad (3)$$

In Equation 3, 1.23 V is the nominal voltage of the feedback pin when the feedback loop is correctly established, and the device is operating normally. The sum of the resistance of the two feedback resistors must be from 15 kΩ to 20 kΩ: $15\ k\Omega < (R1 + R2) < 20\ k\Omega$.

If larger feedback resistors are desired, a 10-pF capacitor must be placed in parallel with resistor R1.

7.4 Device Functional Modes

7.4.1 PWM Brightness/Dimming Control

Brightness of the LEDs can be adjusted in an application by driving the $\overline{SD}$ pin of the LM2750 with a PWM signal. When the PWM signal is high, the LM2750 is ON, and current flows through the LEDs, as described in the previous section. A low PWM signal turns the part and the LEDs OFF. The perceived brightness of the LEDs is proportional to ON current of the LEDs and the duty cycle (D) of the PWM signal (the percentage of time the LEDs are ON).

To achieve good brightness/dimming control with this circuit, proper selection of the PWM frequency is required. The PWM frequency (f_{PWM}) must be set higher than 100 Hz to avoid visible flickering of the LED light. An upper bound on this frequency is also needed to accommodate the turn-on time of the LM2750 (T_{ON} = 0.5 ms typical). This maximum recommended PWM frequency is similarly dependent on the minimum duty cycle (D_{MIN}) of the application. The next equation puts bounds on the recommended PWM frequency range:

$$100\ Hz < F_{PWM} < D_{MIN} \div T_{ON} \quad (4)$$

Choosing a PWM frequency within these limits results in fairly linear control of the time-averaged LED current over the full duty-cycle adjustment range. For most applications, a PWM frequency from 100 Hz to 500 Hz is recommended. A PWM frequency up to 1 kHz may be acceptable in some designs.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Voltage Ripple

The amount of voltage ripple on the output of the LM2750 is highly dependent on the application conditions: output current and the output capacitor, specifically. A simple approximation of output ripple is determined by calculating the amount of voltage droop that occurs when the output of the LM2750 is not being driven. This occurs during the charge phase (φ1). During this time, the load is driven solely by the charge on the output capacitor. The magnitude of the ripple thus follows the basic discharge equation for a capacitor (I = C × dV/dt), where discharge time is one-half the switching period, or $0.5/F_{SW}$. Put simply,

$$RIPPLE_{Peak-Peak} = \frac{I_{OUT}}{C_{OUT}} \times \frac{0.5}{F_{SW}} \quad (5)$$

A more thorough and accurate examination of factors that affect ripple requires including effects of phase non-overlap times and output capacitor equivalent series resistance (ESR). In order for the LM2750 to operate properly, the two phases of operation must never coincide. (If this were to happen all switches would be closed simultaneously, shorting input, output, and ground). Thus, non-overlap time is built into the clocks that control the phases. Because the output is not being driven during the non-overlap time, this time must be accounted for in calculating ripple. Actual output capacitor discharge time is approximately 60% of a switching period, or $0.6/F_{SW}$.

The ESR of the output capacitor also contributes to the output voltage ripple, as there is effectively an AC voltage drop across the ESR due to current switching in and out of the capacitor. Equation 6 is a more complete calculation of output ripple than presented previously, taking into account phase non-overlap time and capacitor ESR.

$$RIPPLE_{Peak-Peak} = \frac{I_{OUT}}{C_{OUT}} \times \frac{0.6}{F_{SW}} + (2 \times I_{OUT} \times ESR_{COUT}) \quad (6)$$

A low-ESR ceramic capacitor is recommended on the output to keep output voltage ripple low. Placing multiple capacitors in parallel can reduce ripple significantly, both by increasing capacitance and reducing ESR. When capacitors are in parallel, ESR is in parallel as well. The effective net ESR is determined according to the properties of parallel resistance. Two identical capacitors in parallel have twice the capacitance and half the ESR as compared to a single capacitor of the same make. On a similar note, if a large-value, high-ESR capacitor (tantalum, for example) is to be used as the primary output capacitor, the net output ESR can be significantly reduced by placing a low-ESR ceramic capacitor in parallel with this primary output capacitor.

8.2 Typical Applications

8.2.1 LM2750-ADJ Typical Application

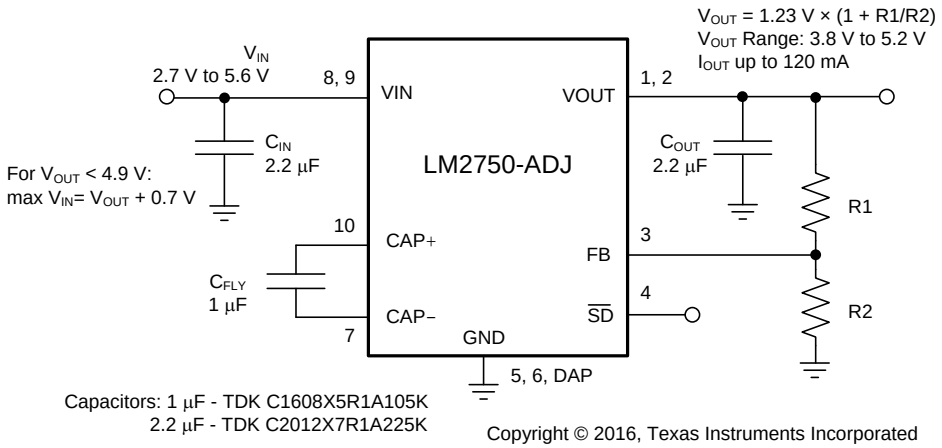


Figure 12. LM2750-ADJ Typical Application Circuit

8.2.1.1 Design Requirements

Example requirements for LM2750-ADJ:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 5.6 V
Output current, 2.9 V ≤ 5.6 V	up to 120 mA
Output current, 2.7 V ≤ 2.9 V	up to 40 mA
Switching frequency	1.7 MHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Capacitors

The LM2750 requires three external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (≤ 10 mΩ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM2750 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM2750. These capacitors have tight capacitance tolerance (as good as ±10%), hold their value over temperature (X7R: ±15% over –55°C to +125°C; X5R: ±15% over –55°C to

=85°C), and typically have little voltage coefficient. Capacitors with Y5V and/or Z5U temperature characteristic are generally not recommended. These types of capacitors typically have wide capacitance tolerance (80%, –20%), vary significantly over temperature (Y5V: 22%, –82% over –30°C to +85°C range; Z5U: 22%, –56% over 10°C to 85°C range), and have poor voltage coefficients. Under some conditions, a nominal 1-µF Y5V or Z5U capacitor could have a capacitance of only 0.1 µF. Such detrimental deviation is likely to cause these Y5V and Z5U of capacitors to fail to meet the minimum capacitance requirements of the LM2750.

Table 1 lists some leading ceramic capacitor manufacturers.

Table 1. Suggested Capacitors

MANUFACTURER	CONTACT INFORMATION
TDK	www.component.tdk.com
AVX	www.avx.com
Murata	www.murata.com
Taiyo-Yuden	www.t-yuden.com
Vishay-Vitramon	www.vishay.com

8.2.1.2.2 Input Capacitor

The input capacitor (C_{IN}) is used as a reservoir of charge, helping to quickly transfer charge to the flying capacitor during the charge phase (φ1) of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase, when the flying capacitor is first connected to the input, and helps to filter noise on the input pin that could adversely affect sensitive internal analog circuitry biased off the input line. As mentioned above, an X7R/X5R ceramic capacitor is recommended for use. For applications where the maximum load current required is from 60 mA to 120 mA, a minimum input capacitance of 2 µF is required. For applications where the maximum load current is 60 mA or less, 1 µF of input capacitance is sufficient. Failure to provide enough capacitance on the LM2750 input can result in poor part performance, often consisting of output voltage droop, excessive output voltage ripple and/or excessive input voltage ripple.

A minimum voltage rating of 10 V is recommended for the input capacitor. This is to account for DC bias properties of ceramic capacitors. Capacitance of ceramic capacitors reduces with increased DC bias. This degradation can be quite significant (> 50%) when the DC bias approaches the voltage rating of the capacitor.

8.2.1.2.3 Flying Capacitor

The flying capacitor (C_{FLY}) transfers charge from the input to the output, providing the voltage boost of the doubler. A polarized capacitor (tantalum, aluminum electrolytic, etc.) must not be used here, as the capacitor is reverse-biased upon start-up of the LM2750. The size of the flying capacitor and its ESR affect output current capability when the input voltage of the LM2750 is low, most notable for input voltages below 3 V. These issues were discussed previously in *Output Current Capability*. For most applications, a 1-µF X7R/X5R ceramic capacitor is recommended for the flying capacitor.

8.2.1.2.4 Output Capacitor

The output capacitor of the LM2750 plays an important part in determining the characteristics of the output signal of the LM2750, many of which have already been discussed. The ESR of the output capacitor affects charge pump output resistance, which plays a role in determining output current capability. Both output capacitance and ESR affect output voltage ripple. For these reasons, a low-ESR X7R/X5R ceramic capacitor is the capacitor of choice for the LM2750 output.

In addition to these issues previously discussed, the output capacitor of the LM2750 also affects control-loop stability of the part. Instability typically results in the switching frequency effectively reducing by a factor of two, giving excessive output voltage droop and/or increased voltage ripple on the output and the input. With output currents of 60 mA or less, a minimum capacitance of 1 µF is required at the output to ensure stability. For output currents from 60 mA to 120 mA, a minimum output capacitance of 2 µF is required.

A minimum voltage rating of 10 V is recommended for the output capacitor. This is to account for DC bias properties of ceramic capacitors. Capacitance of ceramic capacitors reduces with increased DC bias. This degradation can be quite significant (> 50%) when the DC bias approaches the voltage rating of the capacitor.

8.2.1.2.5 Power Efficiency And Power Dissipation

Efficiency of the LM2750 mirrors that of an unregulated switched capacitor converter followed by a linear regulator. The simplified power model of the LM2750, in Figure 13, is used to discuss power efficiency and power dissipation. In calculating power efficiency, output power (P_{OUT}) is easily determined as the product of the output current and the 5-V output voltage. Like output current, input voltage is an application-dependent variable. The input current can be calculated using the principles of linear regulation and switched capacitor conversion. In an ideal linear regulator, the current into the circuit is equal to the current out of the circuit. The principles of power conservation mandate the ideal input current of a voltage doubler must be twice the output current. Adding a correction factor for operating quiescent current (I_Q, 5-mA typical) gives an approximation for total input current which, when combined with the other input and output parameter(s), yields Equation 7 for efficiency:

$$E = \frac{P_{OUT}}{P_{IN}} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times (2 \times I_{OUT} + I_Q)} \quad (7)$$

Comparisons of LM2750 efficiency measurements to calculations using Equation 7 have shown a quite accurate approximation of actual efficiency. Because efficiency is inversely proportional to input voltage, it is highest when the input voltage is low. In fact, for an input voltage of 2.9 V, efficiency of the LM2750 is greater than 80% (I_{OUT} ≥ 40 mA) and peak efficiency is 85% (I_{OUT} = 120 mA). The average efficiency for an input voltage range spanning the Li-Ion range (2.9 V to 4.2 V) is 70% (I_{OUT} = 120 mA). At higher input voltages, efficiency drops dramatically. In Li-Ion-powered applications, this is typically not a major concern, as the circuit is powered off by a charger in these circumstances. Low efficiency equates to high power dissipation, however, which could become an issue worthy of attention.

The LM2750 power dissipation (P_D) is calculated simply by subtracting output power from input power:

$$P_D = P_{IN} - P_{OUT} = [V_{IN} \times (2 \times I_{OUT} + I_Q)] - [V_{OUT} \times I_{OUT}] \quad (8)$$

Power dissipation increases with increased input voltage and output current, up to 772 mW at the ends of the operating ratings (V_{IN} = 5.6 V, I_{OUT} = 120 mA). Internal power dissipation self-heats the device. Dissipating this amount power/heat so the LM2750 does not overheat is a demanding thermal requirement for a small surface-mount package. When soldered to a PCB with layout conducive to power dissipation, the excellent thermal properties of the WSON package enable this power to be dissipated from the LM2750 with little or no derating, even when the circuit is placed in elevated ambient temperatures.

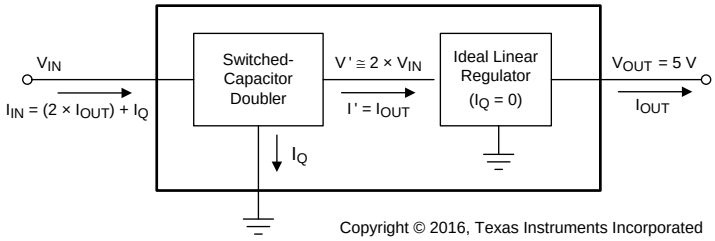


Figure 13. LM2750 Model for Power Efficiency and Power Dissipation Calculations

8.2.1.3 Application Curve

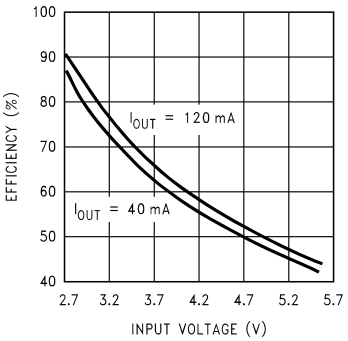


Figure 14. Power Efficiency

8.2.2 LM2750 LED Drive Applications

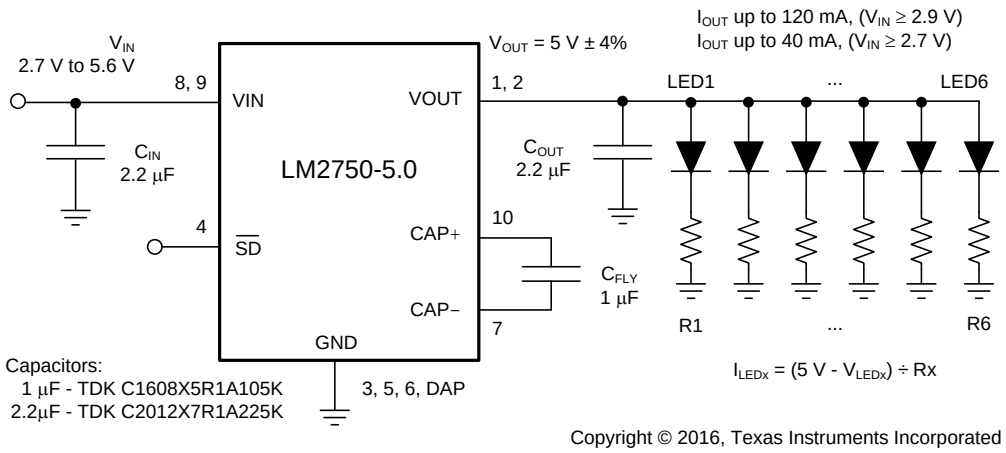


Figure 15. LM2750-5.0 LED Drive Application Circuit

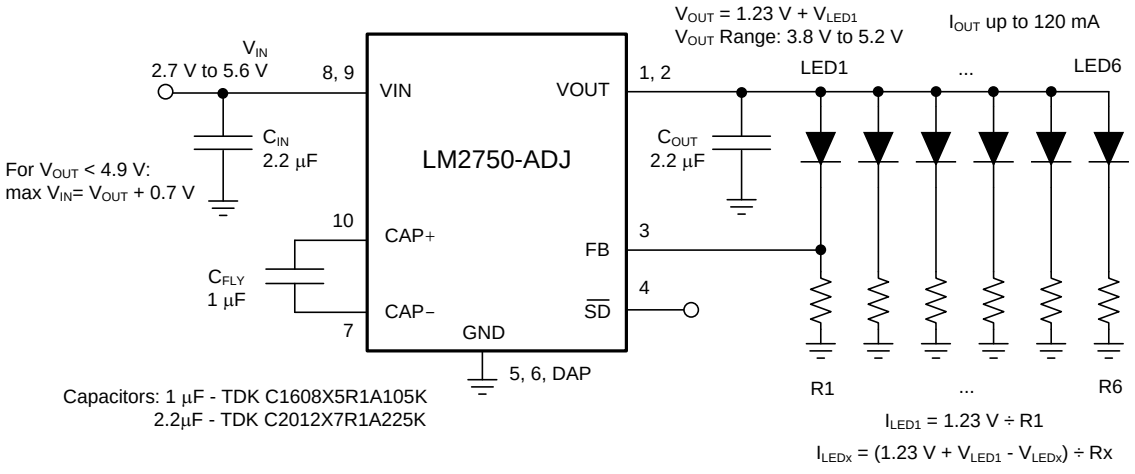


Figure 16. LM2750-ADJ LED Drive Application Circuit

8.2.2.1 Design Requirements

See *Design Requirements*.

8.2.2.2 Detailed Design Requirements

The LM2750 is an excellent device for driving white and blue LEDs for display backlighting and other general-purpose lighting functions. The circuits of Figure 15 and Figure 16 show LED driver circuits for the LM2750-5.0 and the LM2750-ADJ, respectively. Simply placing a resistor (R) in series with each LED sets the current through the LEDs:

$$I_{LED} = (V_{OUT} - V_{LED}) \div R \quad (9)$$

In Equation 9, I_{LED} is the current that flows through a particular LED, and V_{LED} is the forward voltage of the LED at the given current. As can be seen in Equation 9 above, LED current varies with changes in LED forward voltage (V_{LED}). Mismatch of LED currents results in brightness mismatch from one LED to the next.

The feedback pin of the LM2750-ADJ can be utilized to help better control brightness levels and negate the effects of LED forward voltage variation. As shown in Figure 16, connecting the feedback pin to the primary LED-resistor junction (LED1-R1) regulates the current through that LED. The voltage across the primary resistor (R1) is the feedback pin voltage (1.23 V typical), and the current through the LED is the current through that resistor. Current through all other LEDs (LEDx) is not regulated, however, and varies with LED forward voltage variations.

When using the LM2750-ADJ in current-mode, LED currents can be calculated with Equation 10 and Equation 11:

$$I_{LED1} = 1.23\,V \div R1 \quad (10)$$

$$I_{LEDx} = (1.23\,V + V_{LED1} - V_{LEDx}) \div Rx \quad (11)$$

The current-mode configuration does not improve brightness matching from one LED to another in a single circuit, but keeps currents similar from one circuit to the next. For example: if there is forward voltage mismatch from LED1 to LED2 on a single board, the current-mode LM2750-ADJ solution provides no benefit. But if the forward voltage of LED1 on one board is different than the forward voltage of LED1 on another board, the currents through LED1 in both phones will match. This helps keep LED currents fairly consistent from one product to the next, and helps to offset lot-to-lot variation of LED forward voltage characteristics.

8.2.2.2.1 LED Driver Power Efficiency

Efficiency of an LED driver (E_{LED}) is typically defined as the power consumed by the LEDs (P_{LED}) divided by the power consumed at the input of the circuit. Input power consumption of the LM2750 was explained and defined in the previous section titled: . Assuming LED forward voltages and currents match reasonably well, LED power consumption is the product of the number of LEDs in the circuit (N), the LED forward voltage (V_{LED}), and the LED forward current (I_{LED}):

$$P_{LED} = N \times V_{LED} \times I_{LED} \quad (12)$$

$$E_{LED} = P_{LED} \div P_{IN} = (N \times V_{LED} \times I_{LED}) \div \{V_{IN} \times [(2 \times I_{OUT}) + 5\,mA]\} \quad (13)$$

8.2.2.3 Application Curve

Figure 17 is an efficiency curve for a typical LM2750 LED-drive application.

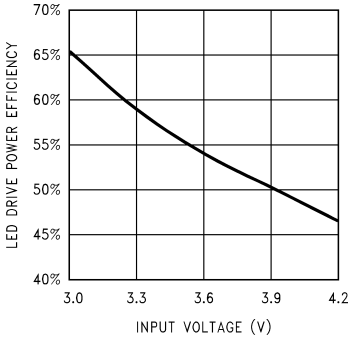


Figure 17. LM2750 LED Drive Efficiency, 6 LEDs
I_{LED} = 20 mA each, V_{LED} = 4 V

9 Power Supply Recommendations

The LM2750 is designed to operate from an input voltage supply range from 2.7 V to 5.6 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

9.1 LED Driver Power Consumption

For battery-powered LED-drive applications, TI strongly recommends that power consumption, rather than power efficiency, be used as the metric of choice when evaluating power conversion performance. Power consumed (P_{IN}) is simply the product of input voltage (V_{IN}) and input current (I_{IN}):

$$P_{IN} = V_{IN} \times I_{IN} \quad (14)$$

The LM2750 input current is equal to twice the output current (I_{OUT}), plus the supply current of the part (nominally 5 mA):

$$I_{IN} = (2 \times I_{OUT}) + 5\ mA \quad (15)$$

Output voltage and LED voltage do not impact the amount of current consumed by the LM2750 circuit. Thus, neither factor affects the current draw on a battery. Because output voltage does not impact input current, there is no power savings with either the LM2750-5.0 or the LM2750-ADJ; both options consume the same amount of power.

In *LED Driver Power Efficiency*, LED Driver Efficiency was defined in Equation 13.

Equation 13 can be simplified by recognizing

- $2 \times I_{OUT} > 5$ mA (high output-current applications);
- $N \times I_{LED} = I_{OUT}$

Thus, simplification yields: $E_{LED} = V_{LED} / V_{IN}$.

This is in direct contrast to the previous assertion that showed that power consumption was completely independent of LED voltage. As is the case here with the LM2750, efficiency is often not a good measure of power conversion effectiveness of LED driver topologies. This is why it is strongly recommended that power consumption be studied or measured when comparing the power conversion effectiveness of LED drivers.

Additionally, efficiency of an LED drive solution must not be confused with an efficiency calculation for a standard power converter (E_P).

$$E_P = P_{OUT} \div P_{IN} = (V_{OUT} \times I_{OUT}) \div (V_{IN} \times I_{IN}) \quad (16)$$

Equation 16 neglects power losses in the external resistors that set LED currents and is a very poor metric of LED-drive power conversion performance.

10 Layout

10.1 Layout Recommendations

A good board layout of the LM2750 circuit is required to achieve optimal assembly, electrical, and thermal dissipation performance. Figure 18 is an example of a board layout implementing recommended techniques. For more information related to layout for the WSON/SON package, see *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

General guidelines for board layout are:

- Place capacitors as close to the LM2750 device as possible and on the same side of the board. V_{IN} and V_{OUT} connections are most critical: run short traces from the LM2750 pads directly to these capacitor pads.
- Connect the ground pins of the LM2750 and the capacitors to a good ground plane. The ground plane is essential for both electrical and thermal dissipation performance.
- For optimal thermal performance, make the ground plane(s) as large as possible. Connect the die-attach pad (DAP) of the LM2750 to the ground plane(s) with wide traces and/or multiple vias. Top-layer ground planes are most effective in increasing the thermal dissipation capability of the WSON package. Large internal ground planes are also very effective in keeping the die temperature of the LM2750 within operating ratings.

10.2 Layout Example

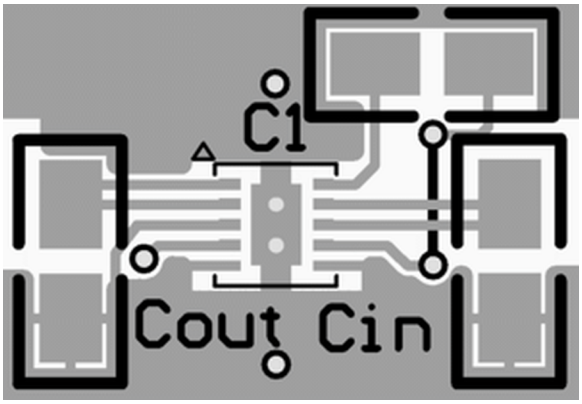


Figure 18. LM2750-5.0 Recommended Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).

11.2.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2750	Click here	Click here	Click here	Click here	Click here
LM2750-ADJ	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2750LD-5.0/NOPB	ACTIVE	WSON	NGY	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	S002B	Samples
LM2750LD-ADJ/NOPB	ACTIVE	WSON	NGY	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	S003B	Samples
LM2750LDX-5.0/NOPB	ACTIVE	WSON	NGY	10	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	S002B	Samples
LM2750SD-5.0/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	S005B	Samples
LM2750SD-ADJ/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	S004B	Samples
LM2750SDX-5.0/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		S005B	Samples
LM2750SDX-ADJ/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	S004B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

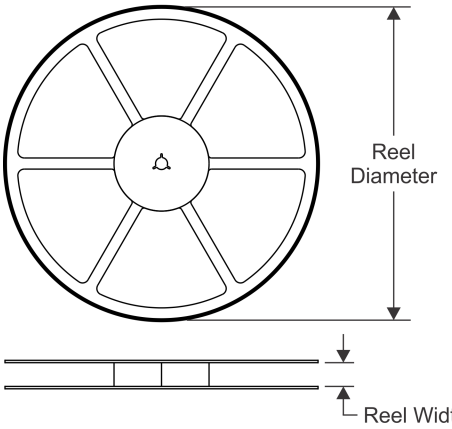
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

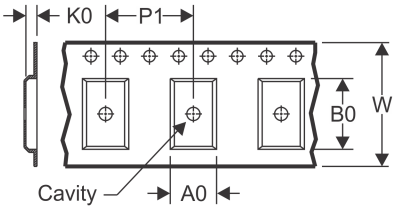
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

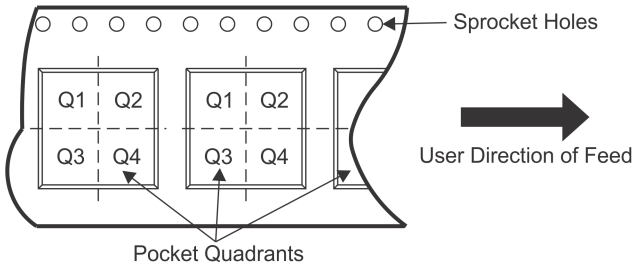


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

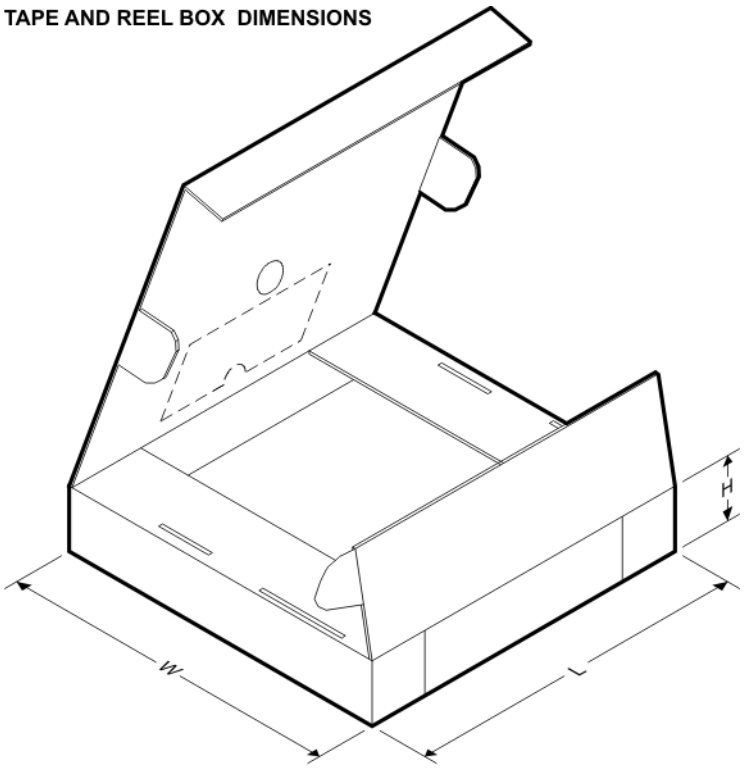
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2750LD-5.0/NOPB	WSON	NGY	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2750LD-ADJ/NOPB	WSON	NGY	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2750LDX-5.0/NOPB	WSON	NGY	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2750SD-5.0/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2750SD-ADJ/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2750SDX-5.0/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2750SDX-ADJ/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

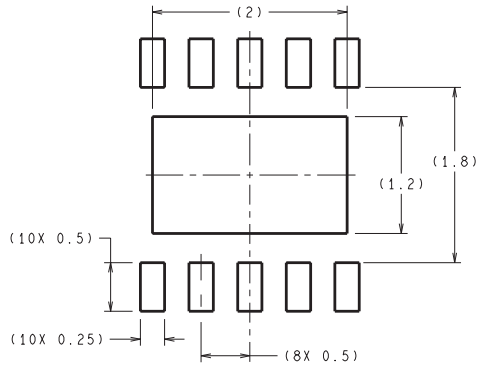
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

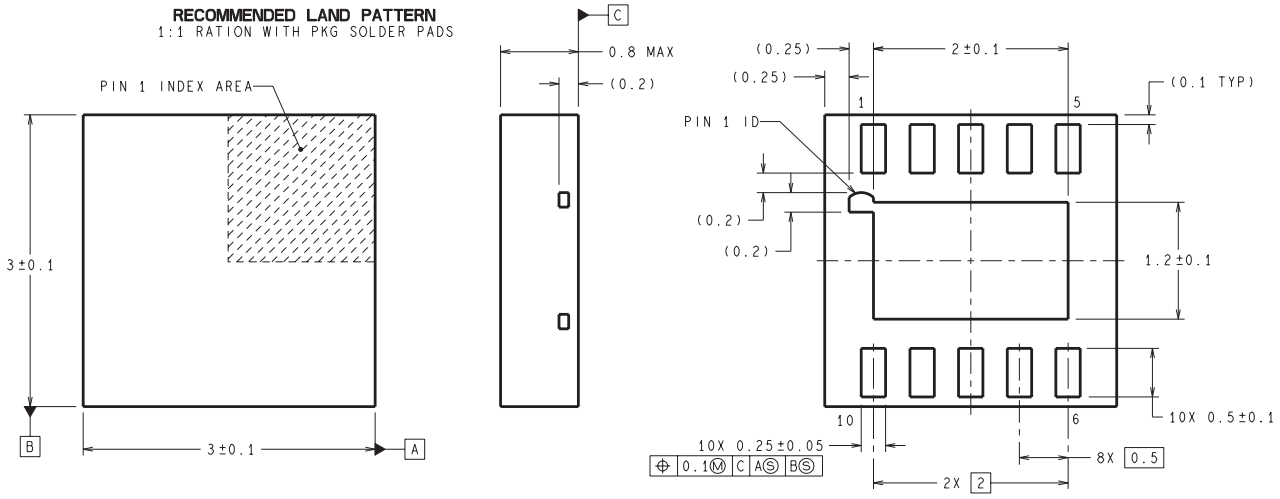
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2750LD-5.0/NOPB	WSON	NGY	10	1000	210.0	185.0	35.0
LM2750LD-ADJ/NOPB	WSON	NGY	10	1000	210.0	185.0	35.0
LM2750LDX-5.0/NOPB	WSON	NGY	10	4500	367.0	367.0	35.0
LM2750SD-5.0/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM2750SD-ADJ/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM2750SDX-5.0/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0
LM2750SDX-ADJ/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

NGY0010A



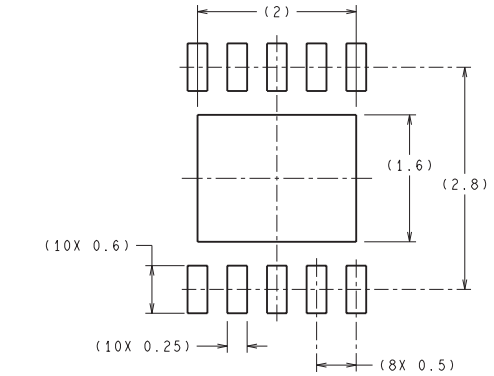
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



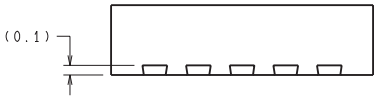
LDA10A (Rev B)

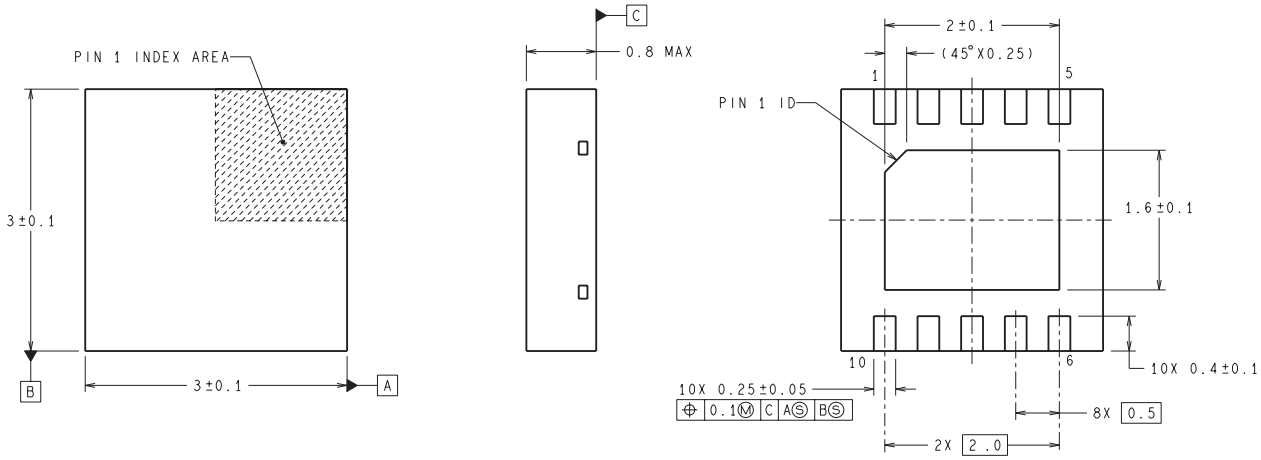
DSC0010A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SDA10A (Rev A)

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