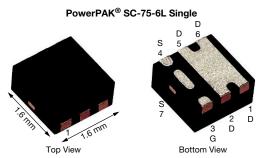


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Vishay Siliconix

## N-Channel 20 V (D-S) MOSFET



Marking code: AD

PRODUCT SUMMARY									
V <sub>DS</sub> (V)	20								
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.046								
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5 \text{ V}$	0.063								
Q <sub>g</sub> typ. (nC)	3.5								
I <sub>D</sub> (A) <sup>a</sup>	6								
Configuration	Single								

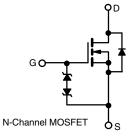
#### **FEATURES**

- TrenchFET® power MOSFET
- New thermally enhanced PowerPAK<sup>®</sup> SC-75 package
  - Small footprint area
  - Low on-resistance
- Typical ESD protection 560 V
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

# ROHS COMPLIANT HALOGEN

#### **APPLICATIONS**

- Load switch for portable applications
- High frequency DC/DC converter



ORDERING INFORMATION						
Package	SC-75					
Lead (Pb)-free and halogen-free	SiB406EDK-T1-GE3					

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)							
PARAMETER		SYMBOL	LIMIT	UNIT			
Drain-source voltage		V <sub>DS</sub>	20	V			
Gate-source voltage		V <sub>GS</sub>	± 12	V			
	T <sub>C</sub> = 25 °C		6 <sup>a</sup>				
O-ation and during an area (T. 150 °O)	T <sub>C</sub> = 70 °C	1 . [	6 <sup>a</sup>				
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	5.1 <sup>b, c</sup>				
	T <sub>A</sub> = 70 °C		4.1 <sup>b, c</sup>	Α			
Pulsed drain current	•	I <sub>DM</sub>	15				
Octive a second delication distance and	T <sub>C</sub> = 25 °C		6 <sup>a</sup>				
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	l <sub>S</sub>	1.6 <sup>b, c</sup>				
	T <sub>C</sub> = 25 °C		10				
Maximum power dissipation	T <sub>C</sub> = 70 °C	] [	6.4	10/			
	T <sub>A</sub> = 25 °C	- P <sub>D</sub>	1.95 <sup>b, c</sup>	W			
	T <sub>A</sub> = 70 °C	1	1.25 <sup>b, c</sup>				
Operating junction and storage temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	00				
Soldering recommendations (peak tempera	ture) <sup>d, e</sup>		260	°C			

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum junction-to-ambient b, f	t ≤ 5 s	$R_{thJA}$	51	64	°C ///				
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	10	12.5	°C/W				

#### Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 100 °C/W

# Vishay Siliconix

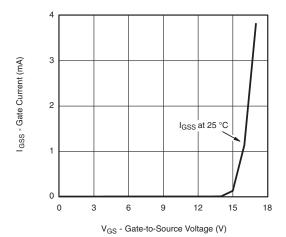
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static			•	•	•	•
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	23	-	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-3.3	-	mV/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \ \mu A$	0.6	-	1.4	V
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	± 8	
Zana mata walta na disala avisuant	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
Zero gate voltage drain current		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	-	-	-10	
On-state drain current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10	-	-	Α
Data a succession and a succession and a		$V_{GS} = 4.5 \text{ V}, I_D = 3.9 \text{ A}$	-	0.037	0.046	
Drain-source on-state resistance a	R <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 3.3 \text{ A}$	-	0.051	0.063	Ω
Forward transconductance a	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 3.9 \text{ A}$	-	14	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>		-	350	-	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	63	-	pF
Reverse transfer capacitance	C <sub>rss</sub>		-	37	-	
<del></del>	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5.1 \text{ A}$	-	7.5	12	nC
Total gate charge			-	3.5	5.5	
Gate-source charge	Q <sub>qs</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5.1 \text{ A}$	-	0.95	-	
Gate-drain charge	Q <sub>ad</sub>		-	0.75	-	
Gate resistance	R <sub>g</sub> f = 1 MHz		-	3.5	-	Ω
Turn-on delay time	t <sub>d(on)</sub>		-	10	15	
Rise time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_{L} = 2.4 \Omega$	-	12	20	
Turn-off delay time	t <sub>d(off)</sub>	$I_D\cong 4.1~A,~V_{GEN}=4.5~V,~R_g=1~\Omega$	-	18	30	
Fall time	t <sub>f</sub>		-	12	20	
Turn-on delay time			-	5	10	ns
Rise time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_{L} = 2.4 \Omega$		12	20	1
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 4.1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	15	25	
Fall time	t <sub>f</sub>		-	10	15	
<b>Drain-Source Body Diode Characteristic</b>	s					1
Continuous source-drain diode current Is		T <sub>C</sub> = 25 °C	-	-	6	
Pulse diode forward current	I <sub>SM</sub>		-	-	15	Α
Body diode voltage V <sub>SD</sub>		I <sub>S</sub> = 4.1 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V
Body diode reverse recovery time $t_{rr}$			-	15	30	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	I <sub>F</sub> = 4.1 A, di/dt = 100 A/μs,	-	8	20	nC
Reverse recovery fall time	t <sub>a</sub>	$T_J = 25  ^{\circ}\text{C}$	-	8	-	
Reverse recovery rise time	t <sub>b</sub>		_	7	_	ns

#### Notes

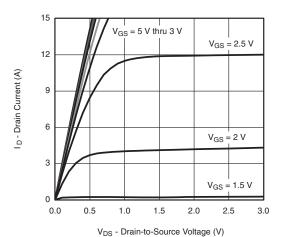
- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

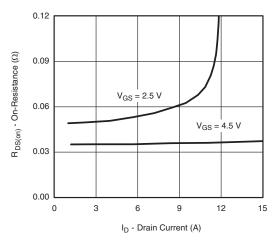




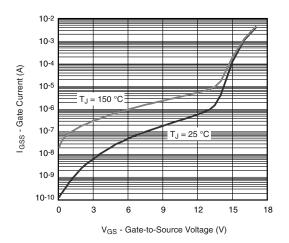
#### Gate Current vs. Gate-Source Voltage



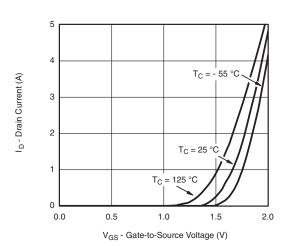
**Output Characteristics** 



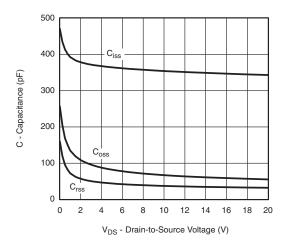
On-Resistance vs. Drain Current and Gate Voltage



Gate Current vs. Gate-Source Voltage

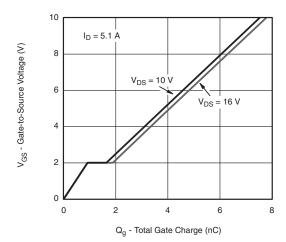


**Transfer Characteristics** 

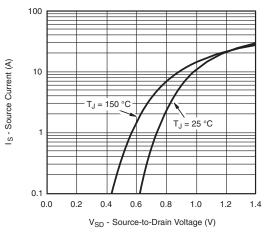


Capacitance

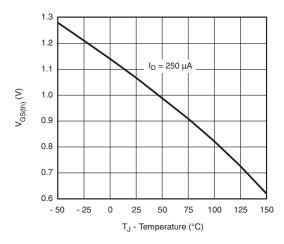




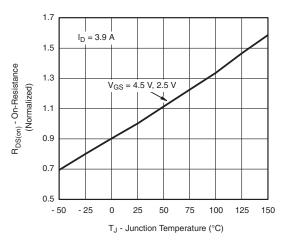
#### **Gate Charge**



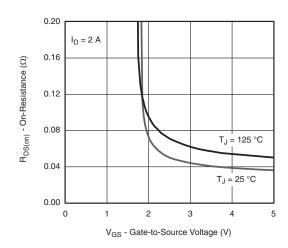
#### Source-Drain Diode Forward Voltage



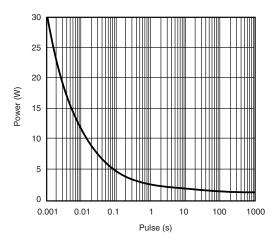
**Threshold Voltage** 



On-Resistance vs. Junction Temperature

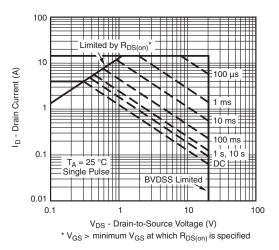


On-Resistance vs. Gate-to-Source Voltage

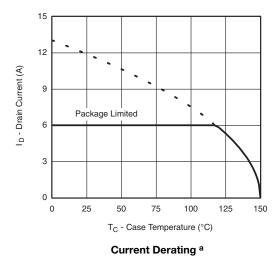


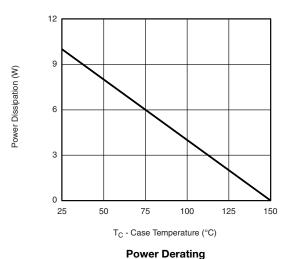
Single Pulse Power (Junction-to-Ambient)





Safe Operating Area, Junction-to-Ambient

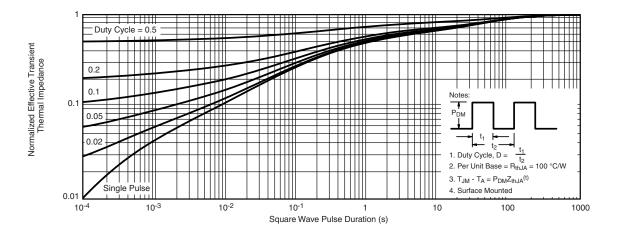




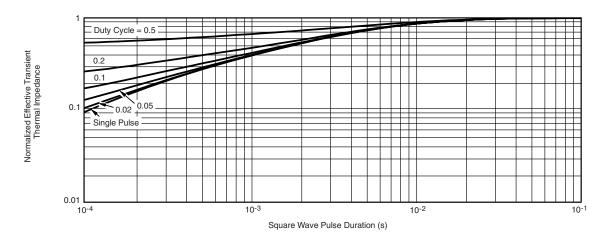
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



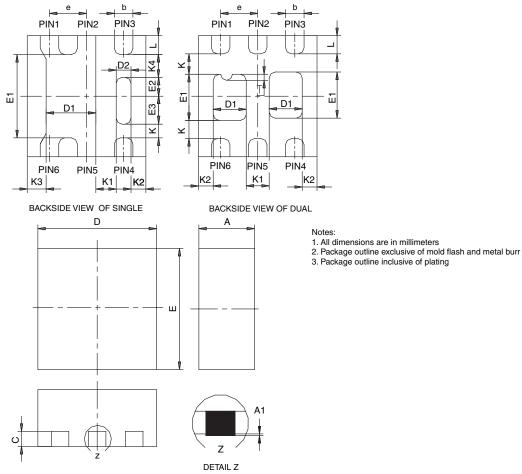
Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® SC75-6L



	SINGLE PAD						DUAL PAD					
DIM	М	ILLIMETER	RS		INCHES		MILLIMETERS		RS		INCHES	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
<b>A</b> 1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
е		0.50 BSC		0.020 BSC 0.50 BSC 0				0.020 BSC				
K		0.180 TYP	)		0.007 TYP	ı	0.245 TYP			0.010 TYP		
K1		0.275 TYP	)	0.011 TYP			0.320 TYP			0.013 TYP		
K2		0.200 TYP	)	0.008 TYP			0.200 BSC			0.008 TYP		
К3		0.255 TYP	)	0.010 TYP								
K4		0.300 TYP	)	0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
Т							0.03	0.08	0.13	0.001	0.003	0.005

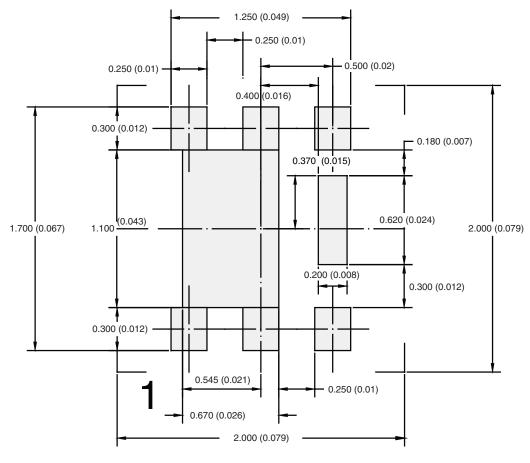
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5935

Document Number: 73000 06-Aug-07



## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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