TEXAS INSTRUMENTS

TPS22965-Q1

SLVSCI3D −APRIL 2014−REVISED DECEMBER 2019

TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch

1 Features

- Qualified for Automotive Applications
  - AEC-Q100 Qualified
  - Device Temperature Grade 2: –40°C to +105°C (TPS22965-Q1, TPS22965N-Q1)
  - Device Temperature Grade 1: –40°C to +125°C (TPS22965W-Q1, TPS22965NW-Q1)
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Functional safety capable
  - Documentation available to aid functional safety system design
- Integrated Single Channel Load Switch
- Input Voltage Range: 0.8 V to 5.5 V
- Ultra-Low On Resistance (R_{ON})
  - R_{ON} = 16 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 16 mΩ at V_{IN} = 3.6 V (V_{BIAS} = 5 V)
  - R_{ON} = 16 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)
- 4-A Maximum Continuous Switch Current
- Low Quiescent Current (50 µA)
- Low Control Input Threshold Enables Use of 1.2-, 1.8-, 2.5- and 3.3-V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD) (TPS22965-Q1 and TPS22965W-Q1 Only)
- WSON 8-pin Package with Thermal Pad

2 Applications

- Automotive Electronics
- Infotainment
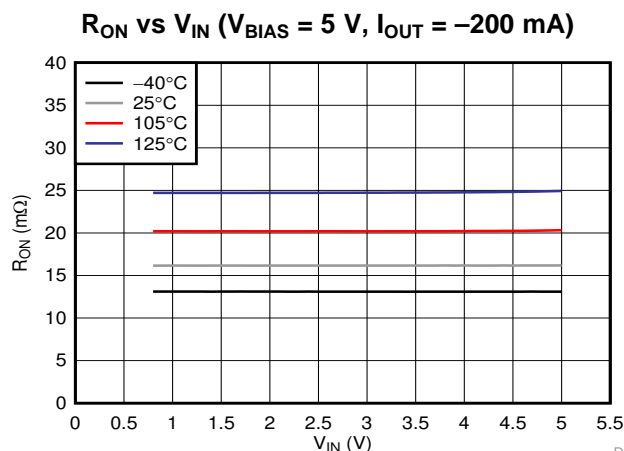- ADAS (Advanced Driver Assistance Systems)
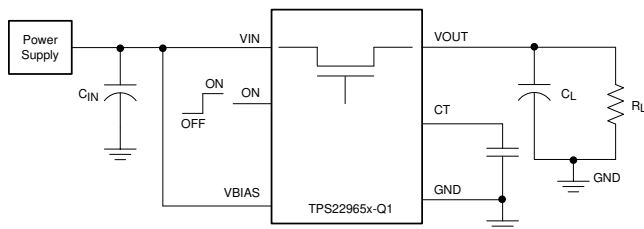
3 Description

The TPS22965x-Q1 is a small, ultralow-R_{ON}, single-channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 4 A. The VOUT rise time is configurable so that inrush current may be reduced. The TPS22965-Q1 and TPS22965W-Q1 devices include a 225-Ω on-chip load resistor for quick output discharge when the switch is turned off.

The TPS22965x-Q1 devices are available in a small, space-saving 2-mm × 2-mm 8-pin WSON package (DSG0008A) with integrated thermal pad allowing for high power dissipation. The TPS22965-Q1 and TPS22965N-Q1 devices are characterized for operation over the free-air temperature range of –40°C to 105°C. Furthermore, the TPS22965W-Q1 and TPS22965NW-Q1 devices feature wettable flanks in the same WSON package (DSG0008B) and it is characterized for operation over the free-air temperature range of –40°C to +125°C.

Device Information [1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22965-Q1	DSG0008A WSON (8)	2.00 mm × 2.00 mm
TPS22965N-Q1		
TPS22965W-Q1	DSG0008B WSON (8)	
TPS22965NW-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

R_{ON} vs V_{IN} (V_{BIAS} = 5 V, I_{OUT} = −200 mA)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2016) to Revision D	**Page**
• Added Functional safety capable link to the *Features* section	1

Changes from Revision B (December 2015) to Revision C	**Page**
• Added package designators in the *Description* section and *Thermal Information* table.	1

Changes from Revision A (June 2015) to Revision B	**Page**
• Updated status of TPS22965W-Q1 part to ACTIVE	1
• Added 125°C temperature performance to typical AC timing parameters	12

Changes from Original (April 2014) to Revision A	**Page**
• Added TPS22965N-Q1 part number.	1
• Updated Thermal Information table.	5
• Updated typical AC timing parameters (tables, graphs and scope captures)	12

Product Folder Links: *TPS22965-Q1*

5   Device Comparison Table

DEVICE	R_{ON} AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE	PACKAGE WITH WETTABLE FLANKS	MAXIMUM OUTPUT CURRENT	TEMPERATURE RANGE
TPS22965-Q1	16 mΩ	Yes	No	4 A	−40°C to +105°C
TPS22965N-Q1	16 mΩ	No	No	4 A	−40°C to +105°C
TPS22965W-Q1	16 mΩ	Yes	Yes	4 A	−40°C to +125°C
TPS22965NW-Q1	16 mΩ	No	Yes	4 A	−40°C to +125°C

6   Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View
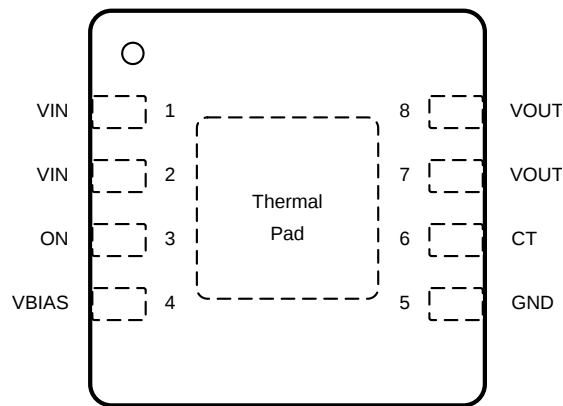
Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the *Application and Implementation* section for more information
2			
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V. See the *Application and Implementation* section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the *Application and Implementation* section for more information
7	VOUT	O	Switch output
8			
—	Thermal pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout* section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

		MIN	MAX	UNIT [2]
V_{IN}	Input voltage	−0.3	6	V
V_{OUT}	Output voltage	−0.3	6	V
V_{BIAS}	Bias voltage	−0.3	6	V
V_{ON}	On voltage	−0.3	6	V
I_{MAX}	Maximum continuous switch current		4	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 μs, 2% duty cycle		6	A
T_J	Maximum junction temperature		150	°C
T_{STG}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.5	V
V_{ON}	ON voltage		0	5.5	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
C_{IN}	Input capacitor		1 [1]		μF
T_A	Operating free-air temperature [2]	TPS22965N-Q1, TPS22965-Q1	−40	105	°C
		TPS22965NW-Q1, TPS22965W-Q1	−40	125	

(1) See the *Application and Implementation* section.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$

7.4 Thermal Information

	THERMAL METRIC[1]	TPS22965-Q1, TPS22965N-Q1 DSG0008A (WSON) 8 PINS	TPS22965W-Q1, TPS22965NW-Q1 DSG0008B (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	67.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	95	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.5	37.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.2	8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature:
–40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1).
Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_Q V_{BIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 5 V		–40°C to +105°C		50	75	µA
				–40°C to +125°C		50	75	
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
				–40°C to +125°C			2	
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +105°C		0.2	8	µA
				–40°C to +125°C			36	
			V_{IN} = 3.3 V	–40°C to +105°C		0.02	3	
				–40°C to +125°C			13	
			V_{IN} = 1.8 V	–40°C to +105°C		0.01	2	
				–40°C to +125°C			6	
			V_{IN} = 0.8 V	–40°C to +105°C		0.005	1	
				–40°C to +125°C			4	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
				–40°C to +125°C			0.5	

Electrical Characteristics—V$_{BIAS}$ = 5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T$_A$ ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T$_A$ ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T$_A$ = 25°C.

PARAMETER		TEST CONDITIONS	T$_A$		MIN	TYP	MAX	UNIT
RESISTANCE CHARACTERISTICS								
R$_{ON}$	ON-state resistance	I$_{OUT}$ = −200 mA, V$_{BIAS}$ = 5 V	V$_{IN}$ = 5 V	25°C		16	23	mΩ
				−40°C to +105°C 965N-Q1, 965-Q1			25	
				−40°C to +105°C 965NW-Q1, 965W-Q1			26	
				−40°C to +125°C			28	
			V$_{IN}$ = 3.3 V	25°C		16	23	mΩ
				−40°C to +105°C 965N-Q1, 965-Q1			25	
				−40°C to +105°C 965NW-Q1, 965W-Q1			26	
				−40°C to +125°C			27	
			V$_{IN}$ = 1.8 V	25°C		16	23	mΩ
				−40°C to +105°C 965N-Q1, 965-Q1			25	
				−40°C to +105°C 965NW-Q1, 965W-Q1			26	
				−40°C to +125°C			27	
			V$_{IN}$ = 1.5 V	25°C		16	23	mΩ
				−40°C to +105°C 965N-Q1, 965-Q1			25	
				−40°C to +105°C 965NW-Q1, 965W-Q1			26	
				−40°C to +125°C			27	
			V$_{IN}$ = 1.2 V	25°C		16	23	mΩ
				−40°C to +105°C 965N-Q1, 965-Q1			25	
				−40°C to +105°C 965NW-Q1, 965W-Q1			26	
				−40°C to +125°C			27	
			V$_{IN}$ = 0.8 V	25°C		16	23	mΩ
				−40°C to +105°C 965N-Q1, 965-Q1			25	
				−40°C to +105°C 965NW-Q1, 965W-Q1			26	
				−40°C to +125°C			27	
R$_{PD}$ [1]	Output pull-down resistance	V$_{IN}$ = 5 V, V$_{ON}$ = 0 V, I$_{OUT}$ = 1 mA	−40°C to +105°C			225	300	Ω
			−40°C to +125°C			225	300	

(1) TPS22965-Q1 and TPS22965W-Q1 Only

Product Folder Links: *TPS22965-Q1*

7.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature:
–40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1).
Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_Q V_{BIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		–40°C to +105°C		20	30	µA
				–40°C to 125°C		20	30	
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
				–40°C to 125°C			2	
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +105°C		0.01	3	µA
				–40°C to 125°C			13	
			V_{IN} = 1.8 V	–40°C to +105°C		0.01	2	
				–40°C to 125°C			6	
			V_{IN} = 1.2 V	–40°C to +105°C		0.005	2	
				–40°C to 125°C			6	
			V_{IN} = 0.8 V	–40°C to +105°C		0.003	1	
				–40°C to 125°C			4	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
				–40°C to +125°C			0.5	

Electrical Characteristics—V$_{BIAS}$ = 2.5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature:
–40°C ≤ T$_A$ ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T$_A$ ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1).
Typical values are for T$_A$ = 25°C.

PARAMETER		TEST CONDITIONS		T$_A$	MIN	TYP	MAX	UNIT
RESISTANCE CHARACTERISTICS								
R$_{ON}$	ON-state resistance	I$_{OUT}$ = –200 mA, V$_{BIAS}$ = 2.5 V	V$_{IN}$ = 2.5 V	25°C	20		26	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			28	
				–40°C to 105°C 965NW-Q1, 965W-Q1			32	
				–40°C to +125°C			34	
			V$_{IN}$ = 1.8 V	25°C	19		26	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			28	
				–40°C to +105°C 965NW-Q1, 965W-Q1			30	
				–40°C to +125°C			32	
			V$_{IN}$ = 1.5 V	25°C	18		25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1/965W-Q1			29	
				–40°C to +125°C			31	
			V$_{IN}$ = 1.2 V	25°C	18		25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1, 965W-Q1			28	
				–40°C to +125°C			30	
			V$_{IN}$ = 0.8 V	25°C	17		25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1, 965W-Q1			28	
				–40°C to +125°C			30	
R$_{PD}$ [1]	Output pulldown resistance	V$_{IN}$ = 2.5 V, V$_{ON}$ = 0 V, I$_{OUT}$ = 1 mA		–40°C to +105°C		275	325	Ω
				–40°C to +125°C		275	330	

(1) TPS22965-Q1 and TPS22965W-Q1 only

Product Folder Links: *TPS22965-Q1*
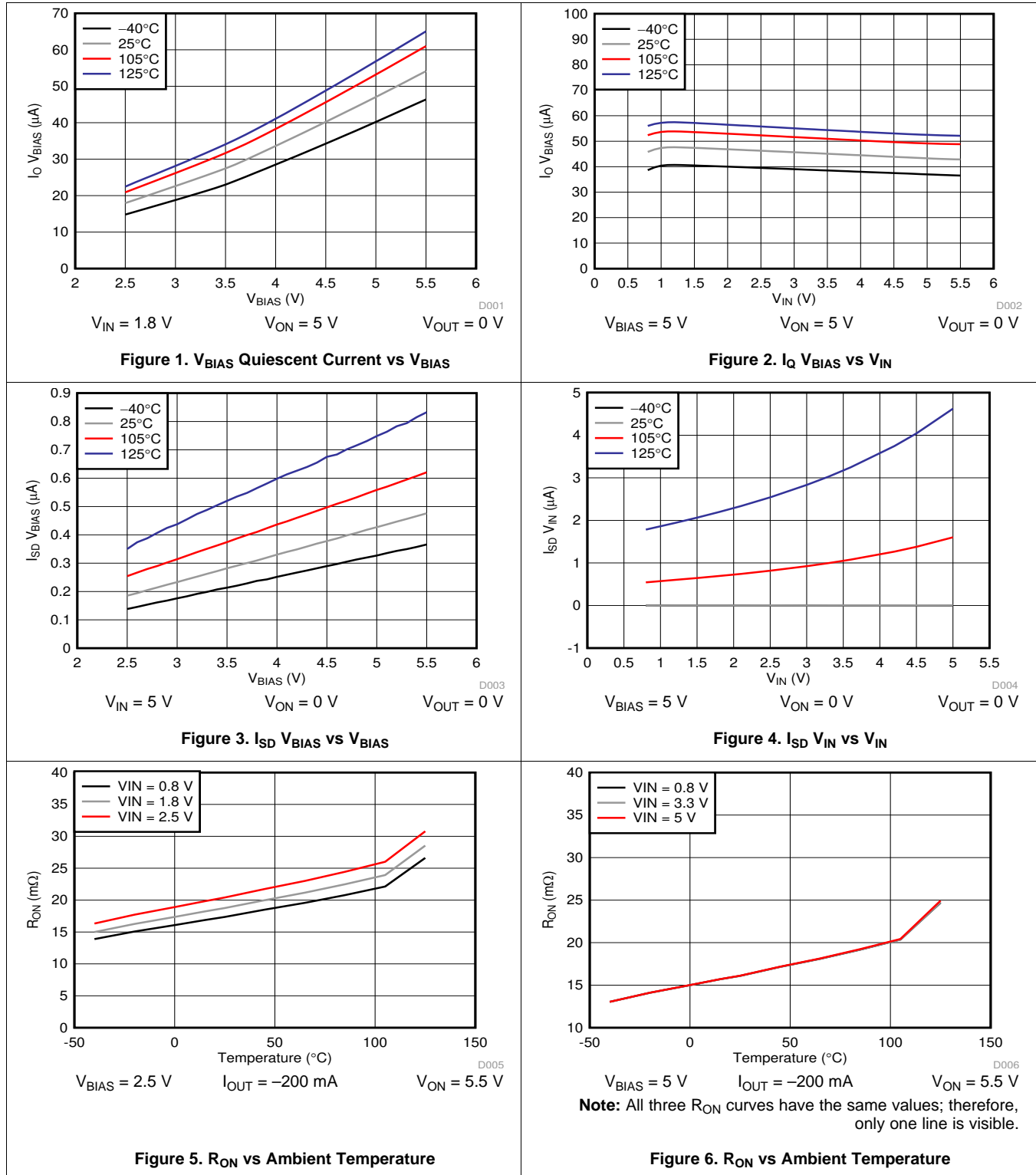
7.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). These switching characteristics are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1600		µs
t_{OFF}	Turnoff time			9		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1985		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		3		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		660		µs
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		730		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		100		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		380		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		8		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		560		µs
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		2435		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		9		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		2515		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		4		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1230		µs
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1565		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		70		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		930		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		8		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1110		µs

7.8 Typical Characteristics

7.8.1 Typical DC Characteristics

T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

Figure 1. V_{BIAS} Quiescent Current vs V_{BIAS}

V_{IN} = 1.8 V V_{ON} = 5 V V_{OUT} = 0 V

Figure 2. I_Q V_{BIAS} vs V_{IN}

V_{BIAS} = 5 V V_{ON} = 5 V V_{OUT} = 0 V

Figure 3. I_{SD} V_{BIAS} vs V_{BIAS}

V_{IN} = 5 V V_{ON} = 0 V V_{OUT} = 0 V

Figure 4. I_{SD} V_{IN} vs V_{IN}

V_{BIAS} = 5 V V_{ON} = 0 V V_{OUT} = 0 V

Figure 5. R_{ON} vs Ambient Temperature

V_{BIAS} = 2.5 V I_{OUT} = −200 mA V_{ON} = 5.5 V

Note: All three R_{ON} curves have the same values; therefore, only one line is visible.

Figure 6. R_{ON} vs Ambient Temperature

V_{BIAS} = 5 V I_{OUT} = −200 mA V_{ON} = 5.5 V

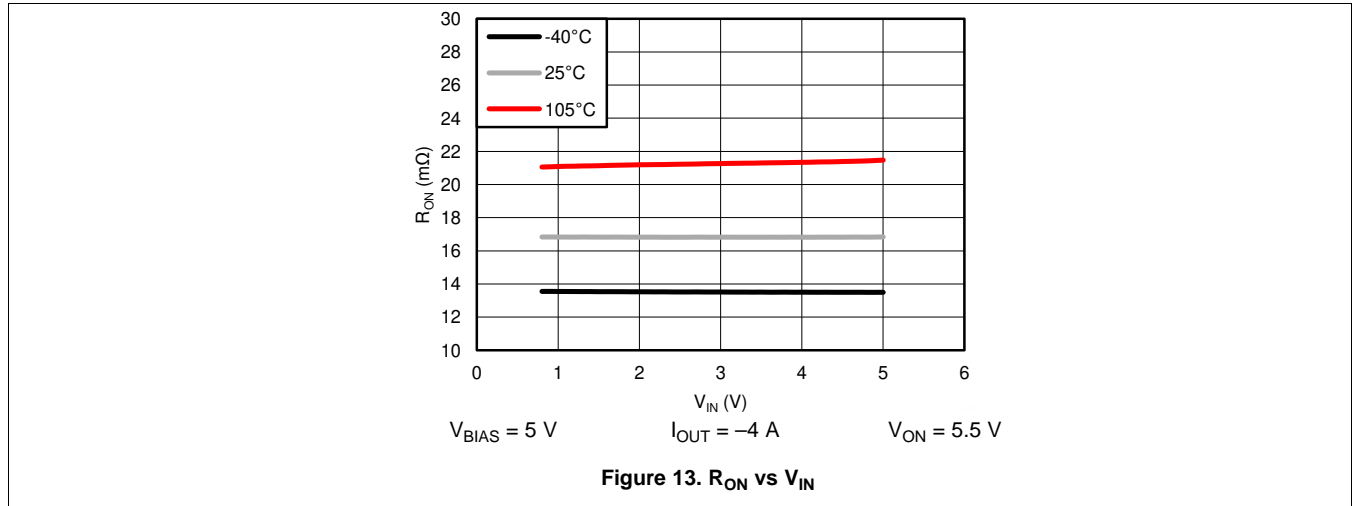Product Folder Links: *TPS22965-Q1*

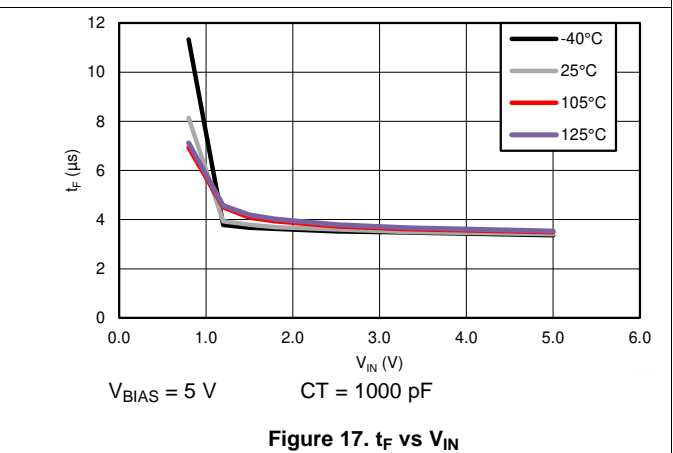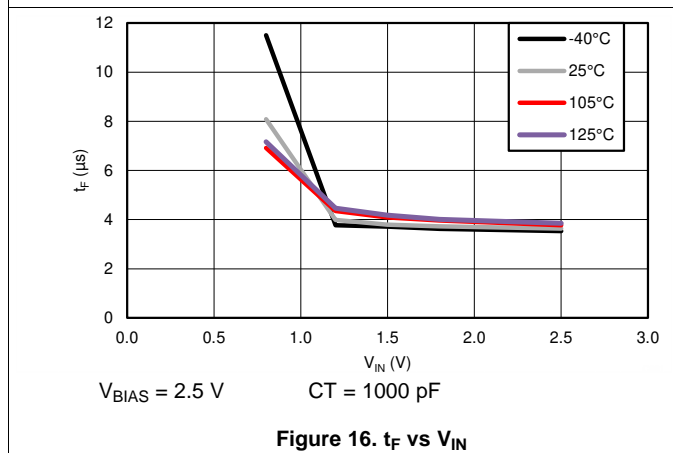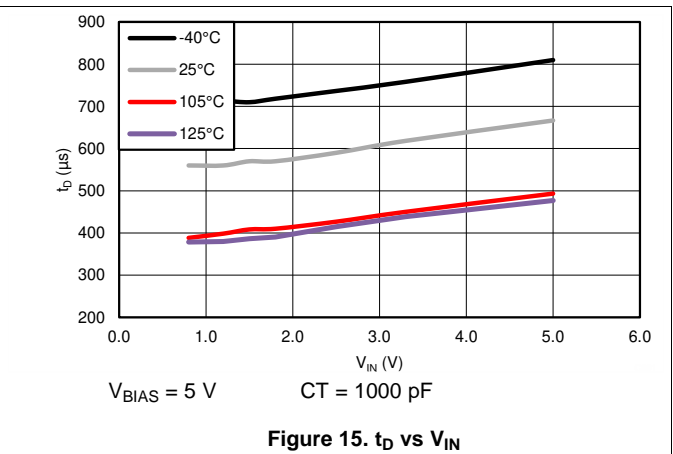## Typical DC Characteristics (continued)

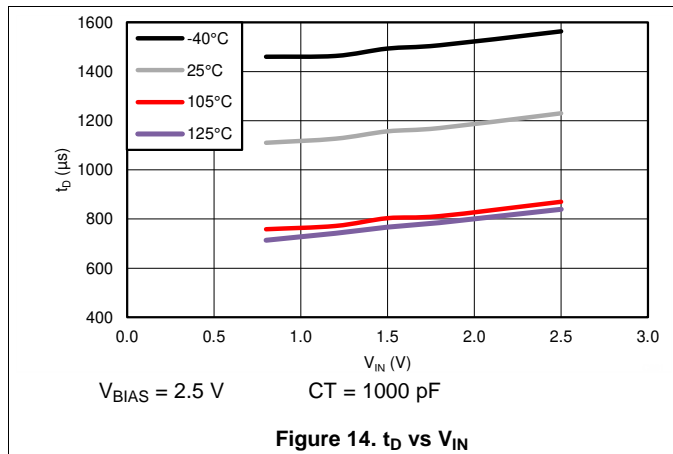T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

Figure 7. R_{ON} vs V_{IN}

V_{BIAS} = 2.5 V I_{OUT} = −200 mA V_{ON} = 5.5 V

Figure 8. R_{ON} vs V_{IN}

V_{BIAS} = 5 V I_{OUT} = −200 mA V_{ON} = 5.5 V

Figure 9. R_{ON} vs V_{BIAS}

T_A = 25°C I_{OUT} = −200 mA V_{ON} = 5.5 V

Figure 10. R_{PD} vs V_{BIAS}

V_{IN} = 1.8 V V_{ON} = 0 V

Figure 11. V_{OUT} vs V_{ON}

V_{IN} = 2 V T_A = 25°C

Figure 12. R_{ON} vs V_{IN}

V_{BIAS} = 2.5 V I_{OUT} = −4 A V_{ON} = 5.5 V

Typical DC Characteristics (continued)

T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

V_{BIAS} = 5 V I_{OUT} = −4 A V_{ON} = 5.5 V

Figure 13. R_{ON} vs V_{IN}

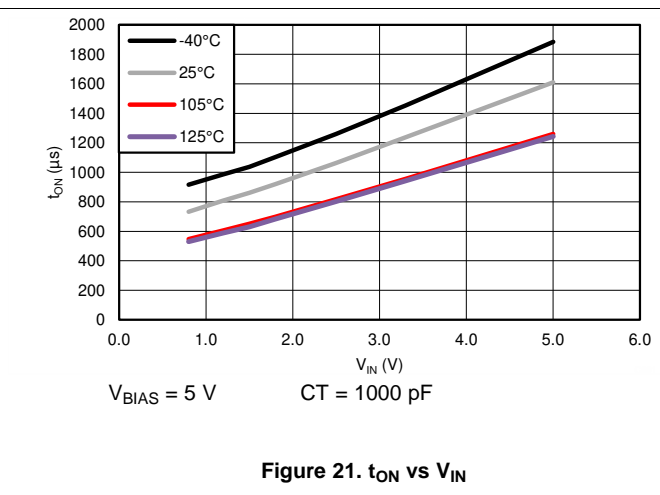### 7.8.2 Typical Switching Characteristics

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

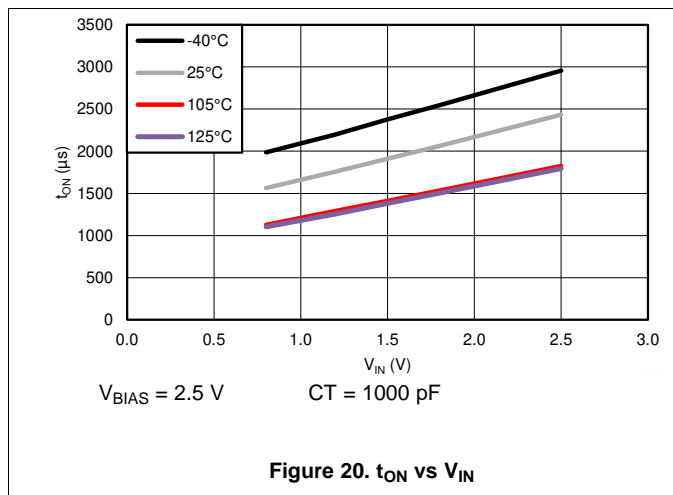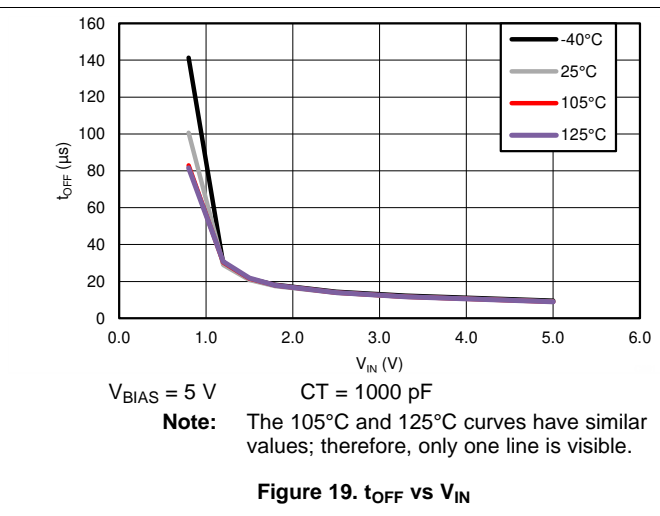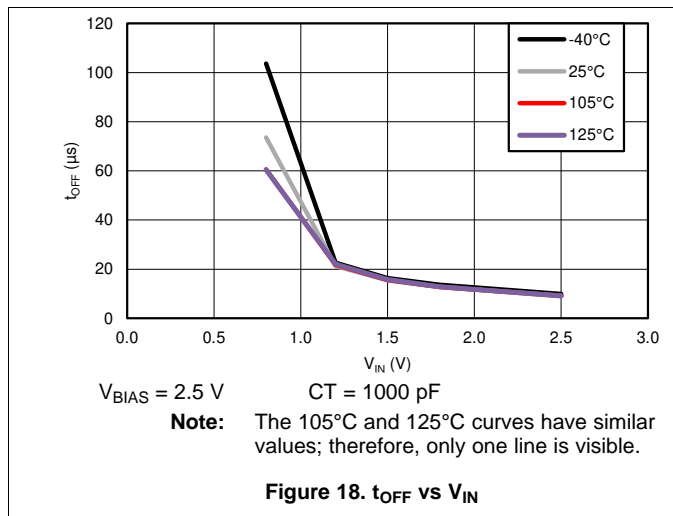V_{BIAS} = 2.5 V   CT = 1000 pF

Figure 14. t_D vs V_{IN}

V_{BIAS} = 5 V   CT = 1000 pF

Figure 15. t_D vs V_{IN}

V_{BIAS} = 2.5 V   CT = 1000 pF

Figure 16. t_F vs V_{IN}

V_{BIAS} = 5 V   CT = 1000 pF

Figure 17. t_F vs V_{IN}

Product Folder Links: *TPS22965-Q1*

Typical Switching Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.
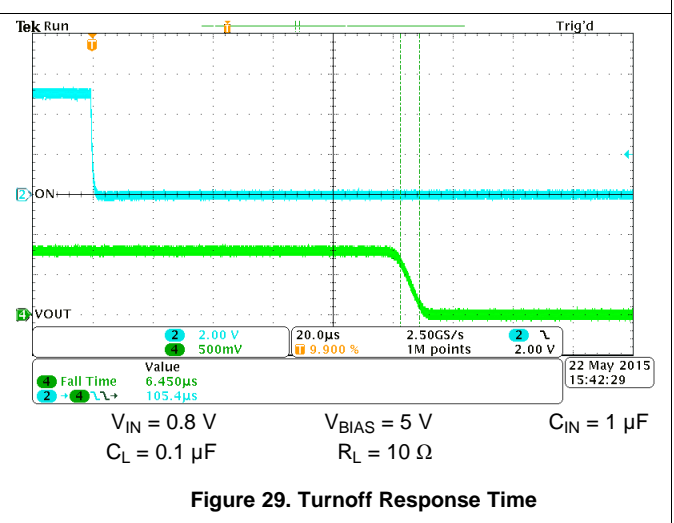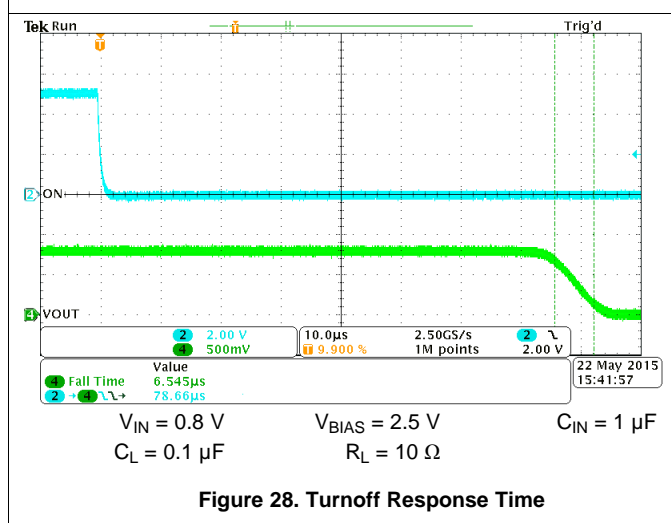

V_{BIAS} = 2.5 V   CT = 1000 pF
Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

Figure 18. t_{OFF} vs V_{IN}

V_{BIAS} = 5 V   CT = 1000 pF
Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

Figure 19. t_{OFF} vs V_{IN}

V_{BIAS} = 2.5 V   CT = 1000 pF

Figure 20. t_{ON} vs V_{IN}

V_{BIAS} = 5 V   CT = 1000 pF

Figure 21. t_{ON} vs V_{IN}

V_{BIAS} = 2.5 V   CT = 1000 pF
Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

Figure 22. t_R vs V_{IN}

V_{BIAS} = 5 V   CT = 1000 pF
Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

Figure 23. t_R vs V_{IN}

Typical Switching Characteristics (continued)

$T_A = 25°C$, $C_T = 1000$ pF, $C_{IN} = 1$ µF, $C_L = 0.1$ µF, $R_L = 10$ Ω (unless otherwise specified). $T_A = 125°C$ data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.
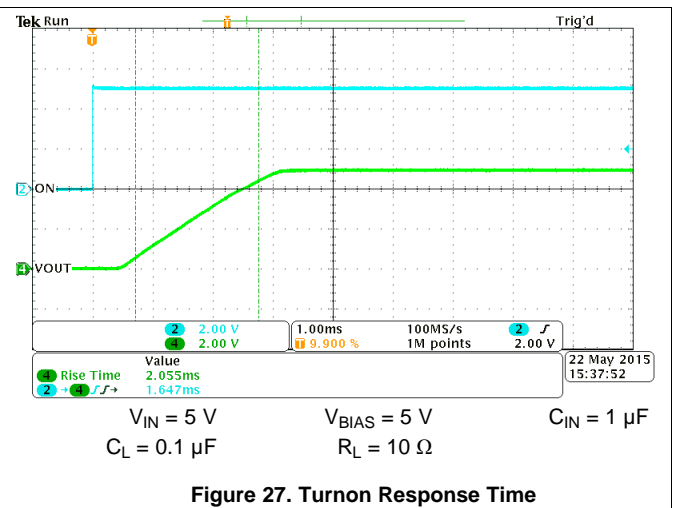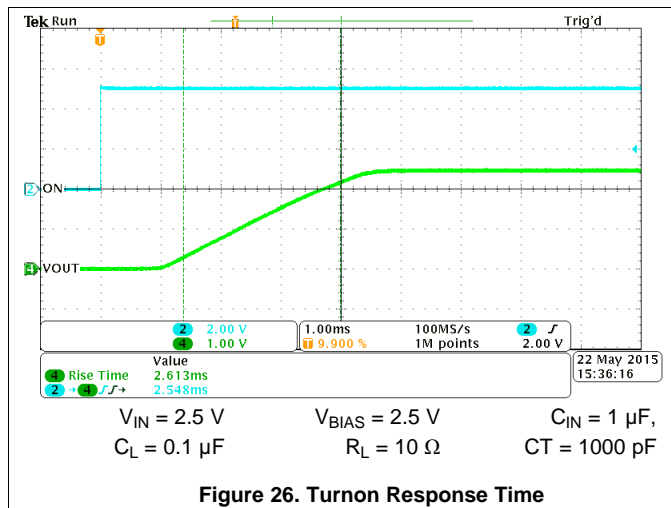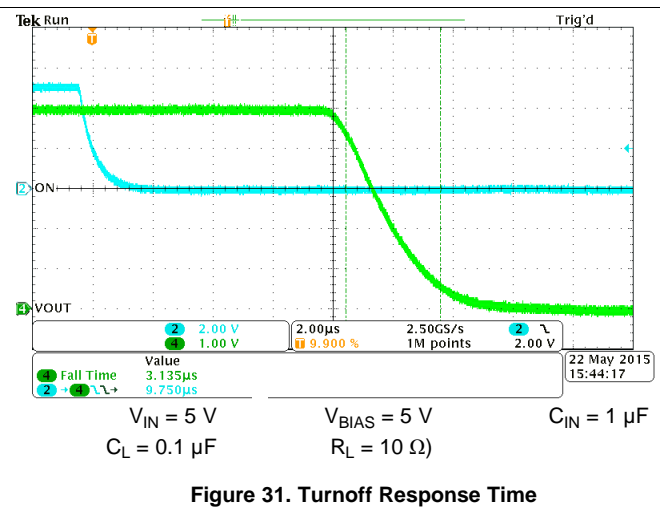

$V_{IN} = 0.8$ V $V_{BIAS} = 2.5$ V $C_{IN} = 1$ µF

$C_L = 0.1$ µF $R_L = 10$ Ω   CT = 1000 pF

Figure 24. Turnon Response Time

$V_{IN} = 0.8$ V $V_{BIAS} = 5$ V $C_{IN} = 1$ µF

$C_L = 0.1$ µF $R_L = 10$ Ω   CT = 1000 pF

Figure 25. Turnon Response Time

$V_{IN} = 2.5$ V $V_{BIAS} = 2.5$ V $C_{IN} = 1$ µF,

$C_L = 0.1$ µF $R_L = 10$ Ω   CT = 1000 pF

Figure 26. Turnon Response Time

$V_{IN} = 5$ V $V_{BIAS} = 5$ V $C_{IN} = 1$ µF

$C_L = 0.1$ µF $R_L = 10$ Ω

Figure 27. Turnon Response Time

$V_{IN} = 0.8$ V $V_{BIAS} = 2.5$ V $C_{IN} = 1$ µF

$C_L = 0.1$ µF $R_L = 10$ Ω

Figure 28. Turnoff Response Time

$V_{IN} = 0.8$ V $V_{BIAS} = 5$ V $C_{IN} = 1$ µF

$C_L = 0.1$ µF $R_L = 10$ Ω

Figure 29. Turnoff Response Time

Product Folder Links: TPS22965-Q1

Typical Switching Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

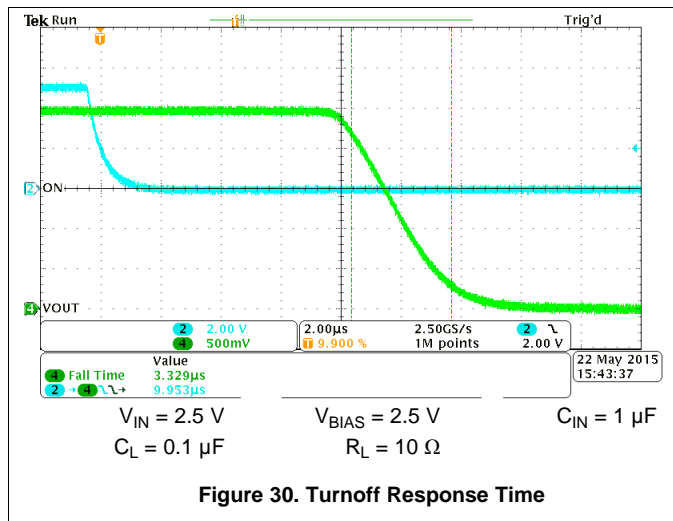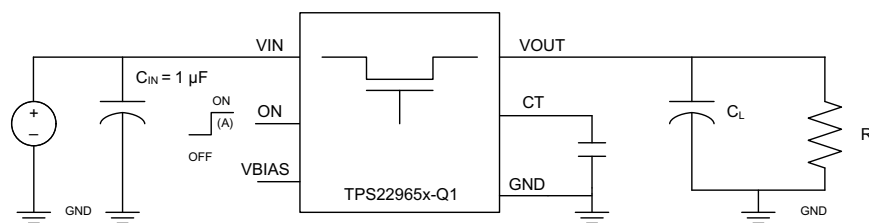V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF

C_L = 0.1 µF R_L = 10 Ω

Figure 30. Turnoff Response Time

V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF

C_L = 0.1 µF R_L = 10 Ω)

Figure 31. Turnoff Response Time

8   Parameter Measurement Information

A.   Rise and fall times of the control signal are 100 ns.
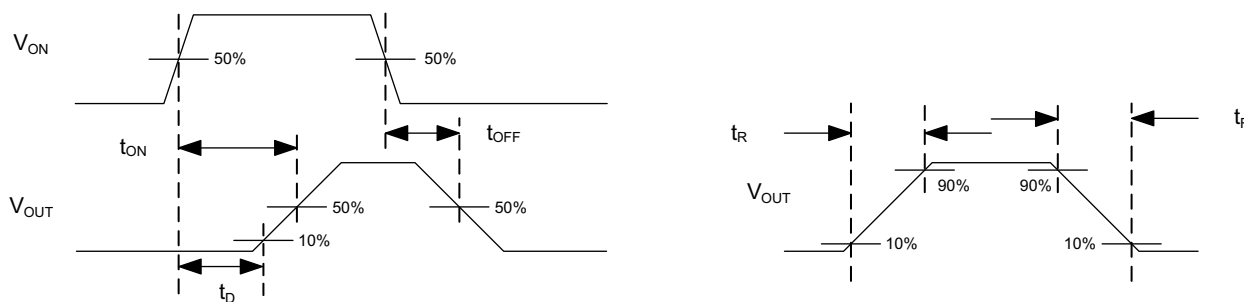
Figure 32. Test Circuit

**Figure 33. t_{ON} and t_{OFF} Waveforms**

9 Detailed Description

9.1 Overview

The TPS22965x-Q1 is a single channel, 4-A load switch in an 8-pin WSON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

9.2 Functional Block Diagram
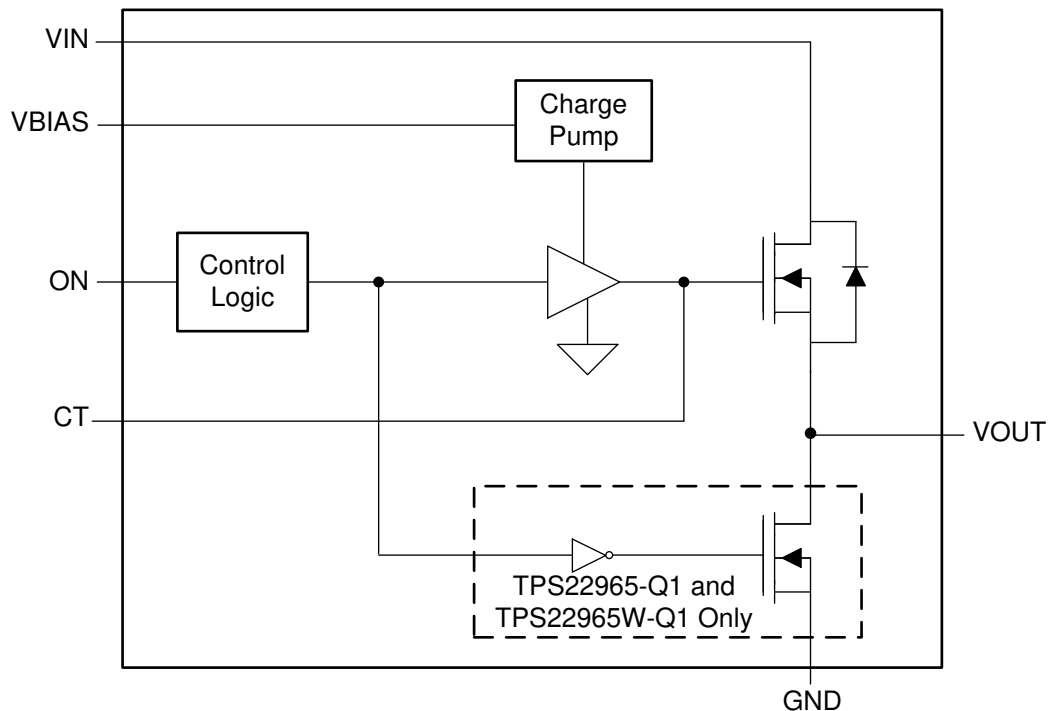
9.3 Feature Description

9.3.1 Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 12 V. Therefore, the minimum voltage rating for the CT cap must be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate when V_{BIAS} is set to 5 V is shown in Equation 1. This equation accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CT = 0 pF. Use Table 1 to determine rise times for when CT = 0 pF.

$$SR = 0.38 \times CT + 34$$

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 34 are µs/V. The units for the constant 0.38 are µs/(V × pF).   (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. The rise times listed in Table 1 are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON pin is asserted high.

Table 1. Rise Time vs CT Capacitor

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V [1]						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.8 V
0	180	136	94	84	74	70	60
220	547	378	232	202	173	157	129
470	962	654	386	333	282	252	206
1000	1983	1330	765	647	533	476	382
2200	4013	2693	1537	1310	1077	959	766
4700	8207	5490	3137	2693	2200	1970	1590
10000	17700	11767	6697	5683	4657	4151	3350

(1)   Typical Values at 25°C with a 25-V X7R 10% Ceramic Capacitor on CT

9.3.2 Quick Output Discharge (TPS22965-Q1 and TPS22965W-Q1 Only)

The TPS22965-Q1 and TPS22965W-Q1 include a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225 Ω and prevents the output from floating while the switch is disabled.

9.3.3 Low Power Consumption During Off State

The I_{SD} V_{IN} supply current is 0.01 µA typical at 1.8 V VIN. Typically, the downstream loads must have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

9.4 Device Functional Modes

Table 2 lists the VOUT pin state as determined by the ON pin.

Table 2. Functional Table

ON	TPS22965N-Q1 AND TPS22965NW-Q1	TPS22965-Q1 AND TPS22965W-Q1
L	Open	GND
H	VIN	VIN

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

10.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics—V_{BIAS} = 2.5 V* table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 2 to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination   (2)

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.1.2 On and Off Control

The ON pin controls the state of the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.1.3 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

10.1.4 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

10.1.5 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics—V_{BIAS} = 2.5 V* table. See Figure 34 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

Application Information (continued)
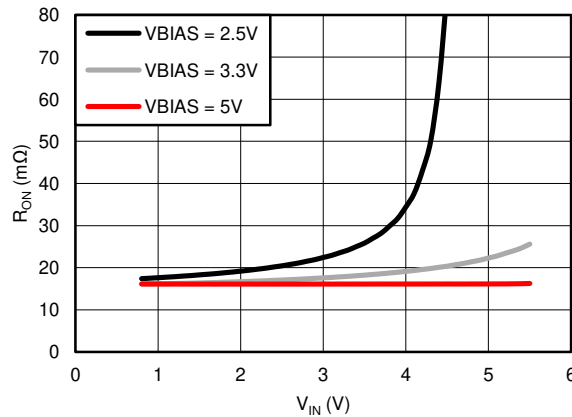
$I_{OUT} = -200mA$ $T_A = 25°C$

Figure 34. R_{ON} vs. V_{IN} ($V_{IN} > V_{BIAS}$)

10.2 Typical Application

This application demonstrates how the TPS22965x-Q1 can be used to power downstream modules.
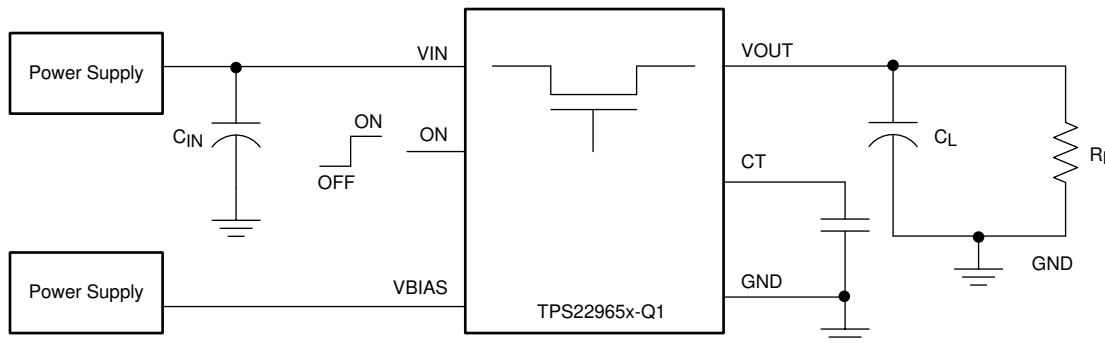

Figure 35. Schematic for Powering a Downstream Module

10.2.1 Design Requirements

Use the values listed in Table 3 as the design parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum Acceptable Inrush Current	400 mA

Product Folder Links: *TPS22965-Q1*

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 3.

Inrush Current = C × dV/dt

where

- C = output capacitance
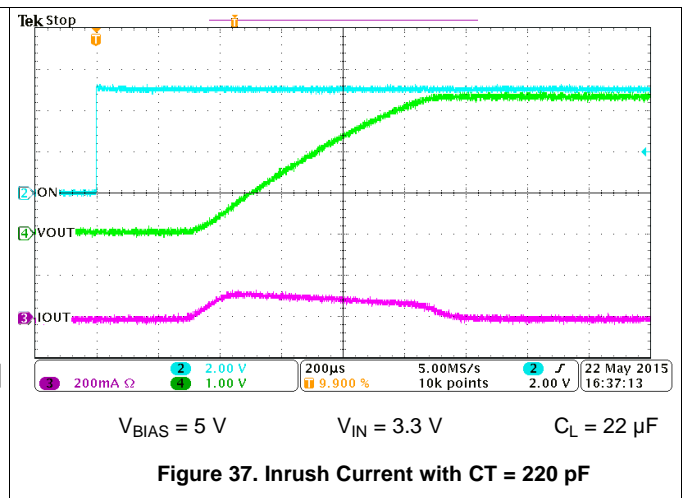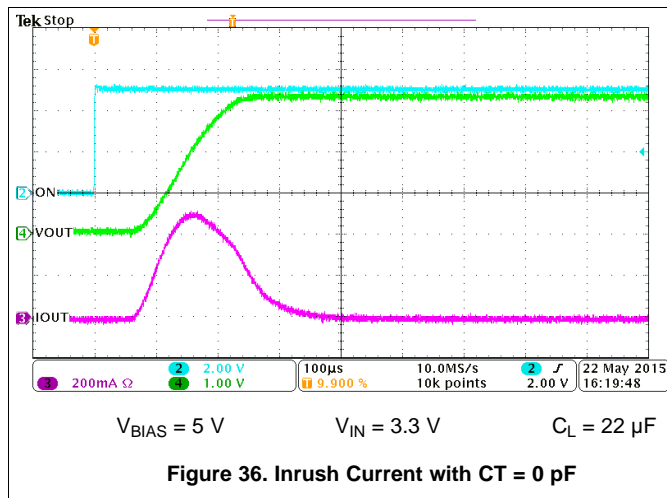- dV = output voltage
- dt = rise time (3)

The TPS22965x-Q1 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation. See Equation 4 and Equation 5.

400 mA = 22 µF × 3.3 V / dt (4)

dt = 181.5 µs (5)

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.3 Application Curves

V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 36. Inrush Current with CT = 0 pF

V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 37. Inrush Current with CT = 220 pF

Product Folder Links: *TPS22965-Q1*

11 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.5 V and a VIN range of 0.8 V to VBIAS.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to avoid parasitic capacitance.

12.2 Layout Example

(1) Thermal relief vias. Thermal relief vias connected to the exposed thermal pad

Figure 38. Layout Recommendation

12.3 Thermal Consideration

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 6 as a guideline.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}}$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22965x-Q1)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See the *Thermal Information* table. This parameter is highly dependent upon board layout   (6)

Refer to Figure 38, notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:
- *Load Switches: What Are They, Why Do You Need Them And How Do You Choose The Right One?*
- *Load Switch Thermal Considerations*
- *Managing Inrush Current*
- *TPS22965WDSGQ1EVM 5.7-V, 4-A, 16-mΩ On-Resistance Load Switch*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.
   This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22965NQWDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	11B	Samples
TPS22965NQWDSGTQ1	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	11B	Samples
TPS22965NTDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZDXI	Samples
TPS22965NTDSGTQ1	PREVIEW	WSON	DSG	8	250	TBD	Call TI	Call TI	-40 to 105		
TPS22965QWDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	11A	Samples
TPS22965QWDSGTQ1	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	11A	Samples
TPS22965TDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZYE	Samples
TPS22965TDSGTQ1	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZYE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22965-Q1 :

• Catalog: TPS22965

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

![Texas Instruments logo]

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22965NQWDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965NQWDSGTQ1	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965NTDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965QWDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965QWDSGTQ1	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965TDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965TDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22965NQWDSGRQ1	WSON	DSG	8	3000	195.0	200.0	45.0
TPS22965NQWDSGTQ1	WSON	DSG	8	250	195.0	200.0	45.0
TPS22965NTDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965QWDSGRQ1	WSON	DSG	8	3000	195.0	200.0	45.0
TPS22965QWDSGTQ1	WSON	DSG	8	250	195.0	200.0	45.0
TPS22965TDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965TDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0

DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224783/A

A | B

2.1
1.9

PIN 1 INDEX AREA

2.1
1.9

0.1 MIN

(0.05)

SECTION A-A
TYPICAL

0.3
0.2

0.4
0.2

OPTIONAL TERMINAL
TYPICAL

0.8 MAX

0.05
0.00

C

SEATING PLANE

0.08 | C

EXPOSED
THERMAL PAD

0.9± 0.1

4

5

6X | 0.5

A | A

2X
1.5

9

1.6± 0.1

1

8

SEE OPTIONAL
TERMINAL

PIN 1 ID
(OPTIONAL)

8X 0.3
0.2

8X 0.4
0.2

(0.2) TYP

⊕ | 0.1 Ⓜ | C | A | B
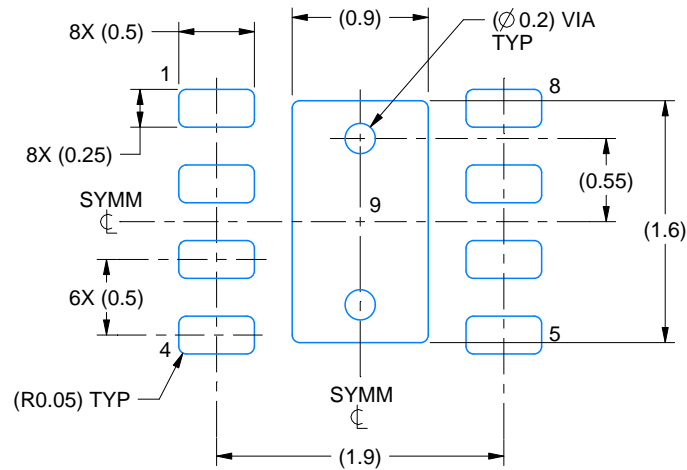0.05 Ⓜ | C
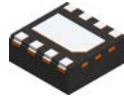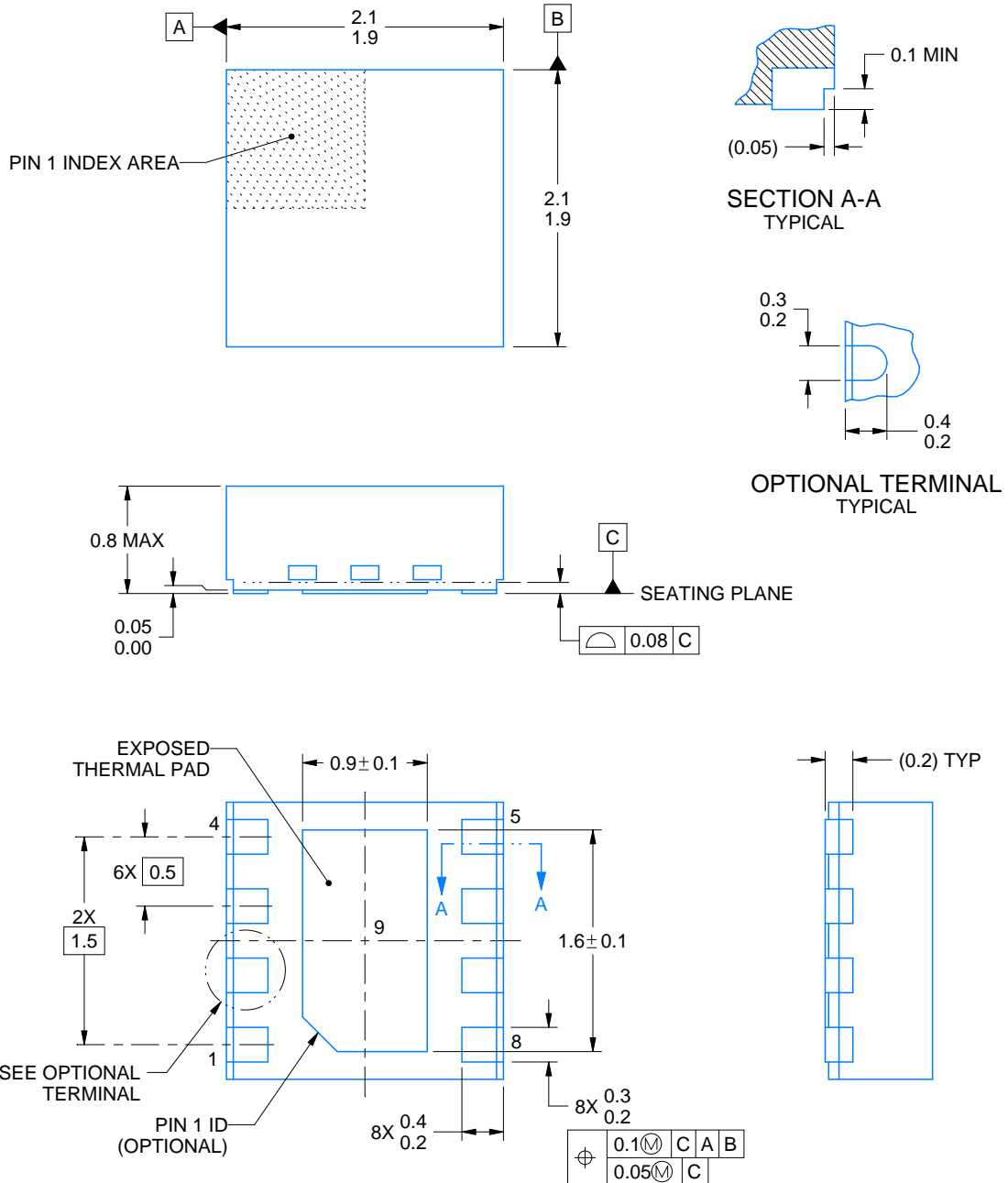
4222124/D   12/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
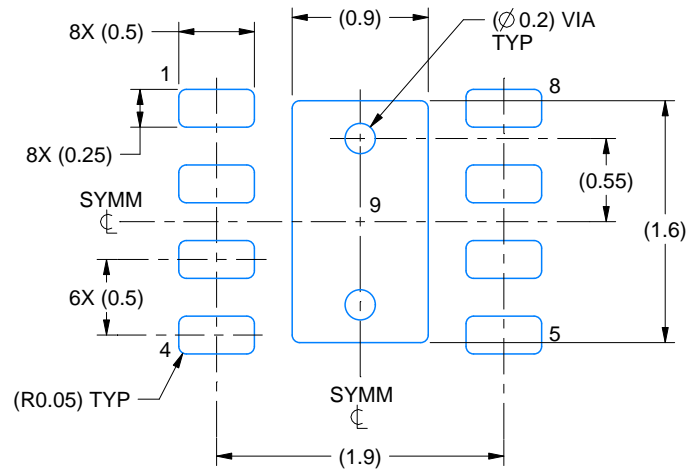
LAND PATTERN EXAMPLE
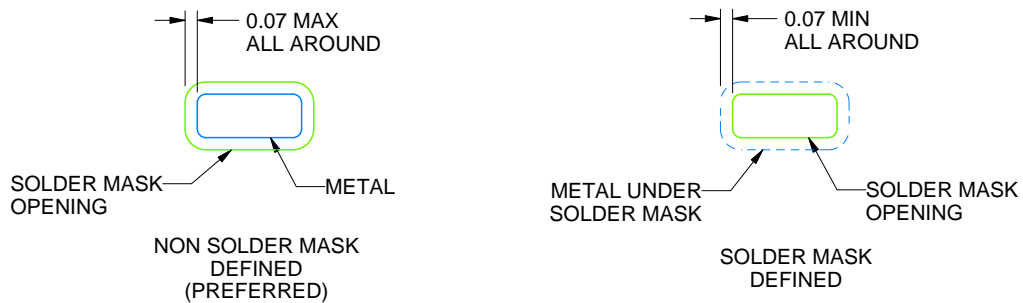EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED
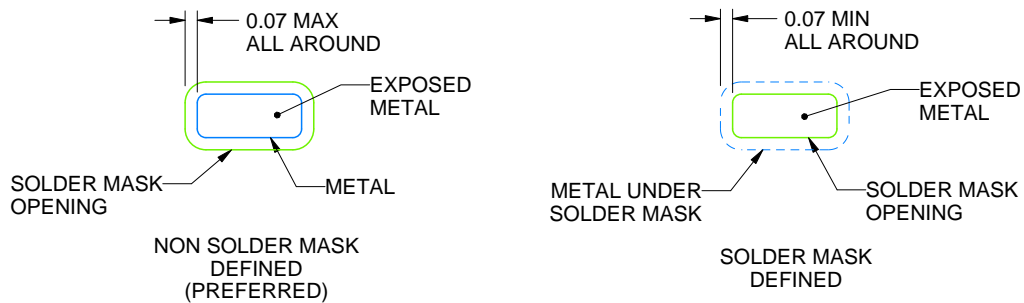
SOLDER MASK DETAILS

4222124/D   12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

8X (0.5)

SYMM

METAL

1

8X (0.25)

8

SYMM

(0.45)

9

6X (0.5)

(0.7)

4

5

(R0.05) TYP

(0.9)

(1.9)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/D   12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

A

2.1
1.9

B

PIN 1 INDEX AREA

2.1
1.9

0.32
0.18

0.4
0.2

OPTIONAL TERMINAL
TYPICAL

0.8 MAX

C

SEATING PLANE

0.05
0.00

◯ 0.08 C

EXPOSED
THERMAL PAD

0.9 ± 0.1

4

5

6X 0.5

2X
1.5

9

1.6 ± 0.1

8

SEE OPTIONAL
TERMINAL

1

(0.2) TYP

PIN 1 ID

8X 0.4
0.2

8X 0.32
0.18

⊕	0.1 Ⓜ	C	A	B
	0.05 Ⓜ	C		

4218900/C   04/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

8X (0.5)

(0.9)

($\varnothing$ 0.2) VIA
TYP

1

8

8X (0.25)

SYMM
℄

9

(0.55)

(1.6)

6X (0.5)

4

5

(R0.05) TYP

SYMM
℄

(1.9)

LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/C   04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

8X (0.5)

1

8X (0.25)

SYMM

6X (0.5)

4

(R0.05) TYP

SYMM

METAL

8

(0.45)

9

(0.7)

5

(0.9)

(1.9)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/C 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.