

## HIGH SPEED POWER DRIVER

 Check for Samples: [UC1705](#), [UC2705](#), [UC3705](#)

### FEATURES

- 1.5 A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise Fall into 1000 pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5 V to 40 V Operation
- Thermal Shutdown Protection
- Minidip and Power Packages

### DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 A may be switched in either direction. With both inverting and non-inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both  $V_S$  and  $V_C$  can independently range from 5 V to 40 V. For additional application details, see the UC1707/3707 data sheet ([SLUS177](#)).

The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to 125°C operation. The UC3705 is specified for a temperature range of 0°C to 70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

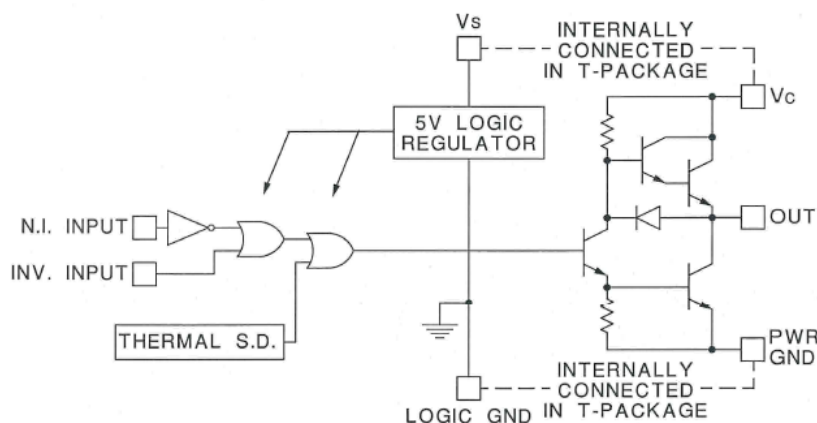
**TRUTH TABLE<sup>(1)(2)</sup>**

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

 (1)  $\overline{OUT} = \overline{INV}$  and N.I.

 (2)  $\overline{OUT} = INV$  and N.i.

### BLOCK DIAGRAM



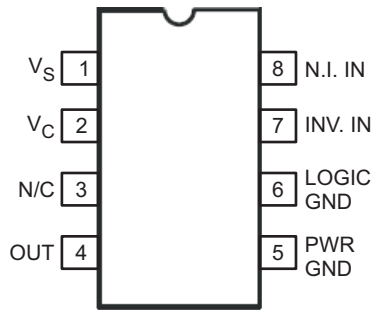
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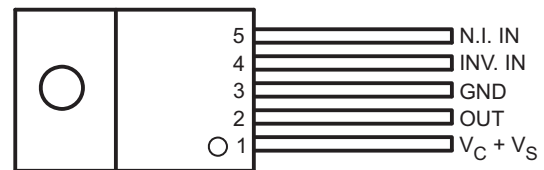
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### CONNECTION DIAGRAMS

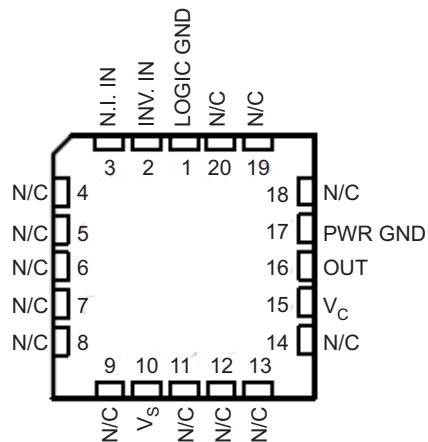
**DIL-8 MINIDIP, SOIC-8  
(TOP VIEW)  
N, JG OR D PACKAGE**



**5-PIN TO-220  
(TOP VIEW)  
T PACKAGE**



**LCCC-20  
(TOP VIEW)  
FK PACKAGE**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

	VALUE			UNIT
	N-Pkg	JG-Pkg	T-Pkg	
Supply Voltage ( $V_{IN}$ )	40	40	40	V
Collector Supply Voltage, $V_C$	40	40	40	
Output current (source or sink)				
Steady-State	±500	±500	±1	A
Peak Transient	±1.5	±1	±2	A
Capacitive Discharge Energy	20	15	50	μJ
Digital Inputs <sup>(2)</sup>	5.5	5.5	5.5	V
Power Dissipation at $T_A = 25^\circ\text{C}$ <sup>(1)</sup>	1	1	3	W
Power Dissipation at $T_A$ (Lead/Case) = $25^\circ\text{C}$ <sup>(1)</sup>	3	2	25	W
Operating Temperature Range	0 to 70	-55 to 125	0 to 70	°C
Storage temperature	-65 to 150	-65 to 150	-65 to 150	°C

(1) All currents are positive into, negative out of the specified terminal.

(2) Digital Drive can exceed 5.5 V if the input current is limited to 10 mA

**ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1705,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2707, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3705;  $V_{IN} = V_C = 20\text{ V}$ .  $T_A = T_J$ .

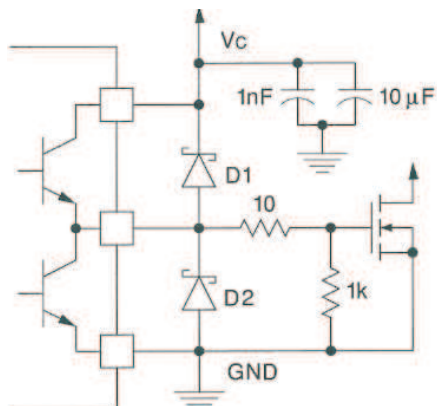
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_S$	Supply current	$V_S = 40\text{ V}$ , outputs high, T package		6	8	mA
		$V_C = 40\text{ V}$ , outputs low, T package		6	12	mA
$V_C$	Supply current (N, JG Only)	$V_C = 40\text{ V}$ , outputs low		2	4	mA
$V_C$	Leakage current (N, JG Only)	$V_S = 0$ , $V_C = 30\text{ V}$		0.05	0.1	mA
	Digital input low level				0.8	V
	Digital input high level		2.2			V
	Input current	$V_I = 0$		-0.6	-1	mA
	Input leakage	$V_I = 5\text{ V}$		0.05	0.1	mA
$V_C - V_O$	Output high saturation	$I_O = -50\text{ mA}$			2	V
		$I_O = -500\text{ mA}$			2.5	
$V_O$	Output low saturation	$I_O = -50\text{ mA}$			0.4	V
		$I_O = -500\text{ mA}$			2.5	
	Thermal shutdown			155		°C

## TYPICAL SWITCHING CHARACTERISTICS

$V_{IN} = V_C = 20\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . Delays measured to 10% output change.

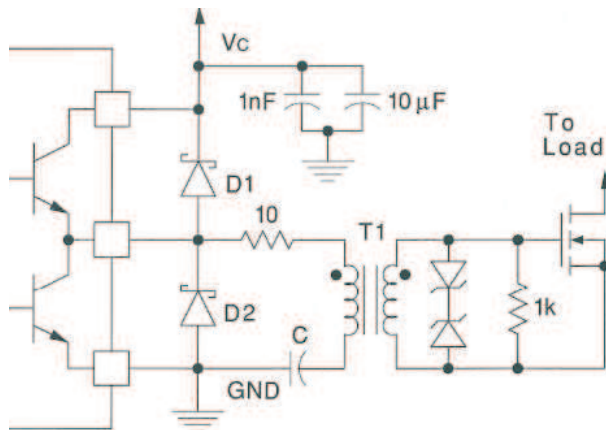
PARAMETER	TEST CONDITIONS	OUTPUT CL =			UNIT
<b>From Inv. Input to Output</b>		open	1	2.2	nF
Rise time delay		60	60	60	ns
10% to 90% rise		20	40	60	ns
Fall time delay		60	60	60	ns
90% to 10% fall		25	40	50	ns
<b>From N.I. Input to Output</b>					
Rise time delay		90	90	90	ns
10% to 90% rise		20	40	60	ns
Fall time delay		60	60	60	ns
90% to 10% fall		25	40	50	ns
$V_C$ cross-conduction current spike duration	Output rise	25			ns
	Output fall	0			ns

APPLICATION INFORMATION



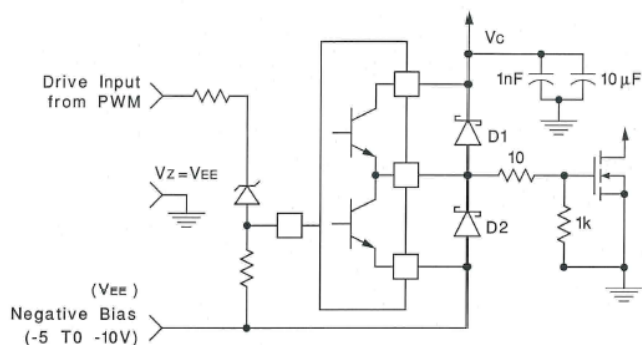
D1, D2: UC3611 Schottky Diodes

Figure 1. Power MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Figure 3. Transformer Coupled MOSFET DRIVE Circuit



D1, D2: UC3611 Schottky Diodes

Figure 2. Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs

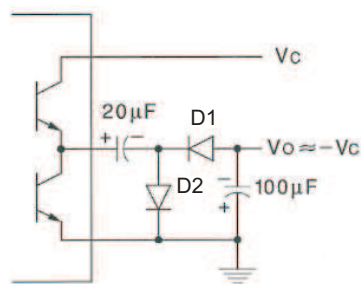
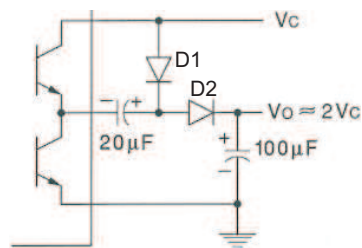


Figure 4. Charge Pump Circuit

## REVISION HISTORY

Changes from Revision C (December, 2011) to Revision D	Page
• Deleted SN54BCT373 from title for FK package image .....	<a href="#">2</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9579801M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9579801M2A UC1705L/ 883B	<a href="#">Samples</a>
5962-9579801MPA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	9579801MPA UC1705	<a href="#">Samples</a>
5962-9579801VPA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	9579801VPA UC1705	<a href="#">Samples</a>
UC1705J	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	UC1705J	<a href="#">Samples</a>
UC1705J883B	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	9579801MPA UC1705	<a href="#">Samples</a>
UC1705L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9579801M2A UC1705L/ 883B	<a href="#">Samples</a>
UC2705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2705D	<a href="#">Samples</a>
UC2705DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2705D	<a href="#">Samples</a>
UC2705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2705N	<a href="#">Samples</a>
UC3705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3705D	<a href="#">Samples</a>
UC3705DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3705D	<a href="#">Samples</a>
UC3705J	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	0 to 70	UC3705J	<a href="#">Samples</a>
UC3705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3705N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UC1705, UC1705-SP, UC3705, UC3705M :**

- Catalog: [UC3705](#), [UC1705](#), [UC3705M](#), [UC3705](#)
- Military: [UC1705](#), [UC1705](#)
- Space: [UC1705-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3705DTR	SOIC	D	8	2500	367.0	367.0	35.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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