

CD4514B, CD4515B Types

CMOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)
CD4514B Output "High" on Select
CD4515B Output "Low" on Select

■ CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0 (CD4514B) or 1 (CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are similar to industry types MC14514 and MC14515.

The CD4514B and CD4515B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), and 16-lead small-outline packages (M and M96 suffixes).

Features:

- Strobed input latch
- Inhibit control
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics.
- Meets all requirements of JEDEC Tentative Standard No. 13B; "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding
- Program-counter decoding
- Control decoder

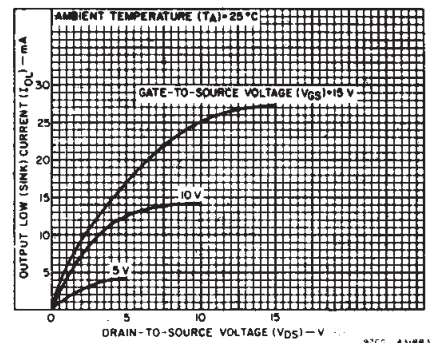
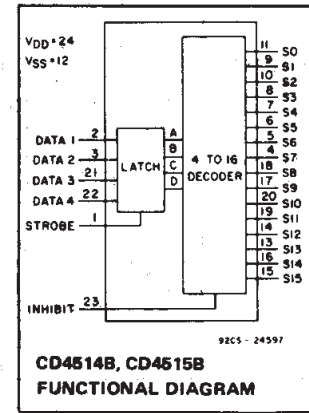


Fig. 1 – Typical output low (sink) current characteristics.

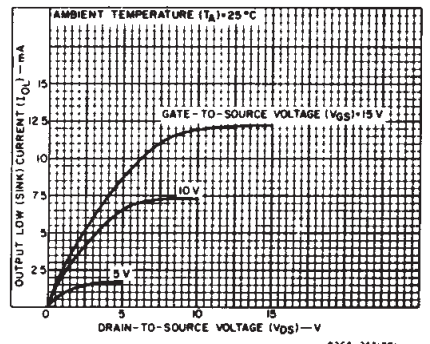


Fig. 2 – Minimum output low (sink) current characteristics.

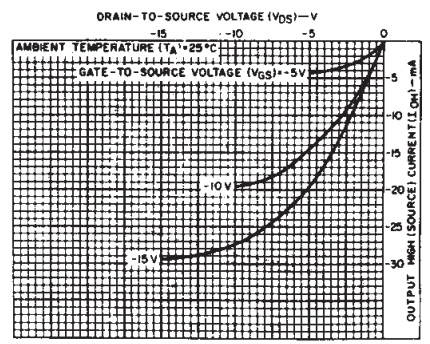


Fig. 3 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	-55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max	$+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	150 70 40	— — —	ns
Strobe Pulse Width, t_W	5 10 15	250 100 75	— — —	ns

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4514B, CD4515B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0.5	5	5	5	150	150	-	0.04	5	μA
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0.5	5	0.05			-	0	0.05	-	V
	-	0.10	10	0.05			-	0	0.05	-	
	-	0.15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, V _{OH} Min.	-	0.5	5	4.95			-	4.95	5	-	V
	-	0.10	10	9.95			-	9.95	10	-	
	-	0.15	15	14.95			-	14.95	15	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5			-	-	1.5	-	V
	1, 9	-	10	3			-	-	3	-	
	1.5, 13.5	-	15	4			-	-	4	-	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5			-	3.5	-	-	V
	1, 9	-	10	7			-	7	-	-	
	1.5, 13.5	-	15	11			-	11	-	-	
Input Current I _{IN} Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

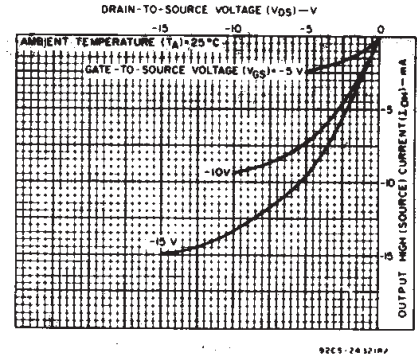


Fig. 4 - Minimum output high (source) current characteristics.

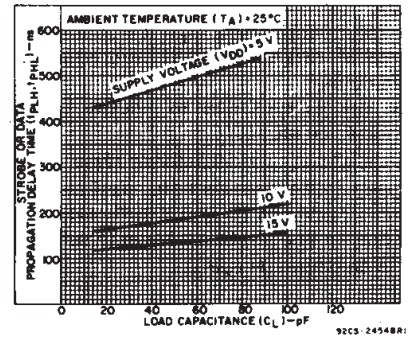


Fig. 5 - Typical strobe or data propagation delay time vs. load capacitance.

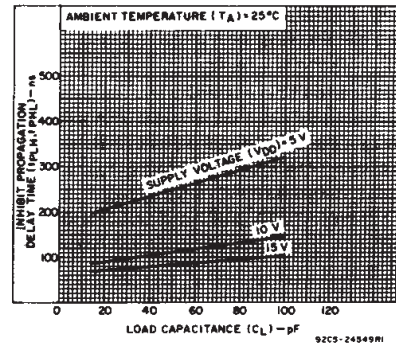


Fig. 6 - Typical inhibit propagation delay time vs. load capacitance.

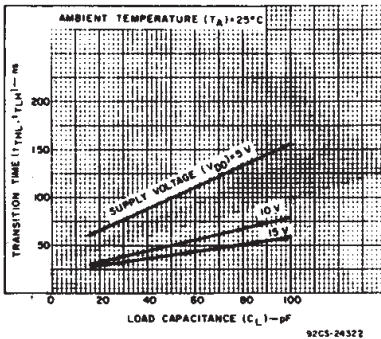


Fig. 7 - Typical low-to-high transition time vs. load capacitance.

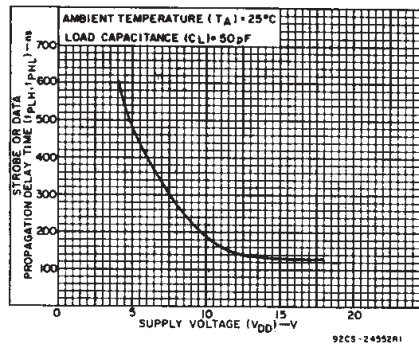


Fig. 8 - Typical strobe or data propagation delay time vs. supply voltage.

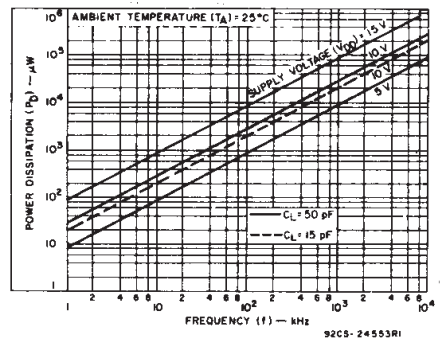


Fig. 9 - Typical power dissipation vs. frequency.

CD4514B, CD4515B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		VDD V	Typ.	Max.	
Propagation Delay Time: t_{PHL} , t_{PLH} Strobe or Data		5	485	970	ns
		10	185	370	
		15	135	270	
Inhibit		5	250	500	ns
		10	110	220	
		15	85	170	
Transition Time, t_{TLH} , t_{THL}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Strobe Pulse Width, t_W		5	125	250	ns
		10	50	100	
		15	40	75	
Minimum Data Setup Time, t_S		5	75	150	ns
		10	35	70	
		15	20	40	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

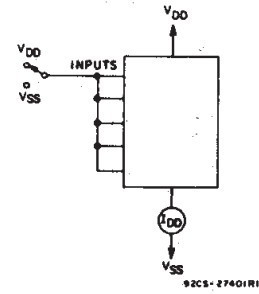


Fig. 10 — Quiescent device current test circuit.

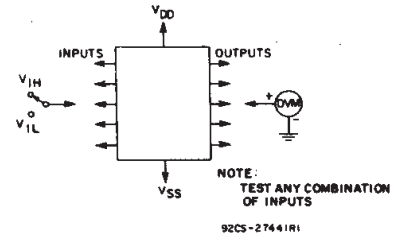


Fig. 11 — Input voltage test circuit.

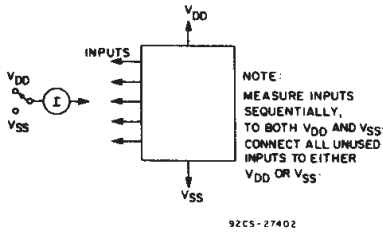


Fig. 12 — Input current test circuit.

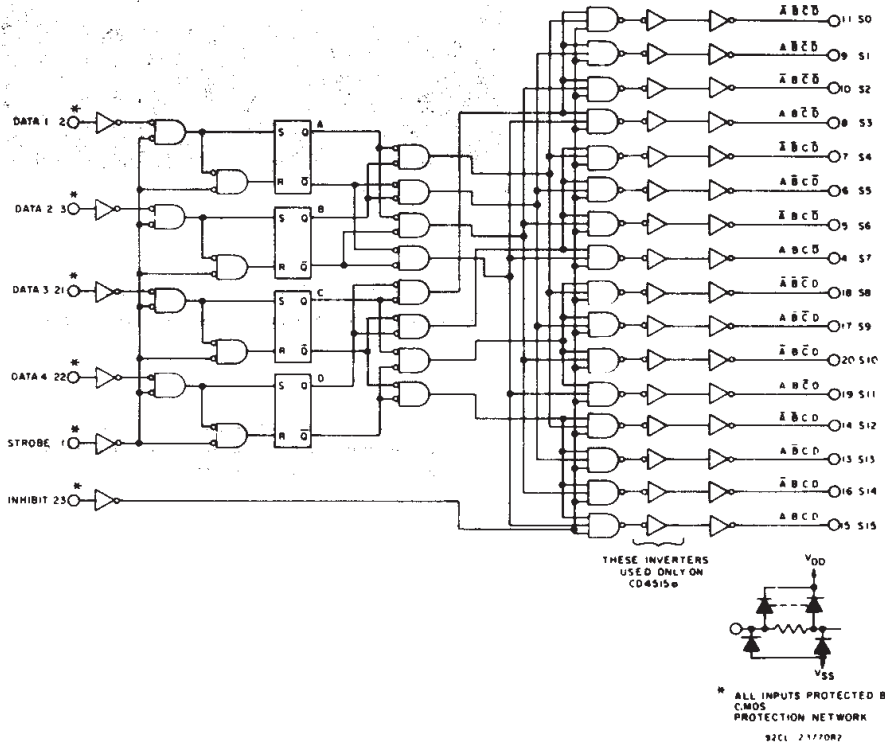


Fig. 13 — Logic diagram for CD4514B and CD4515B.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4514B, CD4515B Types

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT	
	D	C	B	A	CD4514B = Logic 1 (High)	CD4515B = Logic 0 (Low)
0	0	0	0	0	S0	
0	0	0	0	1	S1	
0	0	0	1	0	S2	
0	0	0	1	1	S3	
0	0	1	0	0	S4	
0	0	1	0	1	S5	
0	0	1	1	0	S6	
0	0	1	1	1	S7	
0	1	0	0	0	S8	
0	1	0	0	1	S9	
0	1	0	1	0	S10	
0	1	0	1	1	S11	
0	1	1	0	0	S12	
0	1	1	0	1	S13	
0	1	1	1	0	S14	
0	1	1	1	1	S15	
1	X	X	X	X	All Outputs = 0, CD4514B	All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low

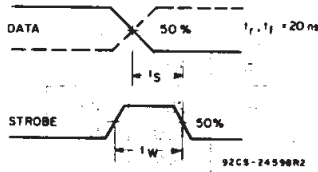
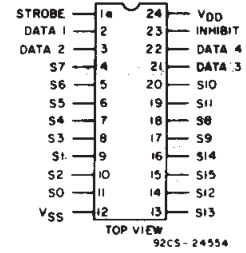
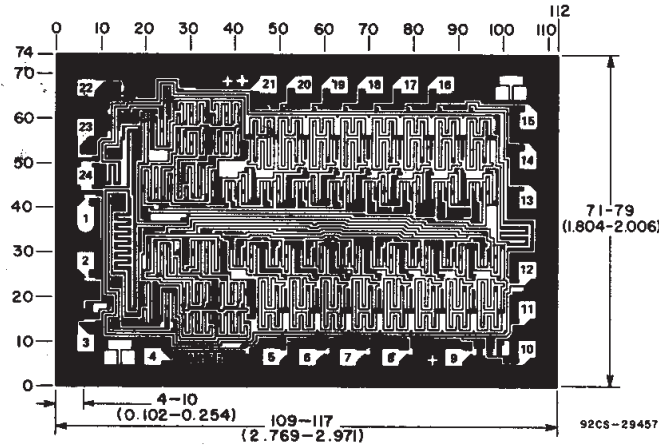


Fig. 14 - Waveforms for setup time and strobe pulse width.



CD4514B
CD4515B

TERMINAL ASSIGNMENT



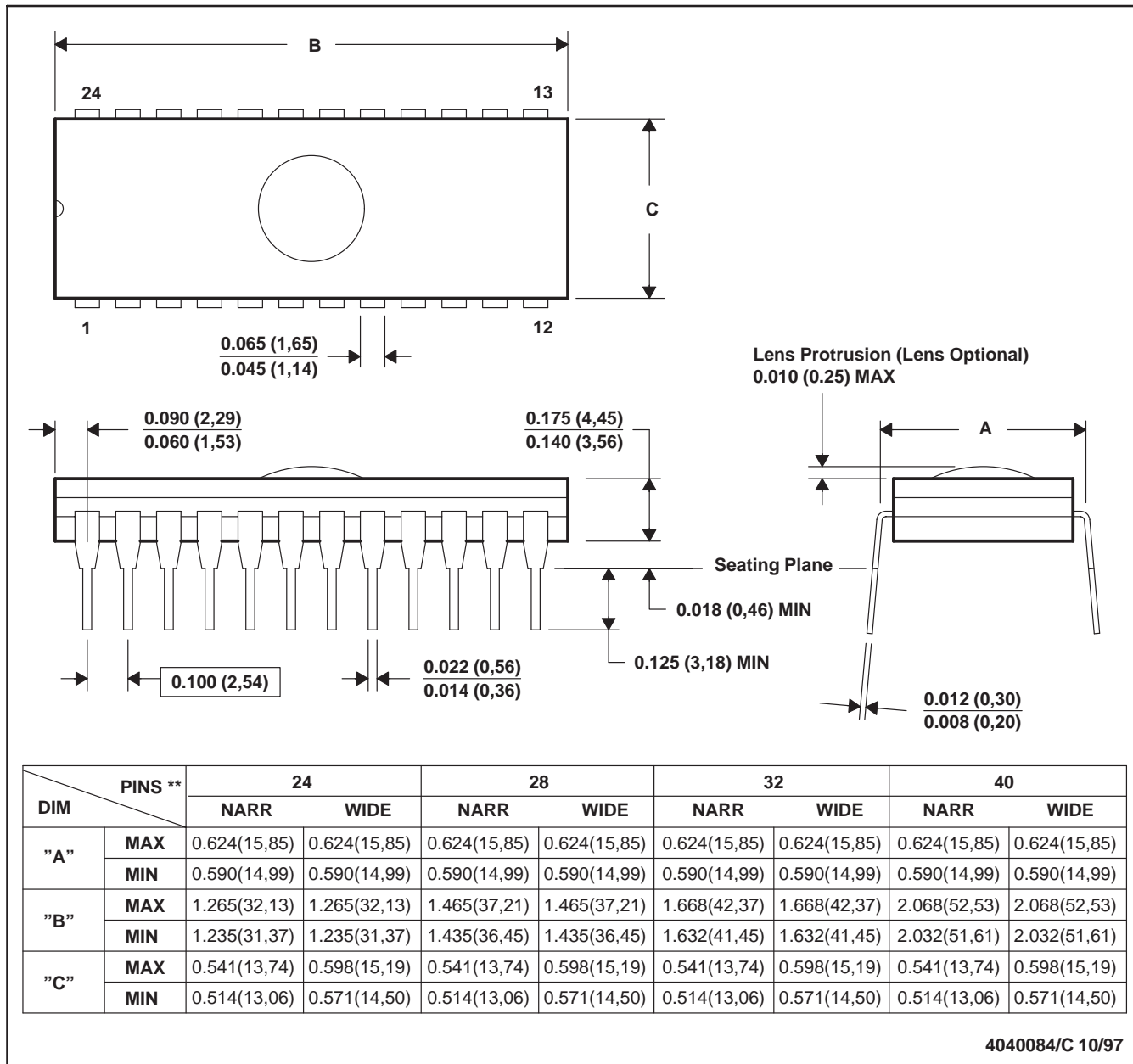
Dimensions and Pad Layout for CD4515B Chip
(Dimensions and pad layout for the CD4514B are identical)

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

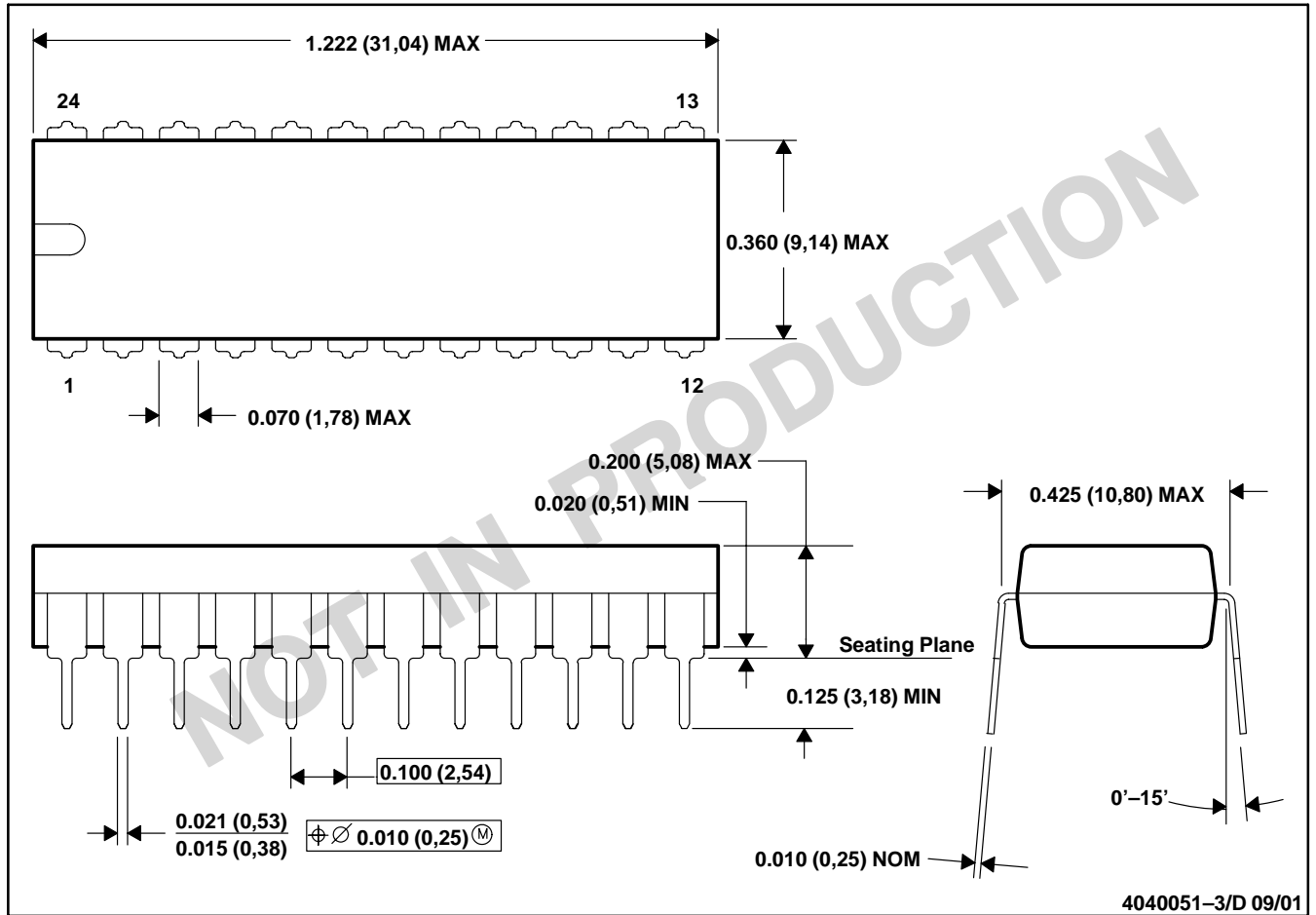
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE

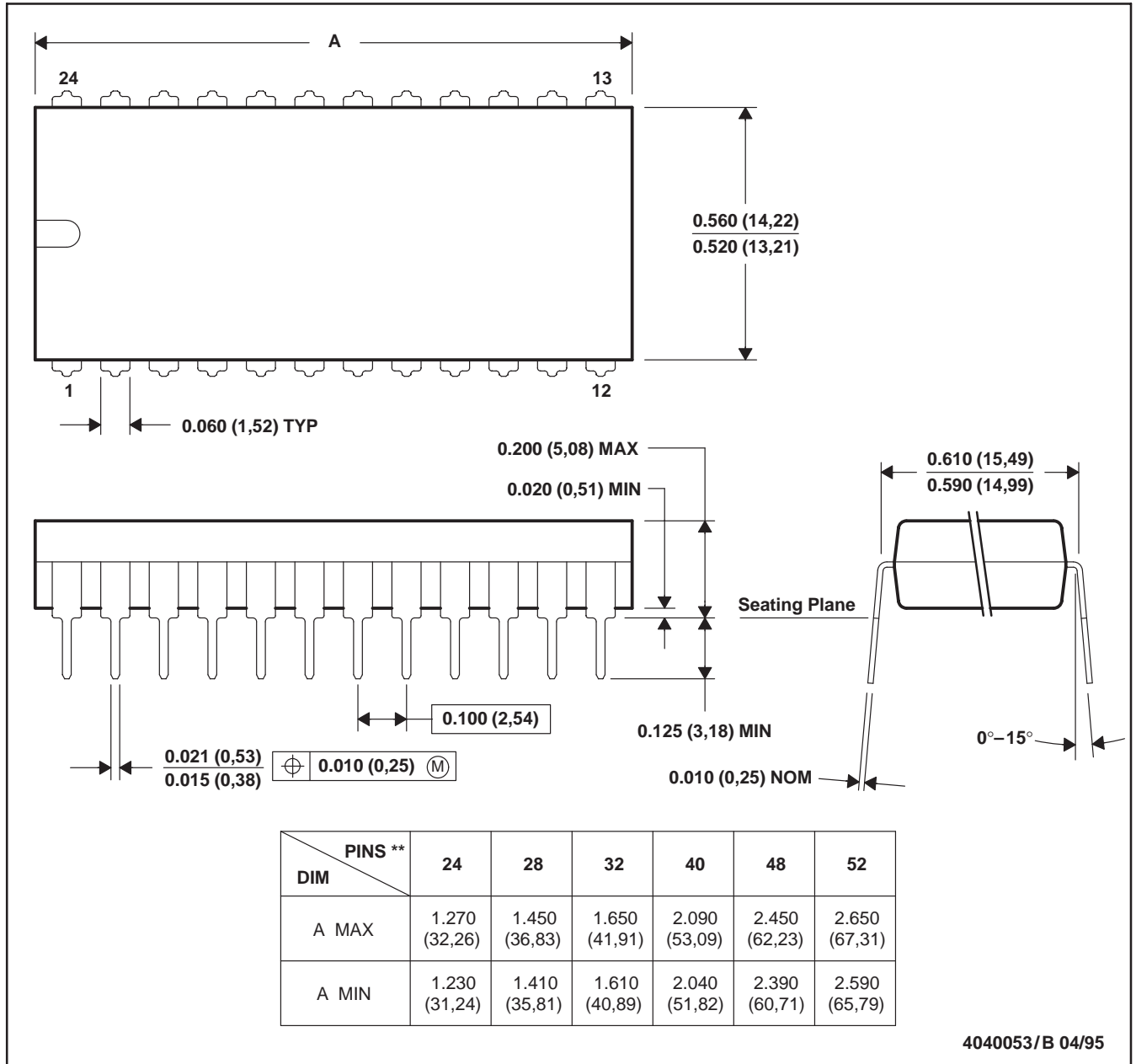


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-010

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

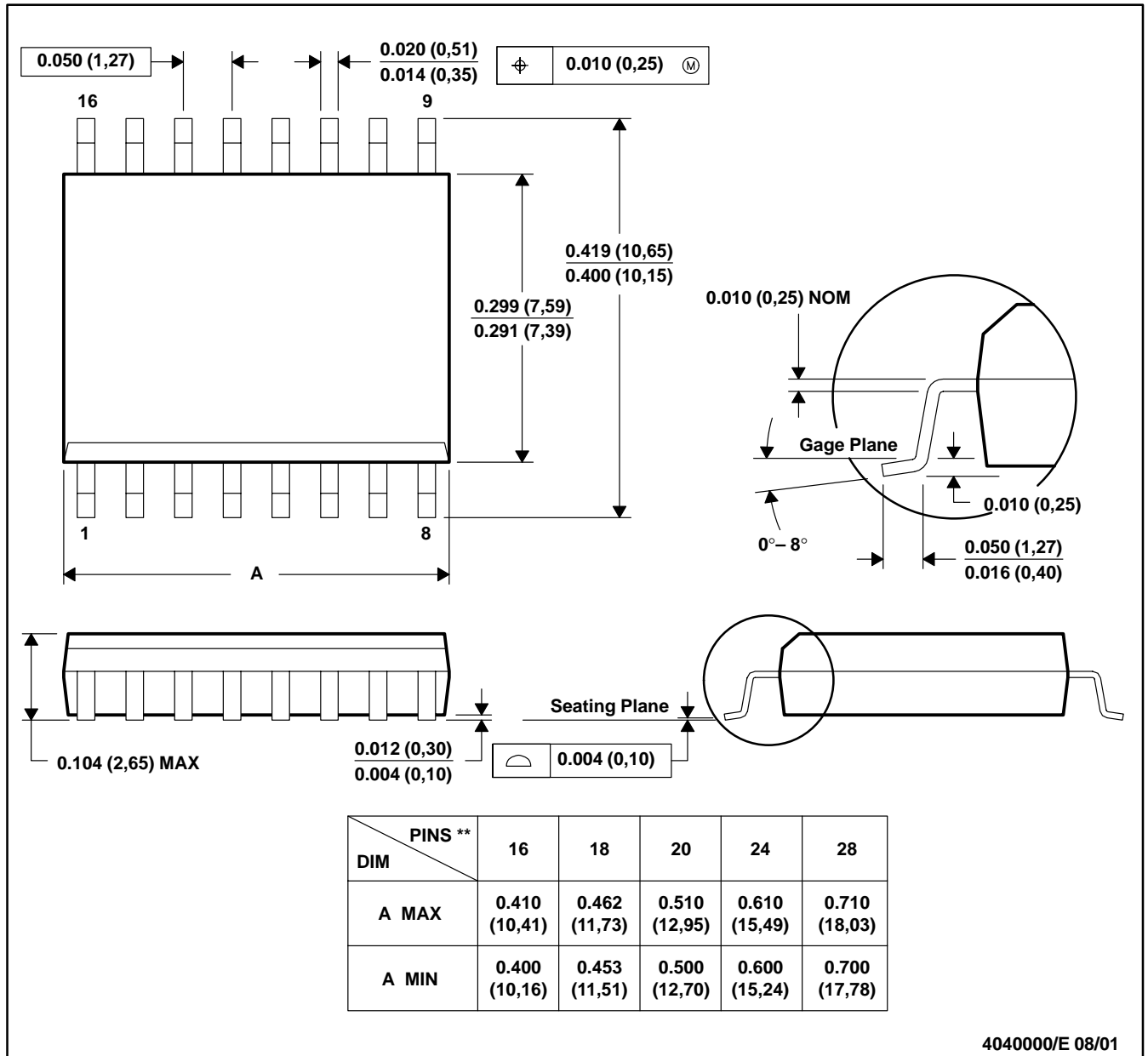


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products & application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265