# QorIQ T2080 Reference Design Board (T2080RDB-PC) User Guide

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# Contents

**Section number** **Title** **Page**

## Chapter 1
## Overview



## Chapter 2
## Architecture

## Chapter 3
## CPLD Specification

# Chapter 1
# Overview

The T2080RDB-PC is a high-performance computing evaluation, development, and test platform supporting the T2080 QorIQ Power Architecture® processor. The T2080RDB-PC is optimized to support the high-bandwidth DDR3LP memory and a full complement of high-speed SerDes ports. This system has two working modes, the Standalone mode and the PCIe Endpoint mode. The motherboard, inside the T2080RDB-PC, is a PCIe form factor card and it is installed in a custom 1U chassis. The system will be in standalone mode by default and you can remove the PCIe from its chassis for PCIe Endpoint mode operation.

**NOTE**

The T2080RDB boards are using Freescale's C29x Crypto Coprocessor series silicon.

## 1.1 Related documentation

The table below lists the related documentation:

**Table 1-1. Related documentation**

| Document name | Description |
|---|---|
| T2080 QorIQ Integrated Multicore Communication Processor Family Reference Manual | This document provides a detail description on the T2080 QorIQ multicore processor and on some of its features like memory map, serial interfaces, power supply, chip features, and clock information. |
| T2080 Product Brief | This document provides an overview of the Freescale T2080 features and examples of the T2080 usage. |
| T2080 QorIQ Advanced Multicore Processor Data Sheet | This document contains the T2080 information on pin assignments, electrical characteristics, hardware design, considerations, package information, and ordering information. |

**NOTE**

Some of the documents mentioned above may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

## 1.2 Acronyms and abbreviations

**Table 1-2. Acronyms and abbreviations**

| Usage | Description |
|---|---|
| COP | Common On-chip Processor |
| CPC | CoreNet Platform Cache |
| CPLD | Complex Programmable Logic Device |
| DIMM | Dual In-Line Memory Module |
| DIP | Dual In-Line Package |
| DMA | Direct Memory Access |
| DPAA | Data Path Acceleration Architecture |
| DRAM | Dynamic Random Access Memory |
| DUT | Device Under Test |
| EC | Ethernet Controllers |
| ECC | Error Detection and Correction |
| EMI | Ethernet Management Interfaces |
| eSDHC | enhanced Secure Digital Host Controller |
| eSPI | enhanced Serial Peripheral Interface |
| FPGA | Field-Programmable Gate Array |
| HW | Hardware |
| I2C | Inter - Integrated Circuit |
| IFC | Integrated Flash Controller |
| JTAG | Joint Test Action Group |
| PCIe/PEX | PCIe = PCI Express = PEX |
| PLD | Programmable Logic Device |
| POR | Power On Reset |
| QMan | Queue Manager |
| SATA | Serial Advanced Technology Attachment |
| SD | Secure Digital |
| SerDes | Serializer/Deserializer |
| SGMII | Serial Gigabit Media Independent Interface |
| SPI | Serial Peripheral Interface |
| SW | Switch |
| SYSCLK | System Clock |

*Table continues on the next page...*

**Table 1-2. Acronyms and abbreviations (continued)**

| Usage | Description |
|---|---|
| UART | Universal Asynchronous Receiver/Transmitter |
| VCC | Voltage for Circuit |
| VTT | Voltage for Terminal |

## 1.3 T2080 silicon features

The T2080 silicon features are as follows:

- Four e6500 cores, built on Power Architecture technology, sharing a 2 MB L2 cache
- 512 KB CoreNet Platform cache (CPC)
- Hierarchical interconnect fabric:
  - CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints
  - Queue Manager (QMan) fabric supporting packet-level queue management and quality of service scheduling
- One 32/64-bit DDR3 SDRAM memory controller:
  - DDR3 and DDR3L with ECC and interleaving support
  - Memory pre-fetch engine
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (Frame Manager 1.1)
  - Queue management for scheduling, packet sequencing, and congestion management (Queue Manager 1.1)
  - Hardware buffer management for buffer allocation and de-allocation (Buffer Manager 1.1)
  - Cryptography Acceleration (SEC 5.2)
  - RegEx Pattern Matching Acceleration (PME 2.1)
  - Decompression/Compression Acceleration (DCE 1.0)
  - DPAA chip-to-chip interconnect, using RapidIO Message Manager (RMan 1.0)
- 16 SerDes lanes at up to 10 GHz.
- Eight Ethernet interfaces, supporting combinations of:
  - Up to four 10 Gbit/s Ethernet MACs
  - Up to eight 1 Gbit/s Ethernet MACs
  - Up to four 2.5 Gbit/s Ethernet MACs
  - IEEE 1588 standard support.
- High-speed peripheral interfaces:

    - Four PCI Express controllers (two supporting PCIe 2.0 and two supporting PCIe 3.0)
    - Two Serial RapidIO 2.0 controllers running at up to 5 GHz with Type 11 messaging and Type 9 data streaming support
- Additional peripheral interfaces:
    - Two Serial ATA (SATA 2.0) controllers
    - Two high-speed USB 2.0 controllers with integrated PHY
    - Enhanced secure digital host controller (SD/MMC/eMMC)
    - Enhanced Serial peripheral interface (eSPI)
    - Four I2C controllers
    - Four 2-pin UARTs or two 4-pin UARTs
    - Integrated flash controller supporting NAND and NOR flash
- Three 8-channel DMA engines
- 896 FC-PBGA package, 25 mm x 25 mm, 0.8 mm pitch

## 1.4 T2080RDB-PC board features

The T2080RDB-PC board features are as follows:

- SerDes connections
    - 16 lanes configuration:
        - SerDes-1 Lane A-B: to two 10GSFP+ (MAC9 and MAC10)
        - SerDes-1 Lane C-D: to two 10GBase-T (MAC1 and MAC2)
        - SerDes-1 Lane E-H: to PCIe slot (PCIe4 x4, Gen3)
        - SerDes-2 Lane A-D: to PCIe Goldfinger (PCIe1 x4, Gen2)
        - SerDes-2 Lane E-F: to C293 secure coprocessor (PCIe2 x2)
        - SerDes-2 Lane G-H: to SATA1 and SATA2
- DDR controller
    - Supports data rates of up to 1600 MHz or 1866 MHz
    - Supports one DDR3LP DIMM of single, dual-rank types
    - DDR power supplies 1.35 V to all devices with automatic tracking of VTT
- IFC/Local Bus
    - NAND flash: 8 bit, async, up to 1 GB
    - NOR: 16 bit, non-multiplexed, up to 128 MB, NOR devices support 8 virtual banks
- Ethernet
    - Two on-board RGMII 10/100/1G Ethernet ports
    - Two on-board XFI 10GEDC for 10G SFP+ Port
    - Two on-board XFI 10GBase-T port

- CPLD
  - Manages system power and reset sequencing
  - Configures DUT, board, clock with dynamic
  - Reset and interrupt monitor and control
  - General fault monitoring and logging
- Clocks
  - System and DDR clock (SYSCLK, DDRCLK)
    - Switch selectable to one of the 16 common settings in the interval 64 MHz-166 MHz
    - Software programmable in 1 MHz increments from 1-200 MHz
  - SerDes clocks
    - Provides clocks to all SerDes blocks and slots
    - 100 MHz
    - 156.25 MHz
- Power supplies
  - Dedicated PMBus regulator for core power; adjustable from 0.7 V to 1.3 V at 60 A
- USB
  - Supports two USB 2.0 ports with integrated PHYs: Two type A ports with 5 V @ 1.5 A per port
- MicroSD card
  - MicroSD port connects directly to MicroSD or TF
- SPI
  - Onboard support of SPI flash
- Other I/O
  - Two serial ports
  - Two I2C ports

## 1.5 Block diagram

The T2080RDB-PC supports two modes of operation, the Standalone mode and the Endpoint mode. There is one configuration in the Standalone mode and second configurations is in the Endpoint mode, the major differences are in the PCIe support. All configurations have Freescale C293, 4x XFI, 2x RGMII, DDR, NOR, NAND, SPI EEPROM, I2C EEPROM, and GPIO. Muxing is controlled by FPGA/CPLD.

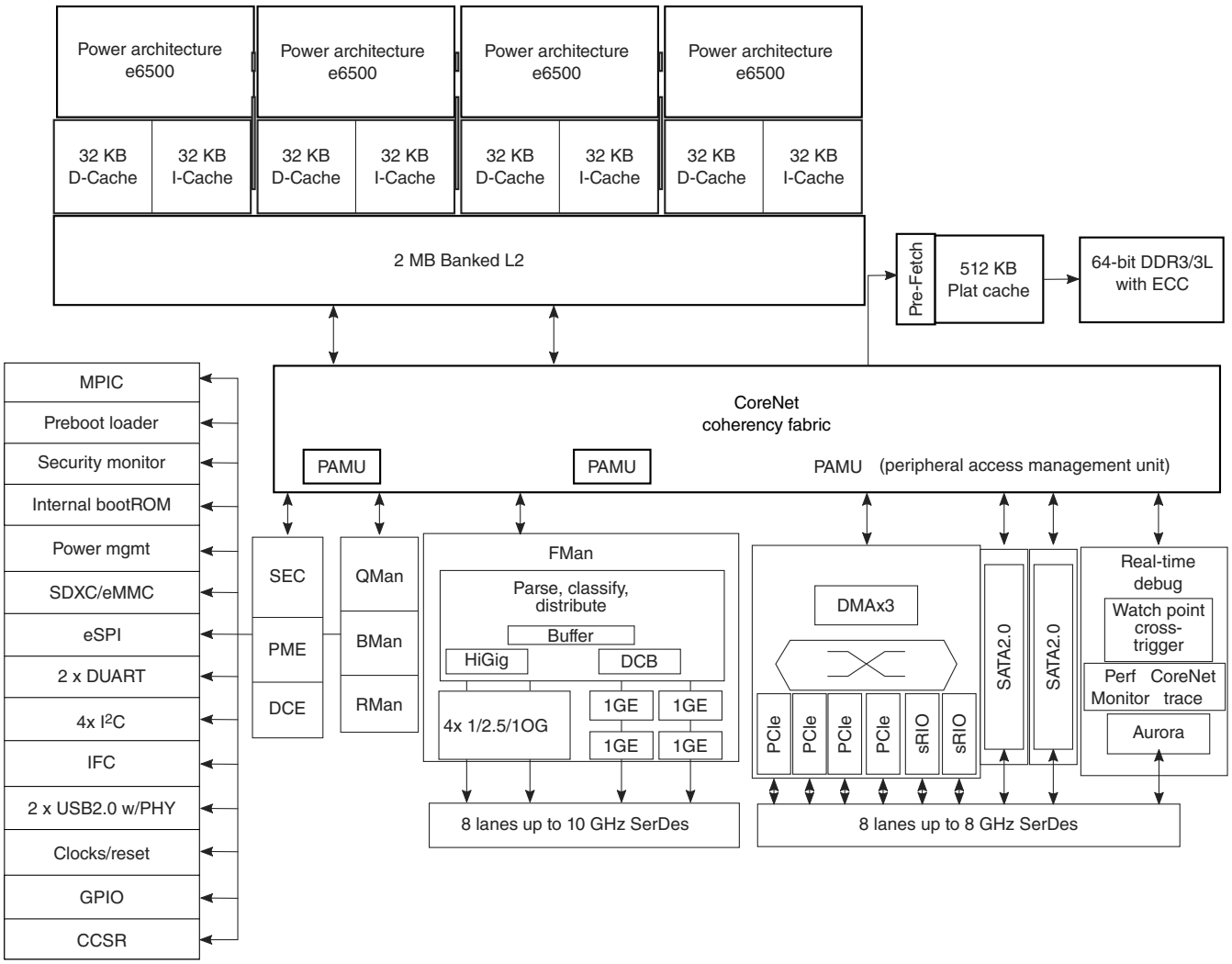



**Figure 1-1. T2080 block diagram**

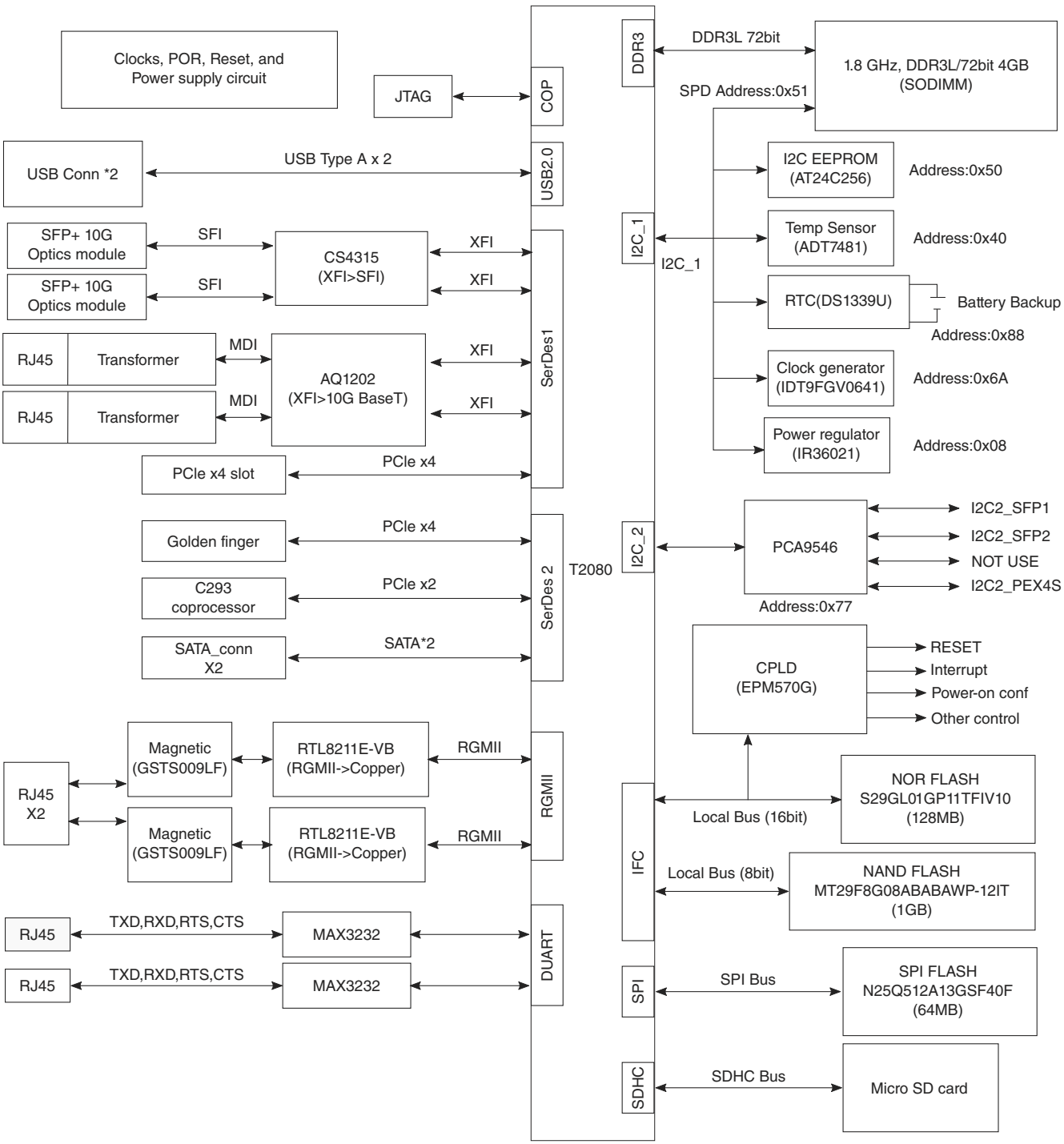



**Figure 1-2. T2080RDB-PC architecture**

# Chapter 2
# Architecture

This section explains the architecture of T2080RDB-PC:

- Processor
- Power
- Reset
- Clocks
- DDR
- SerDes port
- Ethernet controllers
- Ethernet Management Interface
- I2C
- SPI interface
- Local bus
- SDHC interface
- USB interface
- RS-232
- JTAG/COP port
- Connectors, Headers, Jumper, Push buttons, and LEDs
- Temperature
- DIP switch definition

## 2.1 Processor

The T2080RDB-PC supports many features of the T2080 processor, as detailed in the following sections.

## 2.2 Power

The power supply system of the T2080RDB-PC system uses power from a standard 6-pin EPS, to provide power to the numerous processors, CPLD, and peripheral devices.

- Monolithic power supply for VCC (powering internal cores and platform logic)
- DUT-specific power rails are instrumented such that current measurement is possible
- Automatic collection of voltage, current, and power is performed for critical supplies
- Mounting holes are provided of sufficient size to allow onboard supplies to be replaced by bench supplies
- All power supplies can be sequenced as per hardware specifications

The power supplies provided are organized into general categories and are described in the individual sections.

The diagram below shows the power supply architecture.

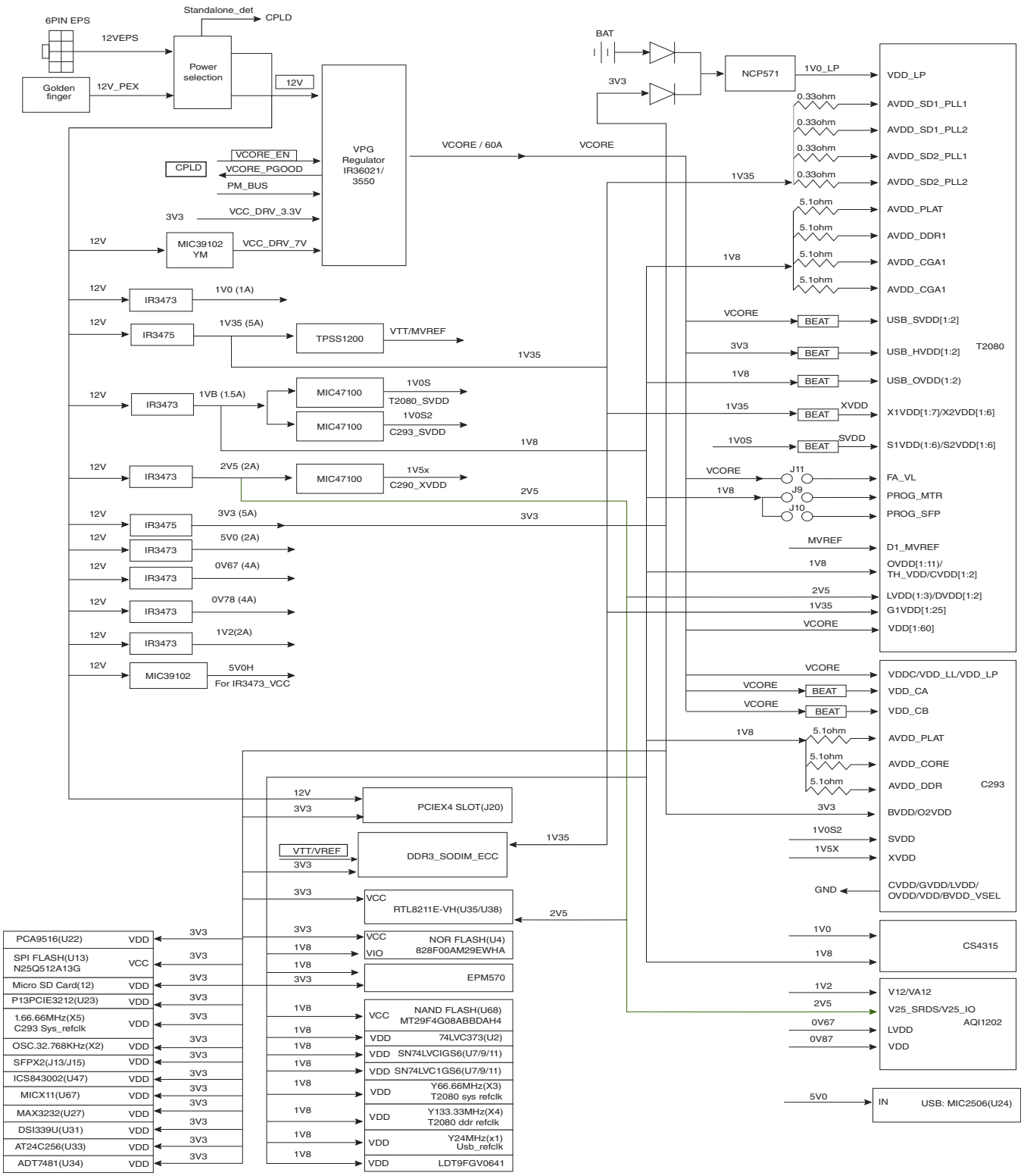



**Figure 2-1. Power supply**

## 2.3 Reset

Reset signals to and from the T2080 processor and other devices on the T2080RDB-PC are managed by CPLD. The diagram below shows an overview of the reset architecture.

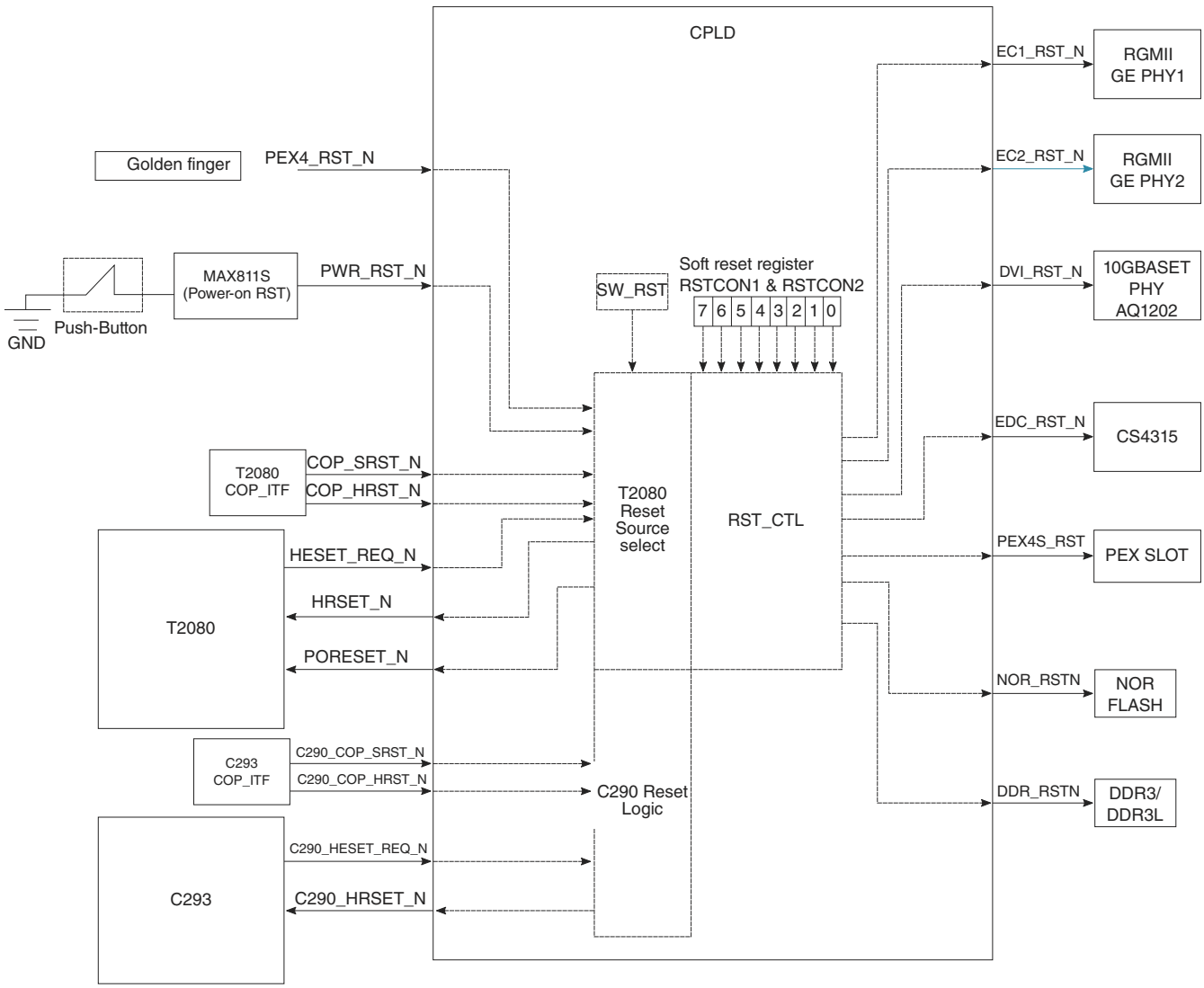



**Figure 2-2. Reset architecture**

## 2.4 Clocks

The clock circuitry provides clocks for the processor, for:

- SYSCLK
- DDRCLK (single-ended and differential)
- SerDes clocks
- Ethernet clocks
- USB clock

The architecture of the clock section is shown in the diagram below.

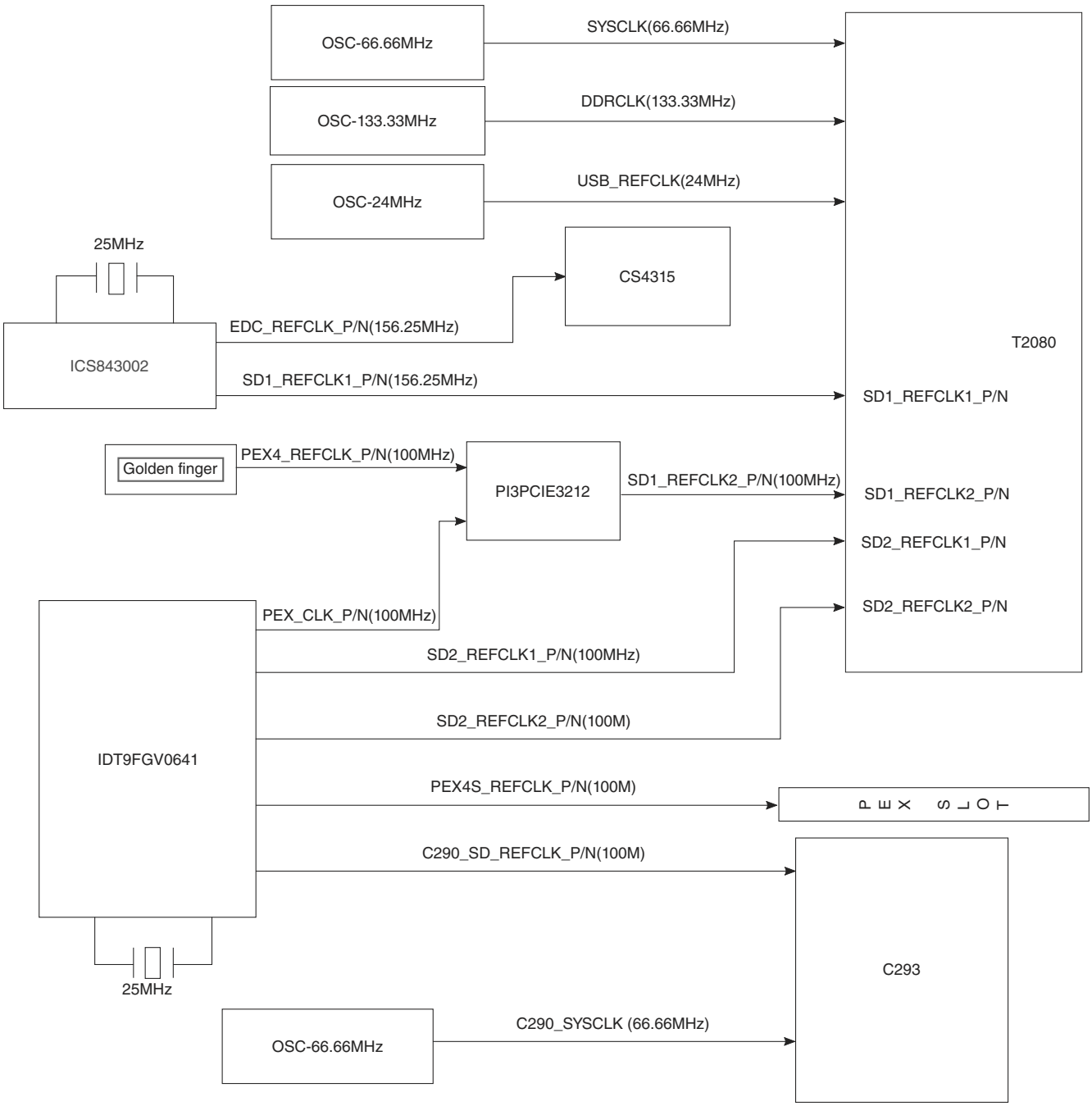



**Figure 2-3. Clock architecture**

## 2.5 DDR

The T2080RDB-PC supports high-speed DRAM, with an SODIM socket, featuring single, dual, and quad-rank support. The memory interface includes the necessary termination and I/O power and is routed so as to achieve maximum performance of the memory bus, as shown in the diagram below.

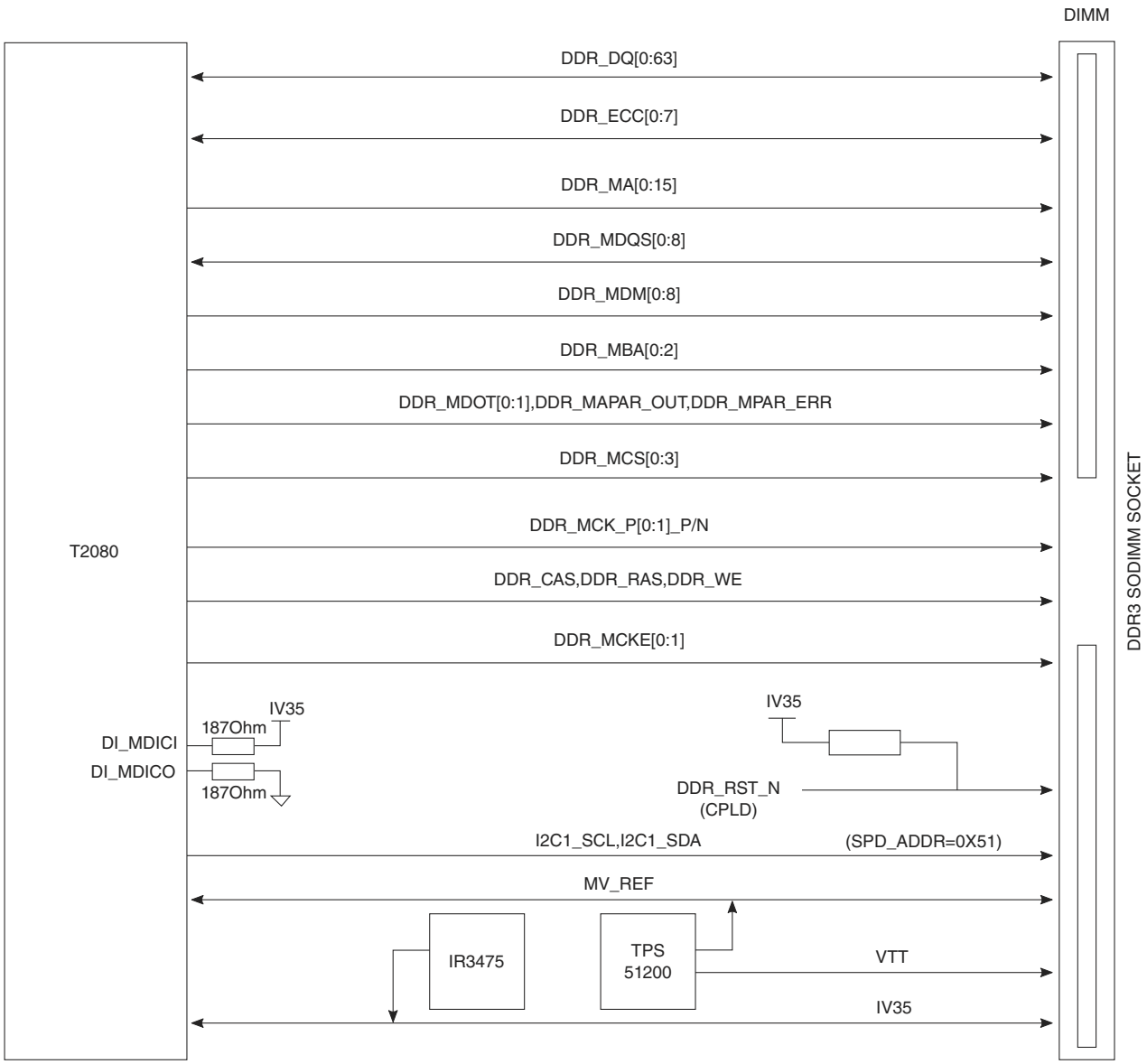



**Figure 2-4. Memory interface**

## 2.6 SerDes port

The T2080 SerDes block provides 16 high-speed serial communication lanes, supporting a variety of protocols, including:

- SGMII 1.25 / 3.125 Gbit/s
- PCI Express (PEX) Gen 1 1X / 2X / 4X 2.5 Gbit/s
- PCI Express (PEX) Gen 2 1X / 2X / 4X 5 Gbit/s
- SATA 1X 1.5 / 3 Gbit/s

The T2080 additionally supports these protocols:

- PCI Express (PEX) Gen 3 1X 8 Gbit/s
- XFI 1X 10.3125 Gbit/s

An overview of the SerDes protocols, which are supported on the T2080RDB, is shown in the table below.

**Table 2-1. SerDes protocols**

| **SERDES1** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **SRDS_PRTCL_S1** | **A** | **B** | **C** | **D** | **E** | **F** | **G** | **H** | **Per lane PLL mapping** |
| 66 | XFI9 | XFI10 | XFI1 | XFI2 | PCIe4 | | | | 1111<br>2222 |
| **SERDES2** | | | | | | | | | |
| **SRDS_PRTCL_S2** | **A** | **B** | **C** | **D** | **E** | **F** | **G** | **H** | **Per lane PLL mapping** |
| 15 | PCIe1 | | | | PCIe2 | PCIe2 | SATA1 | SATA2 | 1111<br>1122 |

The image below shows the SerDes distribution of T2080RDB-PC.

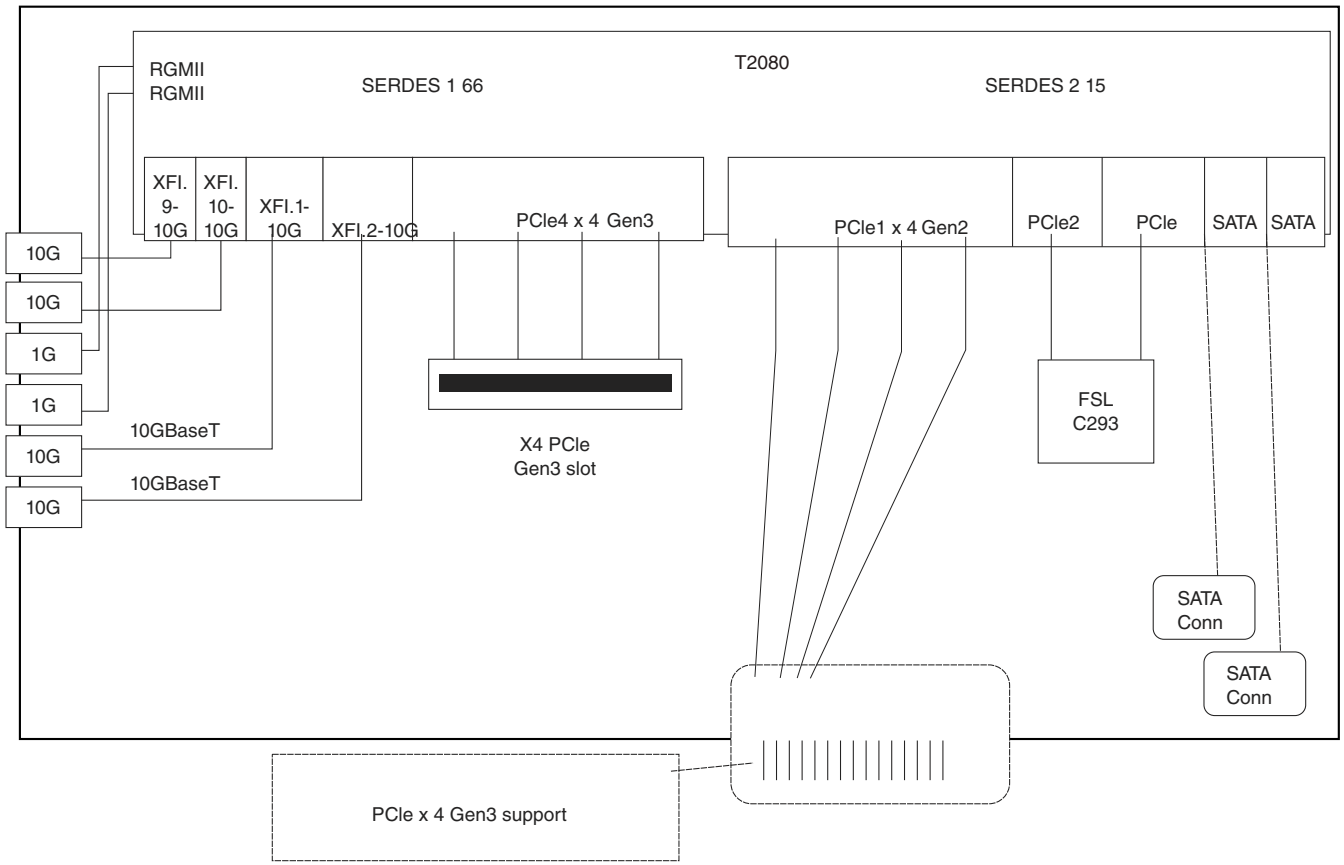



**Figure 2-5. SerDes distribution of T2080RDB-PC**

## 2.6.1 PCI Express support

The T2080RDB-PC supports PCIe x4 Gen 3 for golden finger and PCIe x4 Gen 2 for slot.

## 2.6.2 XFI 10G optics port support

The T2080 supports evaluation of the XFI protocol using Cortina CS4315 dual port 10G CDR. 10G data is carried over the XFI interface. The image below shows the connectivity of XFI interface.

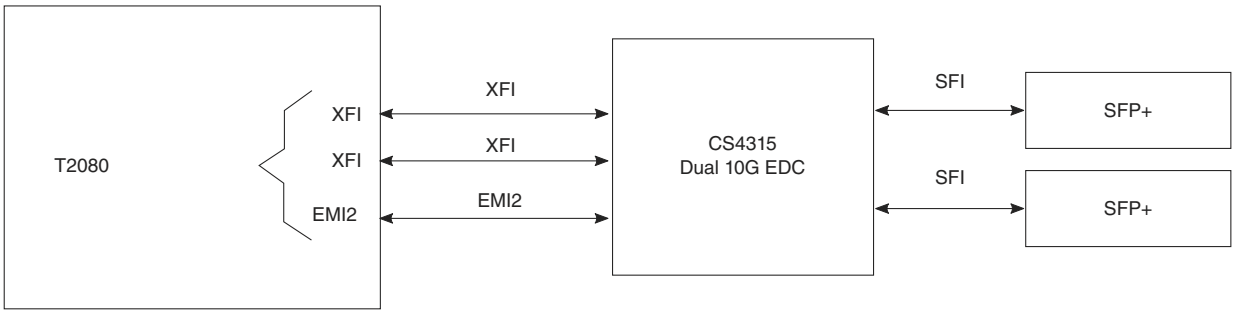



**Figure 2-6. XFI interface**

### 2.6.3 XFI 10GBase-T port support

The T2080 only supports evaluation of the XFI protocol using Aquantia AQ1202 dual port 10GBase-T PHY. 10G data is carried over the XFI interface. The image below shows the connectivity of XFI interface.

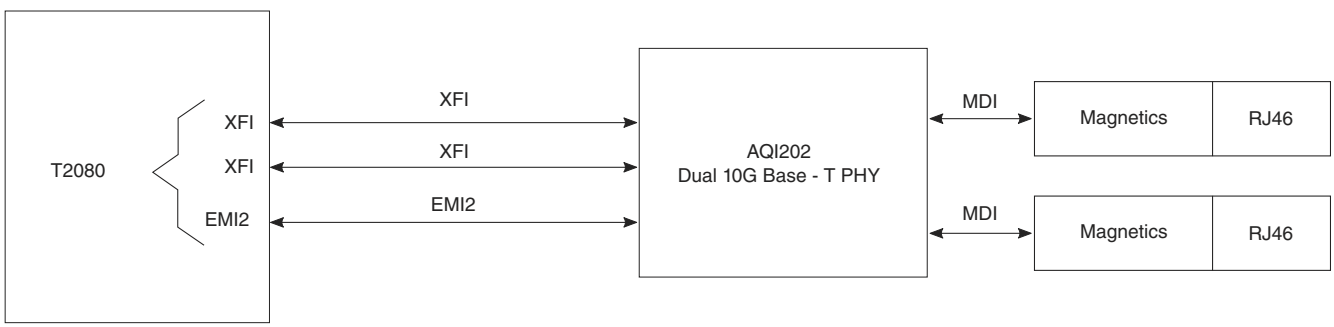



**Figure 2-7. XFI interface**

### 2.6.4 SATA support

SATA is evaluated using the two onboard SATA headers, by selecting a SATA-supporting SerDes protocol.

## 2.7 Ethernet controllers

The T2080 supports two Ethernet Controllers (EC), which can connect to Ethernet PHYs using MII or RGMII protocols. On the T2080RDB-PC, the EC1 and EC2 ports only operates in RGMII mode. Both ports connect to Realtek RTL8211 PHYs.

The image below shows the connectivity of EC1/EC2 interface.

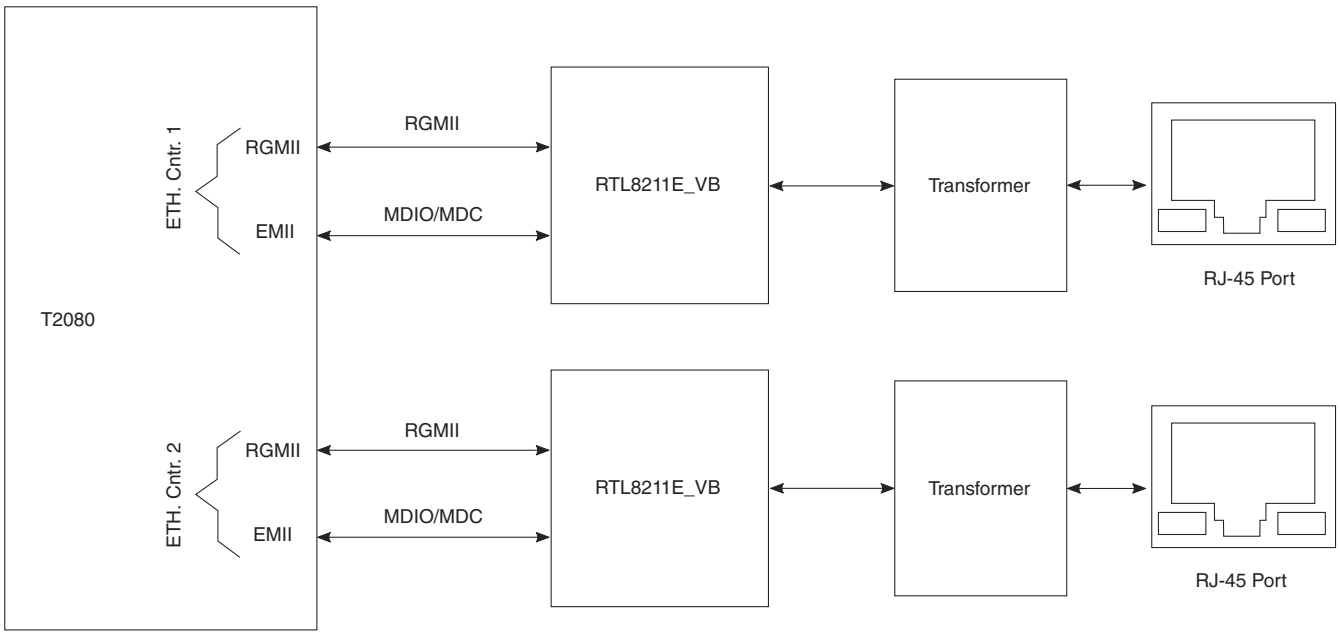



**Figure 2-8. EC1/EC2 interface connectivity**

## 2.8 Ethernet Management Interface

The T2080 has two Ethernet Management Interfaces (EMI), both powered by LVDD. However, EMI2 is only used with XFI based PHYs, which uses 1.2 V pull-up. EMI1 is used with all other non-XFI based PHYs, including the onboard RGMII PHYs. The image below shows the EMI hardware block.

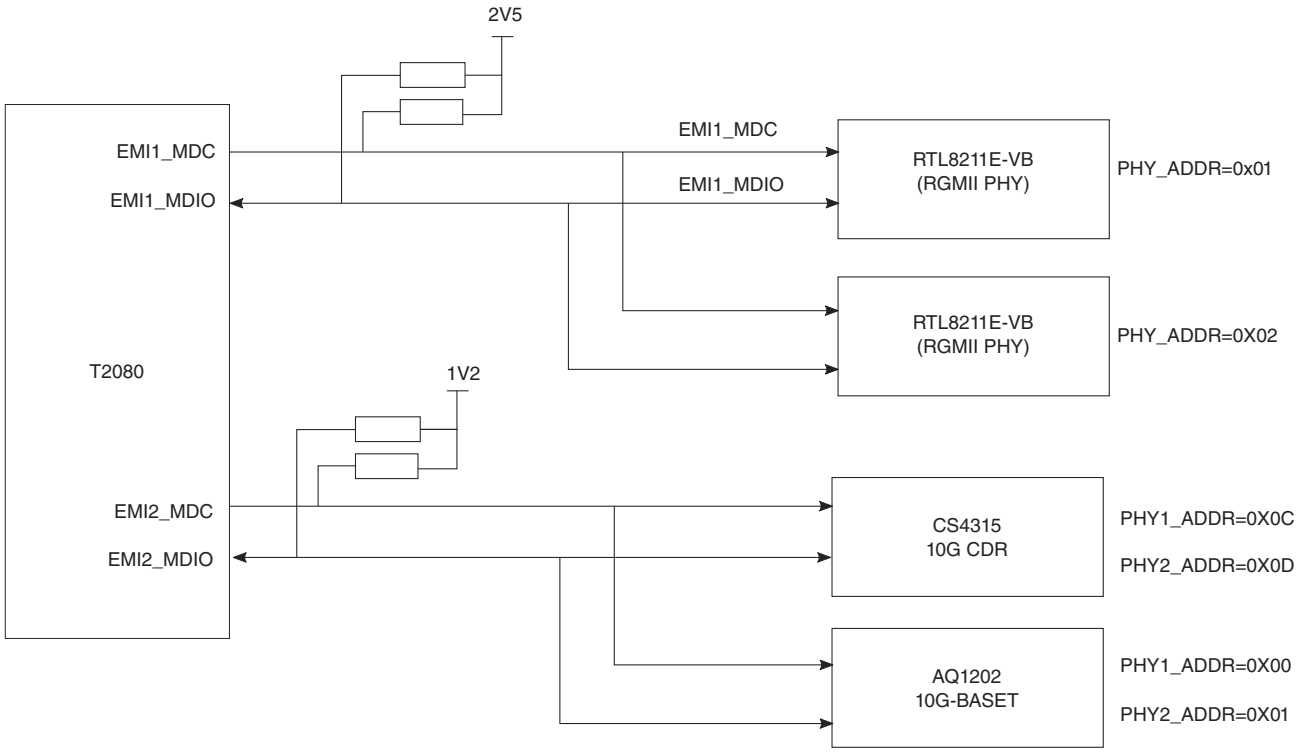



**Figure 2-9. EMI hardware block**

## 2.9 I2C

The T2080 devices supports up to four I2C buses, in order to make the I2C resources equally available to both local and remote systems. The T2080RDB-PC uses I2C1 port to access onboard devices, such as DDR3 DIMM, RTC, I2C EEPROM, clock generator, thermal sensor (ADT7481), and core power regulator (IR36021). The I2C2 bus uses multiplexers to partition the I2C bus into several sub-buses, called channels. Two SFP+ optics use channel 0-1 and the PCIe SLOT use channel 3.

The image below shows the I2C subsystem.

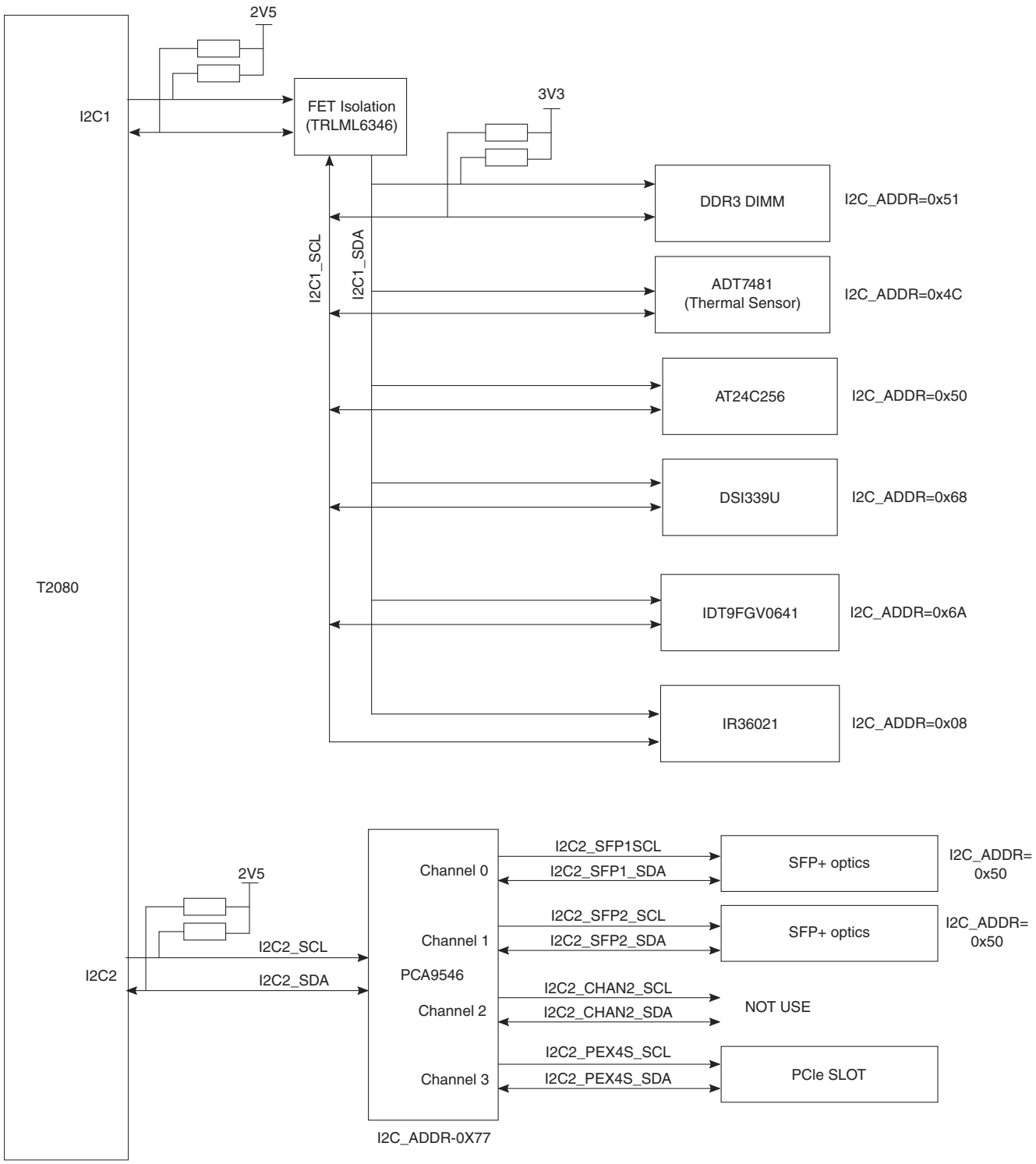



**Figure 2-10. I2C subsystem**

## 2.10 SPI interface

The T2080RDB-PC Serial Peripheral Interface (SPI) pins is only used for onboard SPI device accessing various SPI memory devices.

## 2.11 Local bus

The T2080 Integrated Flash Controller (IFC), also known as the local bus, supports 32-bit addressing and 8 or 16-bit data widths for a variety of devices to effectively manage all these resources with the maximum amount of performance and flexibility.

The image below shows an overview of the IFC bus.

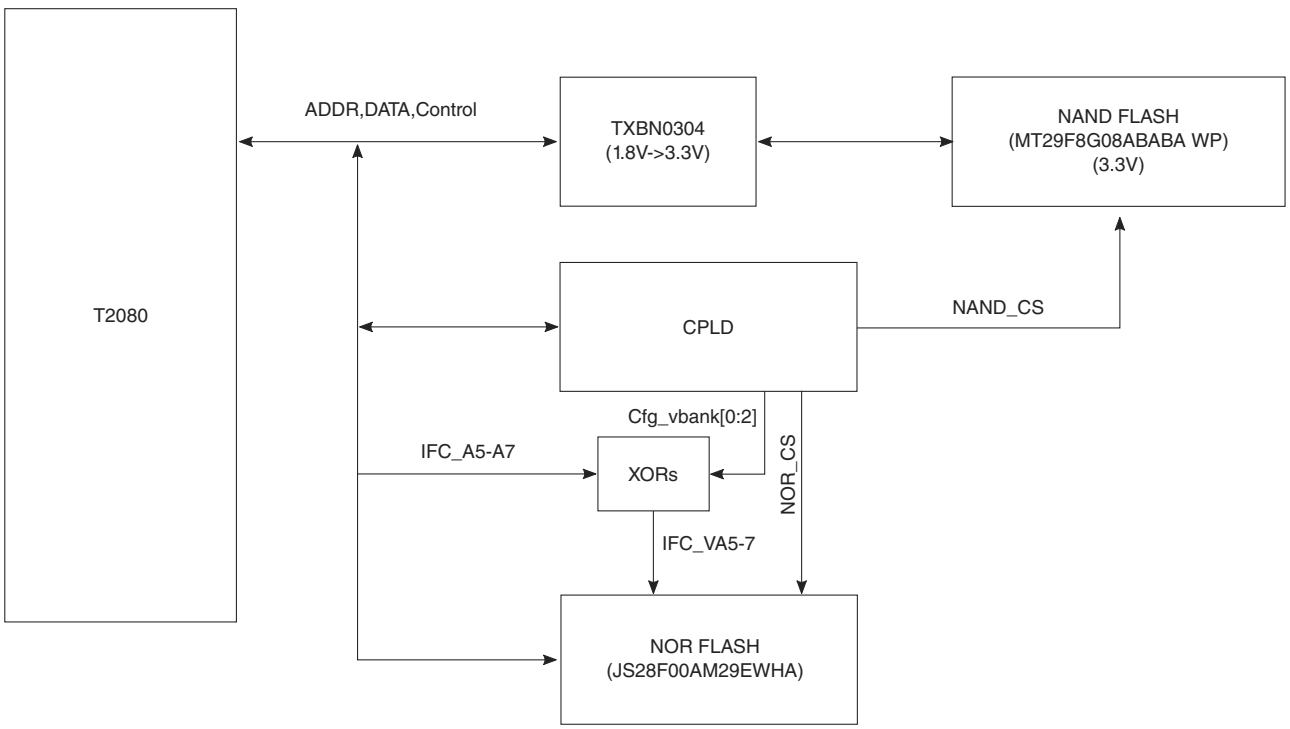



**Figure 2-11. IFC bus**

## 2.12 SDHC interface

The enhanced SD Host Controller (eSDHC) provides an interface between host system and SD cards. The Secure Digital (SD) card is specifically designed to meet the security, capacity, performance, and environmental requirements, inherent in emerging audio and video consumer electronic devices. Booting from eSDHC interface is supported using the processor's on-chip ROM.

On T2080RDB-PC, a single connector is used for MicroSD memory cards, as shown in the image below.

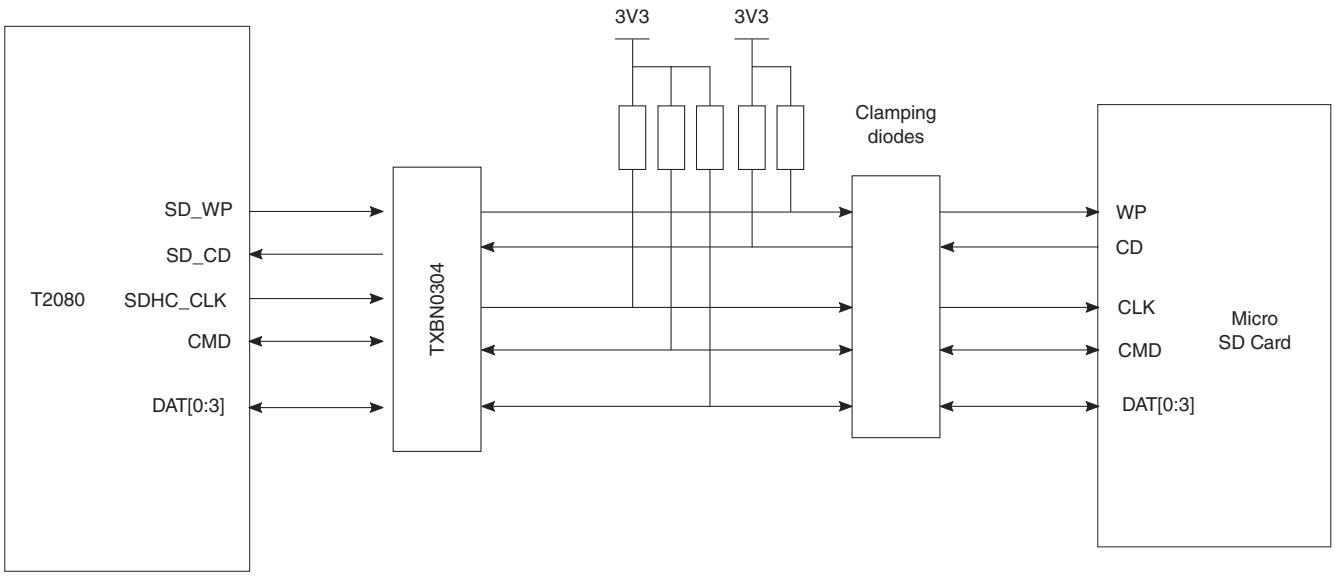



**Figure 2-12. SDHC interface**

## 2.13 USB interface

The T2080RDB-PC systems have two integrated USB 2.0 controllers, that allow direct connection to USB ports with appropriate protection circuitry and power supplies.

The board features are:

- High speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operation
- Host mode
- Dual stacked Type A connection

The USB ports connect to a standard Type A connector (USB1 and USB2) for compatibility with most USB peripherals.

Power for the ports is provided by a MIC2506YM, which supplies 5 V at up to 1 A per port. The power enable and power-fault-detect pins are connected directly to the T2080 for individual port management.

The image below shows how the USB connectivity is implemented on the T2080RDB-PC.

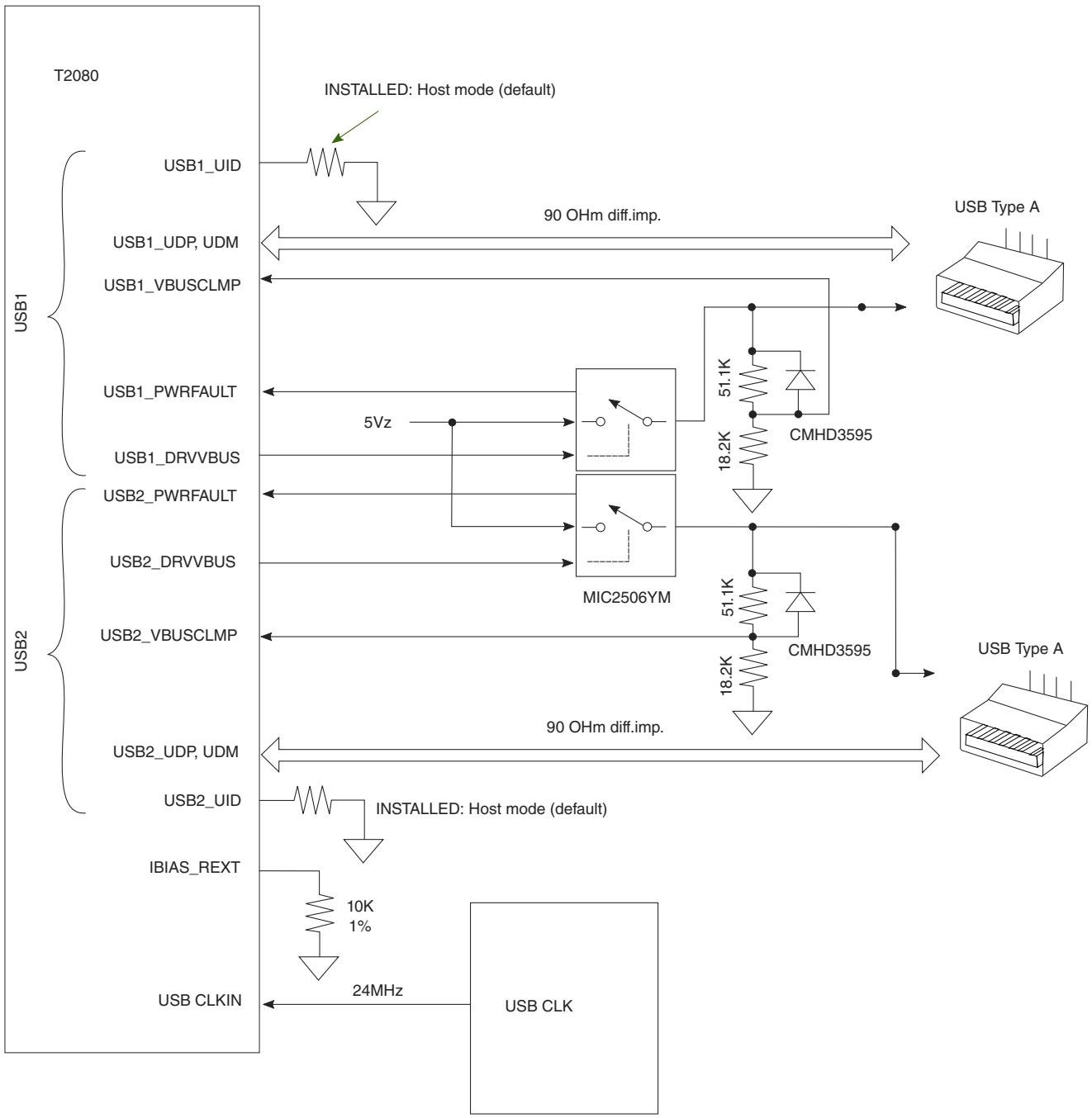



**Figure 2-13. USB connectivity implementation**

## 2.14 RS-232

The T2080 processor has two UART controllers, which provides an RS-232 standard interconnection between the board and an external host. The serial connection is typically configured to run at 11.5 Kbit/s.

Each UART supports:

- Full-duplex operation
- Software-programmable baud generators
- Software-selectable serial interface data format, that includes:
  - Data length
  - Parity
  - 1/1.5/2 STOP bit
  - Baud rate
- Overrun, parity, and framing error detection

The UART ports are routed to 3PIN connectors, as shown in the image below.

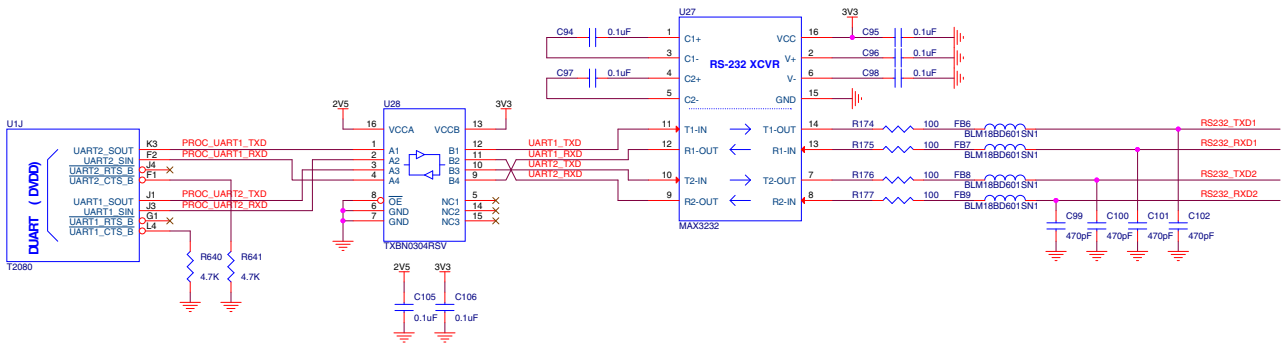



**Figure 2-14. UART ports, routed to 3PIN connectors**

The table below shows the connection setting for the UART 3pin connector to DB9 female cable connection.

**Table 2-2. PIN3 to DB9 connection setting**

| 3PIN connector | RS-232 signal | DB9 female pin number |
|---|---|---|
| 1 | TXD | 2 |
| 2 | GND | 5 |
| 3 | RXD | 3 |

Before powering up the T2080RDB card, configure the serial port of the attached computer with the following values:

- Data rate: 115200 bit/s
- Number of data bits: 8
- Parity: None
- Number of stop bits: 1
- Flow control: Hardware/None

## 2.15 JTAG/COP port

The common on-chip processor (COP) is a part of the T2080's JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the Ethernet port, USB port, parallel port, or RS-232. A typical setup using a USB port emulator is shown in the image below.

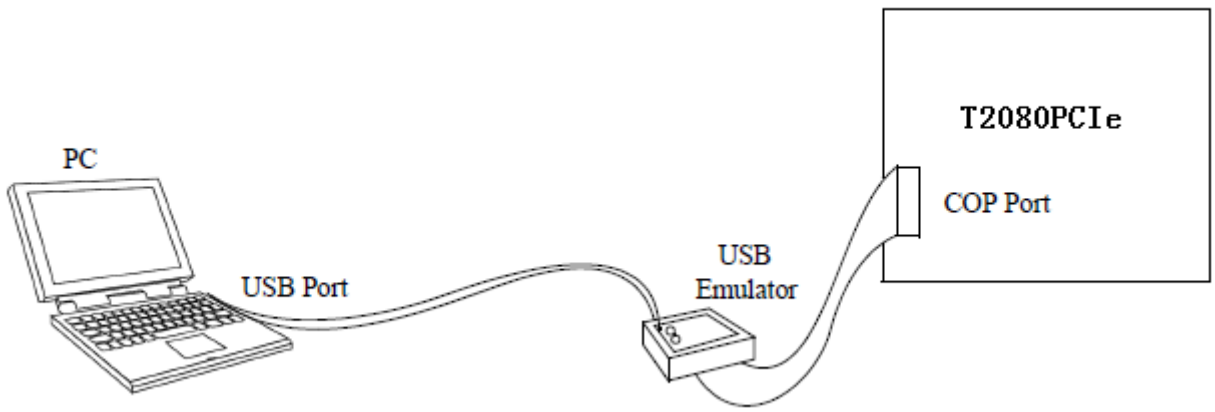



**Figure 2-15. USB port emulator setup**

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pin-out of this connector is shown in the image below.

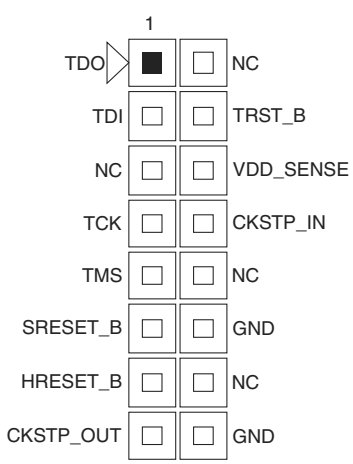



**Figure 2-16. 16-pin connector**

The table below displays the connections made from the T2080RDB-PC COP connector.

**Table 2-3. Connections made from the T2080RDB-PC COP connector**

| Pin no. | Signal name | Connection |
|---|---|---|
| 1 | TDO | Connected directly between the processor and JTAG/COP connector. |
| 2 | NC | Not connected. |
| 3 | TDI | Connected directly between the processor and JTAG/COP connector. |
| 4 | TRST | Routed to the RESET PLD. TRST to the processor is generated from the PLD. |
| 5 | NC | Not connected. |
| 6 | VDD_SENSE | Pulled to 3.3 V using a 10 Ohm resistor. |
| 7 | TCK | Connected directly between the processor and JTAG/COP connector. |
| 8 | CKSTP_IN | Connected directly between the processor and JTAG/COP connector. |
| 9 | TMS | Connected directly between the processor and JTAG/COP connector. |
| 10 | NC | Not connected. |
| 11 | SRESET | Routed to the RESET PLD. SRESET to the processor is generated from the PLD. |
| 12 | GND | Connected to guard. |
| 13 | HRESET | Routed to the RESET PLD. HRESET to the processor is generated from the PLD. |
| 14 | KEY | Not connected. |
| 15 | CKSTP_OUT | Connected directly between the processor and JTAG/COP connector. |
| 16 | GND | Connected to guard. |

## 2.16 Connectors, Headers, Jumper, Push buttons, and LEDs

This section explains:

- Connectors
- Headers
- Jumper
- Push buttons
- LEDs

### 2.16.1 Connectors

Table 2-4 lists the various connectors on the T2080RDB-PC platform.

**Table 2-4. Connectors on the T2080RDB-PC platform**

| Reference designators | Used for | Notes |
|---|---|---|
| J28 | 6-pin EPS connector | - |
| J2 | MicroSD card | - |

*Table continues on the next page...*

**Table 2-4. Connectors on the T2080RDB-PC platform (continued)**

| Reference designators | Used for | Notes |
|---|---|---|
| J20 | PCIe x4 slot | Intended use is for PCIe cards that are 25 W or less. |
| J21, J22 | SATA | - |
| J43 | TDM Riser card | - |
| J36, J37 | Ethernet ports | RGMII -> Copper |
| J17, J18 | Ethernet ports | 10GBase-T |
| J13, J15 | Ethernet ports | 10G optics |
| J41 | Dual Type A USB | - |
| J35 (2 ports) | UART | - |
| J8 | Battery holder | - |
| J1 | SODIM | - |
| J22, J23 | FXS ports | - |
| J24 | FXO port | - |
| J34 | CPU fan | - |
| J33, J44-J46 | Shelf FAN | - |

## 2.16.2 Headers

The table below lists the various headers on the T2080RDB-PC platform.

**Table 2-5. Headers on the T2080RDB-PC platform**

| Reference designators | Used for | Notes |
|---|---|---|
| J24 | Altera Header | Used for programming the Altera CPLD devices. |
| J26 | IR36021 Header | Used for programming the IR36021. |
| J3 | COP/JTAG | Used for debugging the T2080. |

## 2.16.3 Jumper

The table below describes how the push Jumper is used on the T2080RDB-PC platform.

**Table 2-6. Jumper on the T2080RDB-PC platform**

| Reference designator | Description | Status 1 | Status 2 |
|---|---|---|---|
| J29 | Battery selection for VDD_LP source | Mounted: Battery acts as a VDD_LP input source | Unmounted: Battery is disconnected |
| J30 | Tamper detection pin powered selection | 1-2: Tamper detection pin is powered on | 2-3: Tamper detection pin is powered off |

*Table continues on the next page...*

**Table 2-6. Jumper on the T2080RDB-PC platform (continued)**

| Reference designator | Description | Status 1 | Status 2 |
|---|---|---|---|
| J9 | PROG_SFP selection | Mounted: Fuse programming | Unmounted: Normally operate |
| J25 | Not used | - | - |
| J38 | SD/TF card voltage selection | 1-2: TF card works at 3.3 V | 2-3: TF card works at 1.8 V |

## 2.16.4 Push buttons

The table below describes what the push buttons are used for on the T2080RDB-PC platform.

**Table 2-7. Push buttons on T2080RDB-PC platform**

| Reference designators | Used for | Notes |
|---|---|---|
| SW5 | Reset | Used for resetting the whole board. |
| SW4 | Power on/off | Used for turning the power on or off. |

## 2.16.5 LEDs

Table 2-8 lists all the LEDs on the T2080RDB-PC front plate.

**Table 2-8. LEDs on the T2080RDB-PC front plate**

| LEDs | Used for | Controlled by |
|---|---|---|
| D12 | Power on | +3.3V rail |
| D4 | SFP1_LED0 | CPLD |
| D5 | SFP1_LED1 | CPLD |
| D6 | SFP2_LED0 | CPLD |
| D7 | SFP2_LED1 | CPLD |

## 2.17 Temperature

The T2080 has a thermal diode attached to the die, allowing direct temperature measurement. These pins are connected to an ADT7481 3 channel thermal monitor. One channel monitors the T2080 and another channel monitors the C29x, which allows direct reading of the temperature of the die and is accurate to ±1 °C. The third channel of the ADT7481 measures the ambient (board) temperature.

The ADT7481 temperature warning and alarm signals are connected to the CPLD for monitoring. CPLD uses these signals to adjust CPU FAN speed and protect the CPU from over-temperature failure.

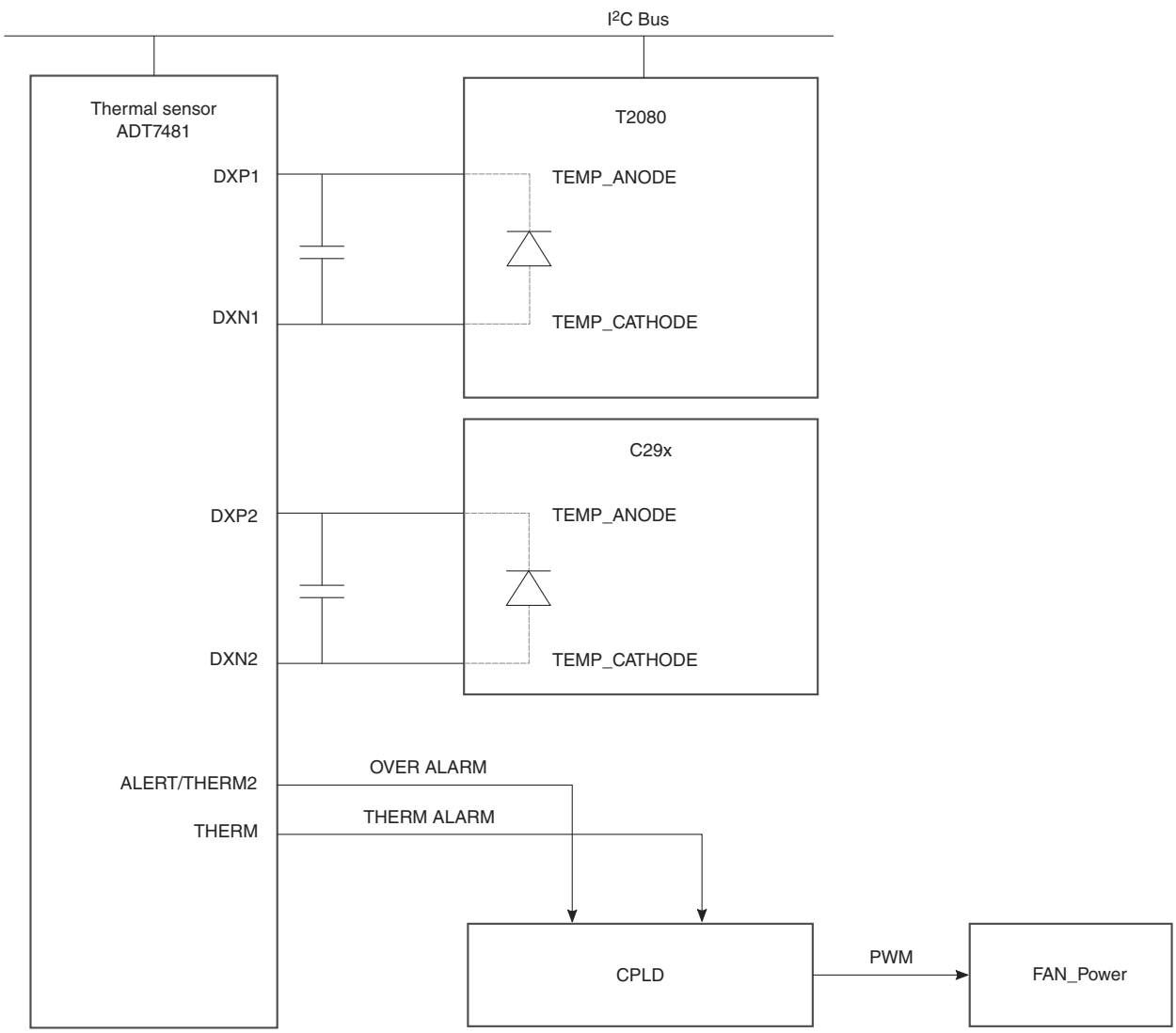



**Figure 2-17. Temperature**

## 2.18 DIP switch definition

The T2080RDB-PC board has user selectable switches, for evaluating different boot configurations and other special configurations for this device.

This configuration allows either the switch or the CPLD register to set the POR pin. The CPLD register allows software to override the pin remotely when the board is in the board farm.

In order to use the CPLD override option, software sets an override bit, that allows the CPLD to override the switch setting during power on reset.

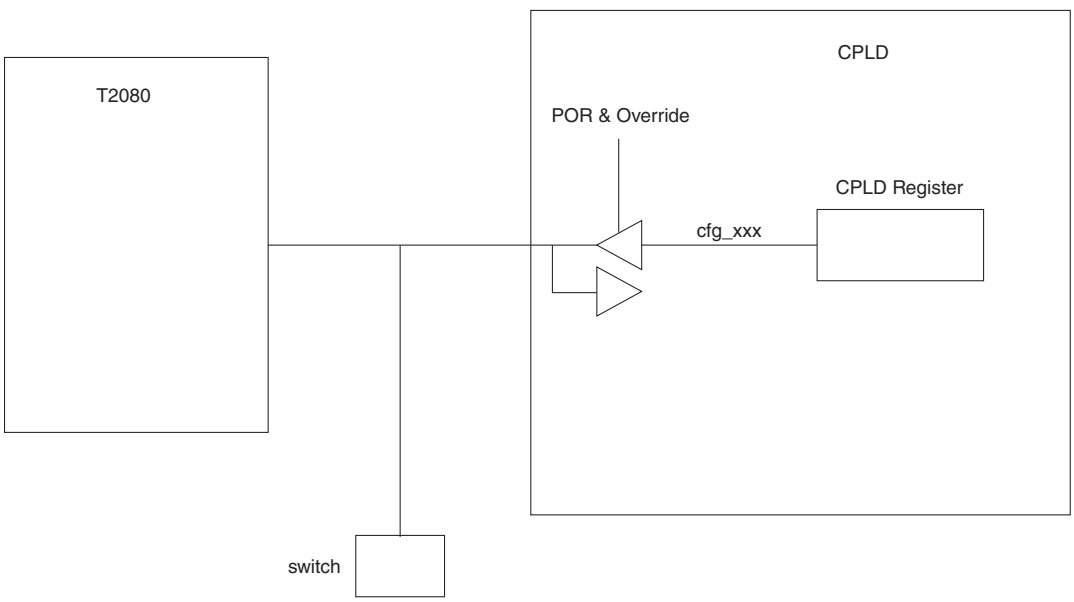



**Figure 2-18. DIP switch definition**

Table 2-9 shows how POR configuration is done through switches.

**Table 2-9. POR configuration through switches**

| Switch | Signal name | Pin name | Signal meaning | Setting |
|---|---|---|---|---|
| SW1[1:8] | cfg_rcw_src[0:7] | IFC_AD[8:15] | Reset Configuration word source.<br>For details, see *T2080 Integrated Multicore Communications Processor Family Reference Manual* (document T2080RM) | NOR boot: 00010011_1<br>NAND boot: 10000010_1<br>SPI boot: 00100010_1<br>SD boot: 00100000_0 |
| SW2[1] | cfg_rcw_src[8] | IFC_CLE | Reset Configuration word source | For details, see *T2080 Integrated Multicore Communications Processor Family Reference Manual* (document T2080RM) |
| SW2[2] | cfg_ifc_te | IFC_TE | IFC external transceiver enable polarity select | 0: IFC drives logic 1 for TE assertion |

*Table continues on the next page...*

## Table 2-9. POR configuration through switches (continued)

| Switch | Signal name | Pin name | Signal meaning | Setting |
|---|---|---|---|---|
| | | | | 1: IFC drives logic 0 for TE assertion |
| SW2[3] | cfg_pll_config_sel_b | IFC_A18 | Reserved | Reserved |
| SW2[4] | cfg_por_ainit | IFC_A19 | Reserved | Reserved |
| SW2[5:6] | cfg_svr[0:1] | IFC_A[16:17] | Reserved | Reserved |
| SW2[7] | cfg_dram_type | IFC_A21 | DRAM type selection | 1: DDR3L(1.35V) |
| SW2[8] | cfg_rsp_dis | IFC_AVD | Reserved | Reserved |
| SW3[1] | cfg_eng_use0 | IFC_WE0 | Sys_clock selection | 1: Single sys_clk is selected |
| SW3[2:3] | cfg_eng_use[1:2] | Reserved | Reserved | - |
| SW3[4] | BOOT_FLASH_SEL | - | Boot flash selection | SW3[4] = 0 for NOR boot<br>SW3[4] = 1 for NAND boot<br>See note[1] |
| SW3[5:7] | CFG_VBANK[0:2] | - | NOR flash bank select | 000: bank0<br>100: bank4<br>See note[2] |
| SW3[8] | TEST_SEL_N | TEST_SEL_B | - | 1:T2080 |

1. For SW3[4]: BOOT_FLASH_SEL, it can act as boot flash selection, when BOOT_FLASH_SEL=1, NOR flash is boot flash or NAND flash is boot flash.
2. SW3[5:7] can be used to change the staring address for the memory banks. The NOR flash memory is divided into eight memory banks with 16 MB size each. Eight different U-Boot image can be programmed into each memory bank. When NOR flash is selected as boot flash (CS0 is connected to NOR flash by setting SW3[4] to ON, RCW[0:8] is set to 0_0111_xxxx using SW1[1:8] and SW2[1]), different U-Boot image can be selected to boot up the board, by setting SW3[5:7].

# Chapter 3
# CPLD Specification

This section explains the CPLD registers.

## 3.1 CPLD Memory Map

**memory map**

| Offset address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|---|---|---|---|---|---|
| 0 | Chip ID1 register (CHIPID1) | 8 | R | 55h | 3.1.1/37 |
| 1 | Chip ID2 register (CHIPID2) | 8 | R | AAh | 3.1.2/38 |
| 2 | Hardware version register (HWVER) | 8 | R | See section | 3.1.3/38 |
| 3 | Software version register (SWVER) | 8 | R | See section | 3.1.4/39 |
| 10 | Reset control register (RSTCON) | 8 | w1c | See section | 3.1.5/39 |
| 11 | Flash control and status register (FLHCSR) | 8 | R/W | See section | 3.1.6/40 |
| 12 | Thermal control and status register (THMCSR) | 8 | R/W | See section | 3.1.7/40 |
| 13 | Panel LED control and status register (LEDCSR) | 8 | R/W | See section | 3.1.8/41 |
| 14 | SFP+ control and status register (SFPCSR) | 8 | R/W | See section | 3.1.9/41 |
| 15 | Miscellanies control and status register (MISCCSR) | 8 | R/W | See section | 3.1.10/42 |
| 16 | Boot configuration override register (BOOTOR) | 8 | R/W | See section | 3.1.11/43 |
| 17 | Boot configuration register 1 (BOOTCFG1) | 8 | R/W | See section | 3.1.12/43 |
| 18 | Boot configuration register 2 (BOOTCFG2) | 8 | R/W | See section | 3.1.13/43 |

### 3.1.1 Chip ID1 register (CHIPID1 )

Address: 0h base + 0h offset = 0h

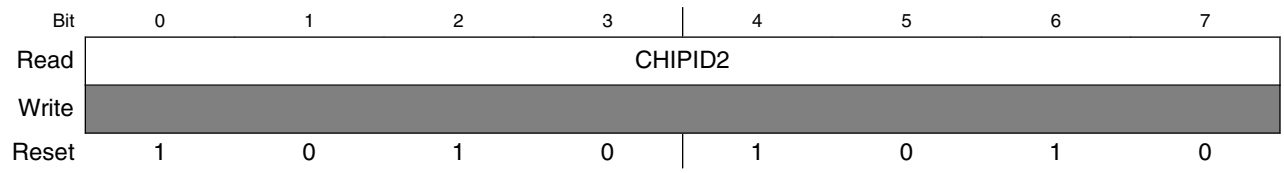
| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read | CHIPID1 | | | | | | | |
| Write | | | | | | | | |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

**CHIPID1 field descriptions**

| Field | Description |
|---|---|
| 0–7<br>CHIPID1 | 0x55, Identification of the CPLD image. |

## 3.1.2 Chip ID2 register (CHIPID2)

Address: 0h base + 1h offset = 1h



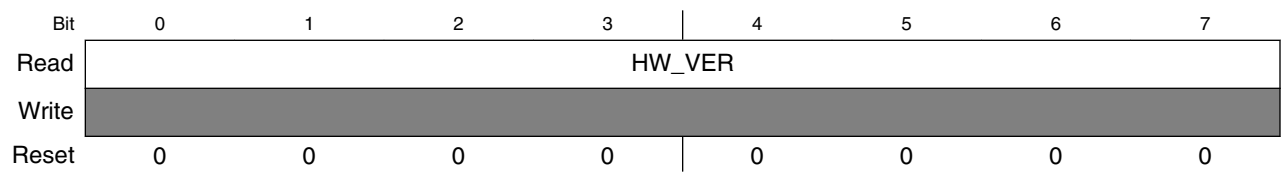

**CHIPID2 field descriptions**

| Field | Description |
|---|---|
| 0–7<br>CHIPID2 | 0xaa, Identification of the CPLD image. |

## 3.1.3 Hardware version register (HWVER)

Hardware version register.

Address: 0h base + 2h offset = 2h




**HWVER field descriptions**

| Field | Description |
|---|---|
| 0–7<br>HW_VER | The version field of the hardware board. |

## 3.1.4 Software version register (SWVER)

Address: 0h base + 3h offset = 3h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read | SW_VER | | | | | | | |
| Write | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SWVER field descriptions**

| Field | Description |
|---|---|
| 0–7<br>SW_VER | The version field of the CPLD software. |

## 3.1.5 Reset control register (RSTCON)

Address: 0h base + 10h offset = 10h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read | SW_RST | C293_RST | Reserved | EC1_RST | EC2_RST | EDC_RST | XGT_RST | PEX_RST |
| Write | w1c | w1c | | w1c | w1c | w1c | w1c | w1c |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**RSTCON field descriptions**

| Field | Description |
|---|---|
| 0<br>SW_RST | 0: No reset occurs.<br>1: Writing logic 1 will produce whole board reset# signal; this bit can auto clear. |
| 1<br>C293_RST | 0: No reset occurs.<br>1: Writing logic 1 will produce C293 Coprocessor reset# signal; this bit can auto clear. |
| 2<br>- | This field is reserved. |
| 3<br>EC1_RST | 0: No reset occurs.<br>1: Writing logic 1 will produce RGMII PHY1 (RTL82111E-VB) reset# signal; this bit can auto clear. |
| 4<br>EC2_RST | 0: No reset occurs.<br>1: Writing logic 1 will produce RGMII PHY2 (RTL82111E-VB) reset# signal; this bit can auto clear. |
| 5<br>EDC_RST | 0: No reset occurs.<br>1: Writing logic 1 will produce 10GEDC PHY(CS4315) reset# signal; this bit can auto clear. |
| 6<br>XGT_RST | 0: No reset occurs.<br>1: Writing logic 1 will produce 10GBase-T PHY(AQ1202) reset# signal; this bit can auto clear. |
| 7<br>PEX_RST | 0: No reset occurs<br>1: Writing logic 1 will produce PCIe x4 slot reset# signal; this bit can auto clear. |

## 3.1.6 Flash control and status register (FLHCSR)

Address: 0h base + 11h offset = 11h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read | BOOT_SEL | BANK_OR | SW_BANK_SEL0 | SW_BANK_SEL1 | SW_BANK_SEL2 | BANK_SEL0 | BANK_SEL1 | BANK_SEL2 |
| Write | | | | | | | | |
| Reset | n | 0 | n | n | n | 0 | 0 | 0 |

**FLHCSR field descriptions**

| Field | Description |
|---|---|
| 0<br>BOOT_SEL | 0: Boot from 16-bit NOR flash.<br>1: Boot from 8-bit NAND flash. |
| 1<br>BANK_OR | 0: NOR flash bank select from CPLD override disable.<br>1: NOR flash bank select from CPLD override enable. |
| 2<br>SW_BANK_SEL0 | 0: NOR flash bank select bit0 of switch status is 0.<br>1: NOR flash bank select bit0 of switch status is 1. |
| 3<br>SW_BANK_SEL1 | 0: NOR flash bank select bit1 of switch status is 0.<br>1: NOR flash bank select bit1 of switch status is 1. |
| 4<br>SW_BANK_SEL2 | 0: NOR flash bank select bit2 of switch status is 0.<br>1: NOR flash bank select bit2 of switch status is 1. |
| 5<br>BANK_SEL0 | 0: NOR flash bank select bit0 set 0.<br>1: NOR flash bank select bit0 set 1. |
| 6<br>BANK_SEL1 | 0: NOR flash bank select bit1 set 0.<br>1: NOR flash bank select bit1 set 1 |
| 7<br>BANK_SEL2 | 0: NOR flash bank select bit2 set 0.<br>1: NOR flash bank select bit2 set 1. |

## 3.1.7 Thermal control and status register (THMCSR)

Address: 0h base + 12h offset = 12h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read | THM_FAULT | THM_ALERT | Reserved | | FAN_PWM | | | |
| Write | | | | | | | | |
| Reset | n | n | 0 | 0 | 1 | 1 | 1 | 1 |

**THMCSR field descriptions**

| Field | Description |
|---|---|
| 0<br>THM_FAULT | 0: Thermal sensor no fault occurs.<br>1: Thermal sensor fault output. |
| 1<br>THM_ALERT | 0: Thermal sensor no alert occurs.<br>1: Thermal sensor alert output. |
| 2–3<br>- | This field is reserved. |
| 4–7<br>FAN_PWM | 0000: PWM duty cycle is 0%, fan stop running.<br>0001 - 1110: PWM duty cycle is 6.7% - 93.3%, fan speed control.<br>1111: PWM duty cycle is 100%, fan full speed. |

## 3.1.8 Panel LED control and status register (LEDCSR )

Address: 0h base + 13h offset = 13h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | STS_LED | Reserved | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**LEDCSR field descriptions**

| Field | Description |
|---|---|
| 0<br>STS_LED | 0: Panel STATUS LED on.<br>1: Panel STATUS LED flash at 0.5s. |
| 1–7<br>- | This field is reserved. |

## 3.1.9 SFP+ control and status register (SFPCSR )

Address: 0h base + 14h offset = 14h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read | SFP1_DET | SFP1_<br>TXDIS | SFP1_<br>RXLOS | SFP1_<br>TXFAIL | SFP2_DET | SFP2_<br>TXDIS | SFP2_<br>RXLOS | SFP2_<br>TXFAIL |
| Write | | | | | | | | |
| Reset | n | 0 | n | n | n | 0 | n | n |

**SFPCSR field descriptions**

| Field | Description |
|---|---|
| 0<br>SFP1_DET | 0: SFP+1 module not inserted<br>1: SFP+1 module inserted |
| 1<br>SFP1_TXDIS | 0: SFP+1 TX enable<br>1: SFP+1 TX disable |
| 2<br>SFP1_RXLOS | 0: SFP+1 RX LOS logic 0<br>1: SFP+1 RX LOS logic 1(some SFP+ used as RXSD) |
| 3<br>SFP1_TXFAIL | 0: SFP+1 TX FAIL not occurs<br>SFP+1 TX FAIL occurs |
| 4<br>SFP2_DET | 0: SFP+2 module not inserted<br>1: SFP+2 module inserted |
| 5<br>SFP2_TXDIS | 0: SFP+2 TX enable<br>1: SFP+2 TX disable |
| 6<br>SFP2_RXLOS | 0: SFP+2 RX LOS logic 0<br>1: SFP+2 RX LOS logic 1(some SFP+ used as RXSD) |
| 7<br>SFP2_TXFAIL | 0: SFP+2 TX FAIL not occurs<br>1: SFP+2 TX FAIL occurs |

## 3.1.10 Miscellanies control and status register (MISCCSR )

Address: 0h base + 15h offset = 15h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read | RUN_MODE | Reserved | | | | | PEX_PRS | TEST_SEL_N |
| Write | | | | | | | | |
| Reset | n | 0 | 0 | 0 | 0 | 0 | n | n |

**MISCCSR field descriptions**

| Field | Description |
|---|---|
| 0<br>RUN_MODE | 0: T2080RDB-PC runs as standalone mode<br>1: T2080RDB-PC runs as PCIe x4 add-in card |
| 1–5<br>- | This field is reserved. |
| 6<br>PEX_PRS | 0: PCIe x4 card not present<br>1: PCIe x4 card present |
| 7<br>TEST_SEL_N | 0: TEST_SEL_N pin status is 0<br>1: TEST_SEL_N pin status is 1 |

## 3.1.11 Boot configuration override register (BOOTOR)

Address: 0h base + 16h offset = 16h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | Reserved | | | | | | | BOOT_OR |
| Reset | | | | | | | | |

**BOOTOR field descriptions**

| Field | Description |
|---|---|
| 0–6<br>- | This field is reserved. |
| 7<br>BOOT_OR | 0: Boot configuration from CPLD override disable<br>1: Boot configuration from CPLD override enable |

## 3.1.12 Boot configuration register 1 (BOOTCFG1 )

Address: 0h base + 17h offset = 17h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | cfg_rcw_src[0:7] | | | | | | | |
| Reset | | | | | | | | |

**BOOTCFG1 field descriptions**

| Field | Description |
|---|---|
| 0–7<br>cfg_rcw_src[0:7] | **NOTE:** For details, see T2080 Integrated Multicore Communications Processor Family Reference Manual (document T2080RM). |

## 3.1.13 Boot configuration register 2 (BOOTCFG2)

Address: 0h base + 18h offset = 18h

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | cfg_rcw_<br>src8 | Reserved | cfg_svr[0:1] | | Reserved | cfg_eng_use[0:2] | | |
| Reset | | | | | | | | |

## BOOTCFG2 field descriptions

| Field | Description |
|---|---|
| 0<br>cfg_rcw_src8 | RCW source bit 8. |
| 1<br>- | This field is reserved. |
| 2–3<br>cfg_svr[0:1] | cfg_svr bits for Power-on Reset using. |
| 4<br>- | This field is reserved. |
| 5–7<br>cfg_eng_use[0:2] | cfg_eng_use bits for Power-on Reset using. |

# Appendix A
# Revision history

The table below summarizes revisions to this document.

**Table A-1. Revision history**

| Revision | Date | Topic cross-reference | Change description |
|---|---|---|---|
| Rev. 0 | 06/2015 | - | Initial public release. |

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