Octal, 16-Bit DAC with 5 ppm/°C On-Chip Reference in 16-Lead TSSOP

Enhanced Product

AD5668-EP

FEATURES

Enhanced product features
- **Supports defense and aerospace applications (AQEC)**
- **Military temperature range (−55°C to +125°C)**
- **Controlled manufacturing baseline**
- **One assembly/test site**
- **One fabrication site**
- **Product change notification**
- **Qualification data available on request**

Low power, smallest pin-compatible octal DAC: 16 bits
16-lead TSSOP
On-chip 1.25 V, 5 ppm/°C reference
Power down to 400 nA at 5 V, 200 nA at 3 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on reset to zero scale or midscale
3 power-down functions
Hardware LDAC and LDAC override function
CLR function to programmable code
Rail-to-rail operation

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments

FUNCTIONAL BLOCK DIAGRAM

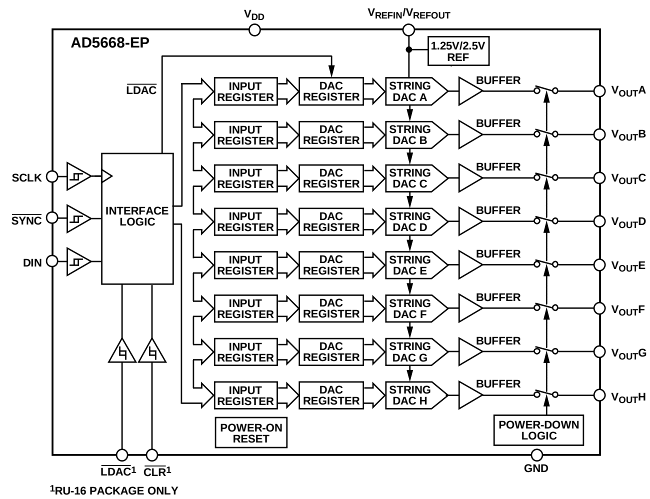

Figure 1.

GENERAL DESCRIPTION

The AD5668-EP is a low power, octal, 16-bit, buffered voltage-output digital-to-analog converter (DAC). It operates from a single 2.7 V to 5.5 V supply and is guaranteed monotonic by design.

The AD5668-EP has an on-chip reference with an internal gain of 2. The AD5668-EP has a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V. The on-board reference is off at power-up, allowing the use of an external reference, and the internal reference is enabled via a software write.

The part incorporates a power-on-reset circuit that ensures that the DAC output powers up to 0 V and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode for any or all DAC channels. The outputs of all DACs can be updated simultaneously using the LDAC function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous CLR that updates all DACs to a user-programmable code—zero scale, midscale, or full scale.

The AD5668-EP uses a versatile 3-wire serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI, QSPI, MICROWIRE, and DSP interface standards.

Additional application and technical information can be found in the AD5668 data sheet.

PRODUCT HIGHLIGHTS

1. Octal, 16-bit DAC.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 16-lead TSSOP.
4. Power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 200 nA at 3 V and 400 nA at 5 V.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

1/2018—Rev. A to Rev. B

Change to Features Section ... 1
Changes to Table 5 ... 7
Changes to Figure 23 ... 11
Moved Figure 33 ... 13
Changes to Ordering Guide ... 14

1/2015—Rev. 0 to Rev. A

Changes to Ordering Guide ... 14

10/2010—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range is −55°C to +125°C, typical at +25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
STATIC PERFORMANCE[1]					
Resolution	16			Bits	
Relative Accuracy		±8	±21	LSB	See Figure 4
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design (see Figure 7)
Zero-Code Error		1	14	mV	All 0s loaded to DAC register (see Figure 9)
Zero-Code Error Drift		±2		µV/°C	
Full-Scale Error		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 10)
Gain Error			±1	% FSR	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
Offset Error		±1	±14	mV	
DC Power Supply Rejection Ratio		−80		dB	V_{DD} ± 10%
DC Crosstalk (External Reference)		10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5		µV/mA	Due to load current change
		10		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 5 V
Power-Up Time		4		µs	Coming out of power-down mode, V_{DD} = 5 V
REFERENCE INPUTS					
Reference Current		40	55	µA	V_{REF} = V_{DD} = 5.5 V (per DAC channel)
Reference Input Range	0		V_{DD}	V	
Reference Input Impedance		14.6		kΩ	
REFERENCE OUTPUT					
Output Voltage	1.247		1.253	V	At ambient
Reference Temperature Coefficient[2]		±5		ppm/°C	
Reference Output Impedance		7.5		kΩ	
LOGIC INPUTS[2]					
Input Current			±3	µA	All digital inputs
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 5 V
Input High Voltage, V_{INH}	2			V	V_{DD} = 5 V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	4.5		5.5	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[3]					V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		1.3	1.8	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		2	2.6	mA	Internal reference on
I_{DD} (All Power-Down Modes)[4]					
V_{DD} = 4.5 V to 5.5 V		0.4	1	µA	V_{IH} = V_{DD} and V_{IL} = GND

[1] Linearity calculated using a reduced code range of AD5668 (Code 512 to 65,024). Output unloaded.
[2] Guaranteed by design and characterization; not production tested.
[3] Interface inactive. All DACs active. DAC outputs unloaded.
[4] All eight DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range is −55°C to +125°C, typical at +25°C.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time		6	10	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.5		V/µs	
Digital-to-Analog Glitch Impulse		4		nV-sec	1 LSB change around major carry (see Figure 24)
Digital Feedthrough		0.1		nV-sec	
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 Hz to 20 MHz
Digital Crosstalk		0.5		nV-sec	
Analog Crosstalk		2.5		nV-sec	
DAC-to-DAC Crosstalk		3		nV-sec	
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.2 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = 0x8400, 1 kHz
		100		nV/√Hz	DAC code = 0x8400, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. V_{DD} = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX} V_{DD} = 2.7 V to 5.5 V	Unit	Conditions/Comments
t_1[1]	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ to SCLK falling edge set-up time
t_5	4	ns min	Data setup time
t_6	4	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	15	ns min	Minimum $\overline{SYNC}$ high time
t_9	13	ns min	$\overline{SYNC}$ rising edge to SCLK fall ignore
t_{10}	0	ns min	SCLK falling edge to $\overline{SYNC}$ fall ignore
t_{11}	10	ns min	$\overline{LDAC}$ pulse width low
t_{12}	15	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{13}	5	ns min	$\overline{CLR}$ pulse width low
t_{14}	0	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{15}	300	ns typ	$\overline{CLR}$ pulse activation time

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.

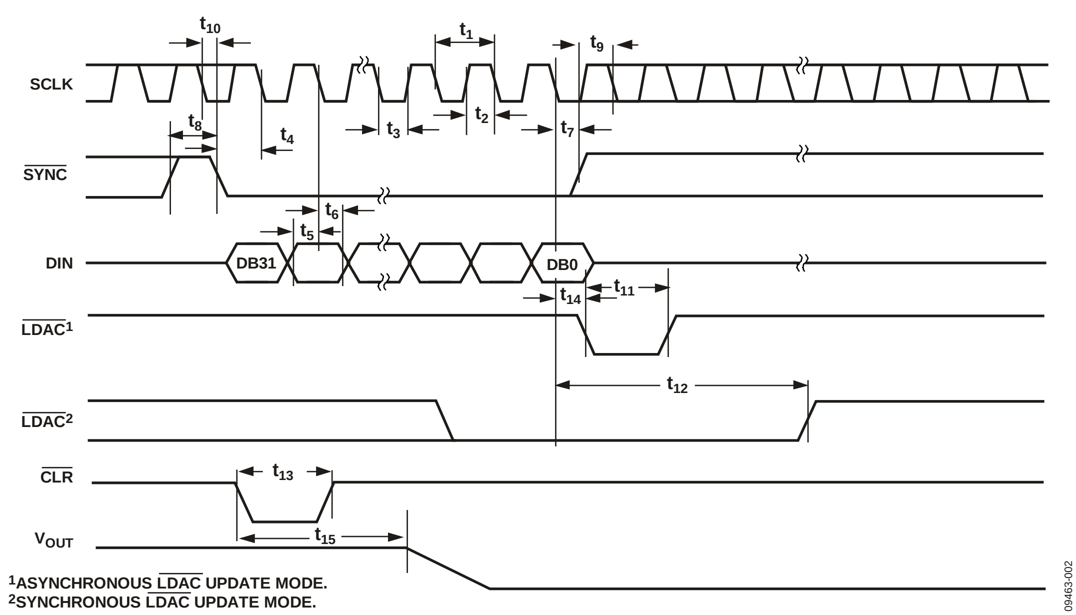

Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\,MAX}$)	150°C
TSSOP Package	
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb-Free	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

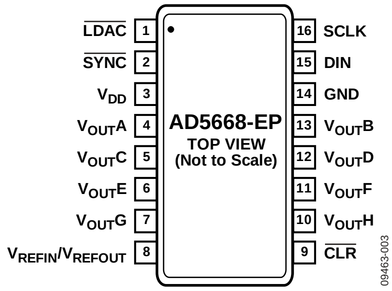

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	$\overline{\text{LDAC}}$	Active Low Control Input. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to update simultaneously. Alternatively, this pin can permanently be tied low.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. This device can be operated from 2.7 V to 5.5 V, and it is recommended the supply be decoupled with a 10 μF capacitor in parallel with a 0.1 μF capacitor to GND.
4	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	$V_{OUT}E$	Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
7	$V_{OUT}G$	Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
8	V_{REFIN}/ V_{REFOUT}	Common Pin for Reference Input and Reference Output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is a reference input.
9	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register: zero, midscale, or full-scale. Default setting clears the output to 0 V.
10	$V_{OUT}H$	Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
11	$V_{OUT}F$	Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
12	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
13	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
14	GND	Ground Reference Point for All Circuitry on the Device.
15	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
16	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

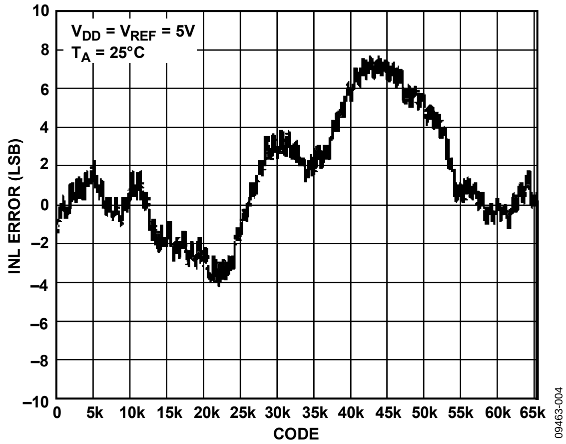

Figure 4. INL—External Reference

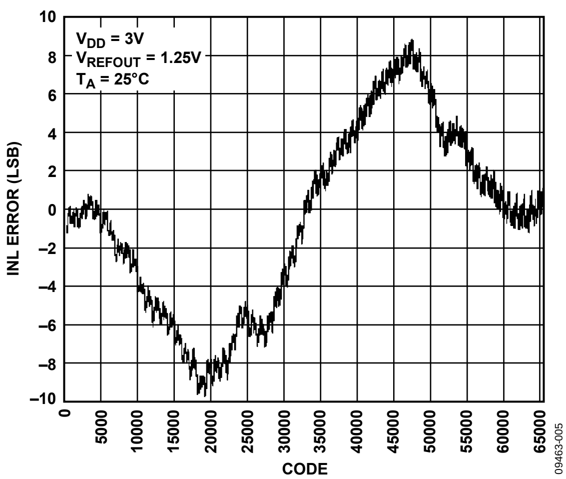

Figure 5. INL

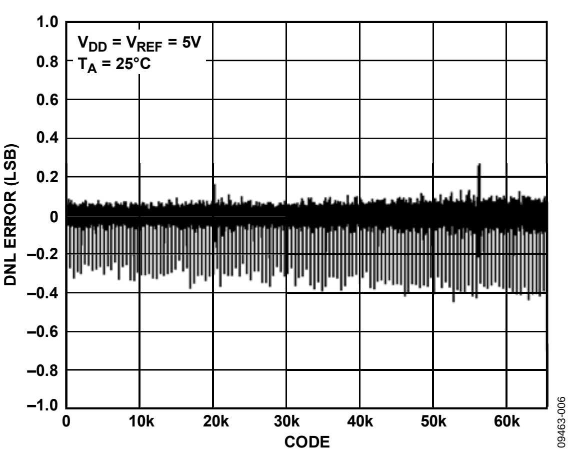

Figure 6. DNL—External Reference

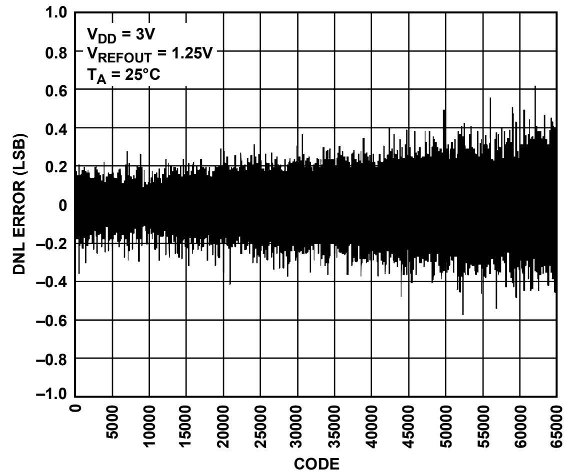

Figure 7. DNL

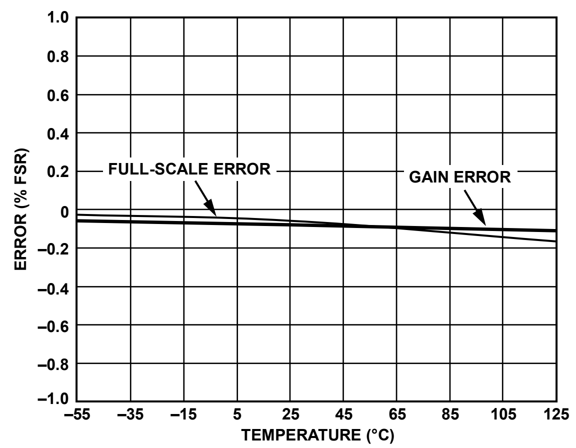

Figure 8. Gain Error and Full-Scale Error vs. Temperature

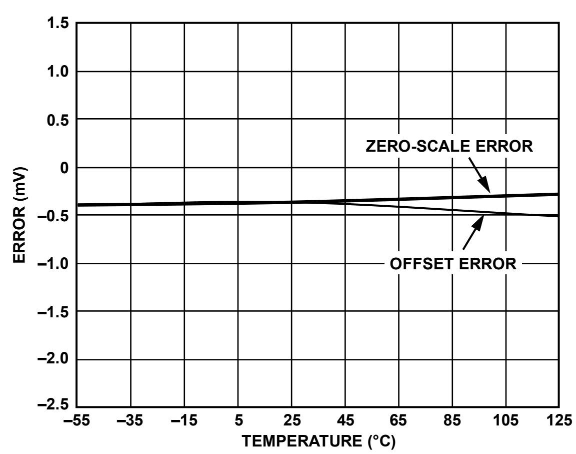

Figure 9. Zero-Scale Error and Offset Error vs. Temperature

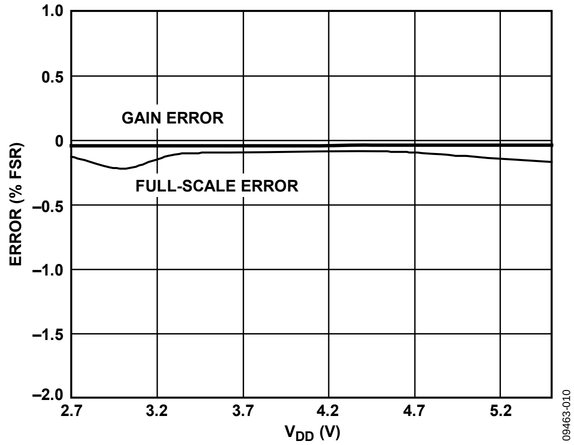

Figure 10. Gain Error and Full-Scale Error vs. Supply Voltage (V_{DD})

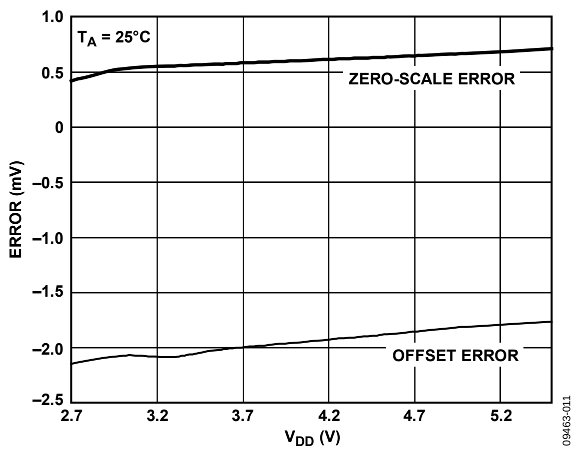

Figure 11. Zero-Scale Error and Offset Error vs. Supply Voltage (V_{DD})

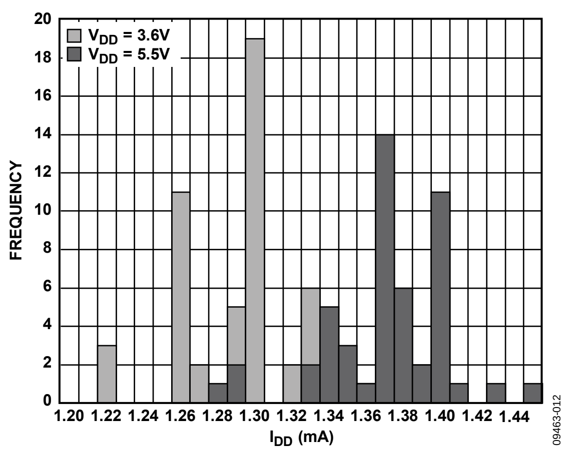

Figure 12. I_{DD} Histogram with External Reference

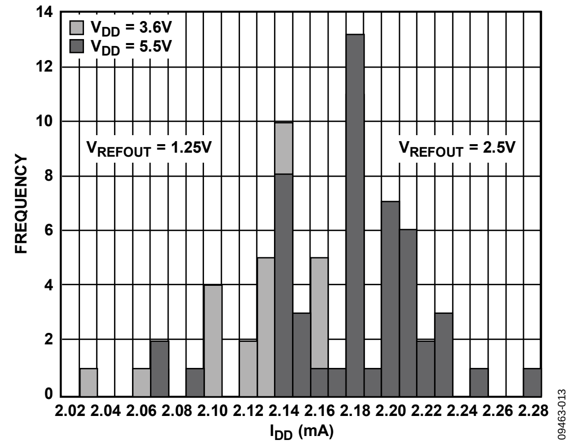

Figure 13. I_{DD} Histogram with Internal Reference

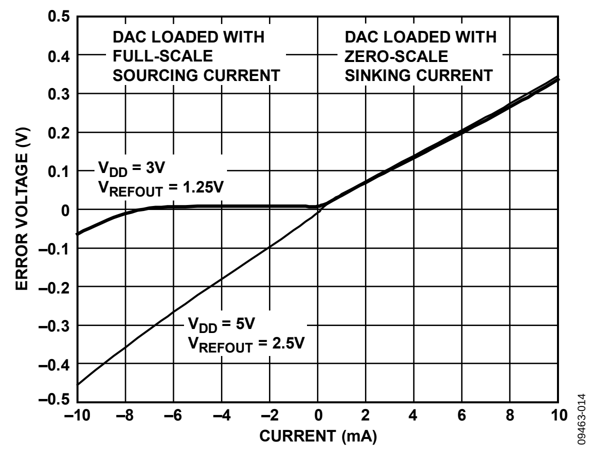

Figure 14. Headroom at Rails vs. Source and Sink

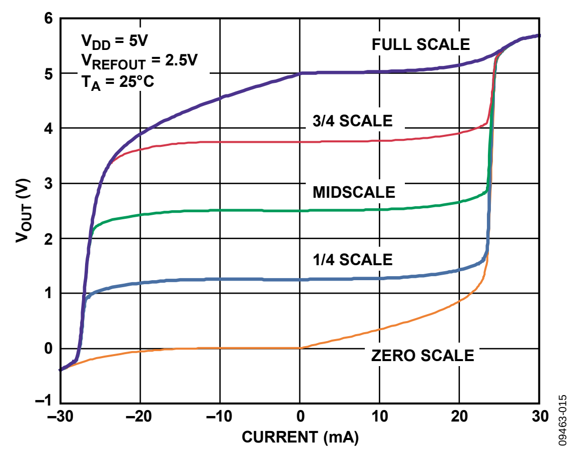

Figure 15. Source and Sink Capability

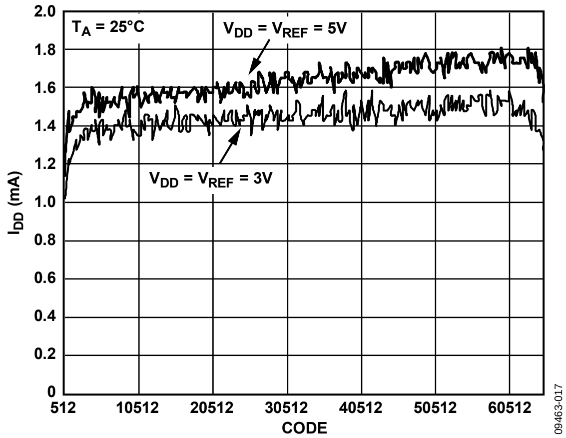

Figure 16. Supply Current (I_{DD}) vs. Code

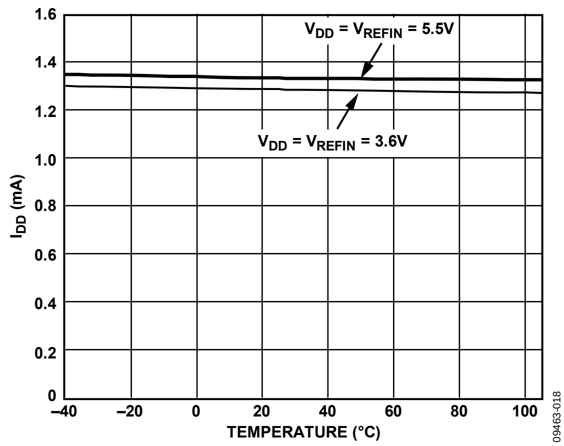

Figure 17. Supply Current (I_{DD}) vs. Temperature

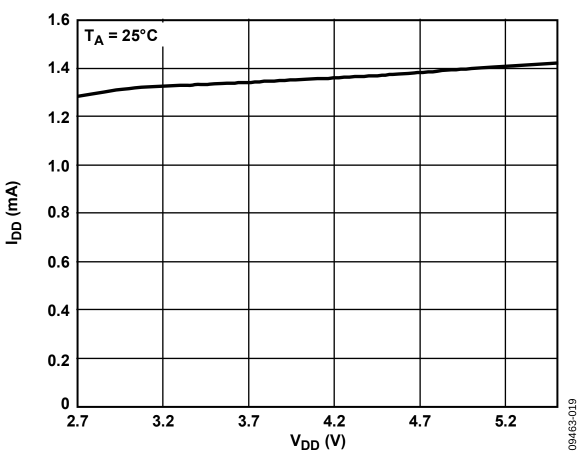

Figure 18. Supply Current (I_{DD}) vs. Supply Voltage (V_{DD})

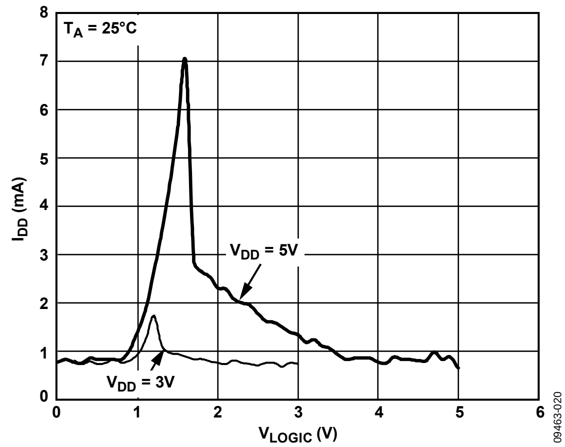

Figure 19. Supply Current (I_{DD}) vs. Logic Input Voltage (V_{LOGIC})

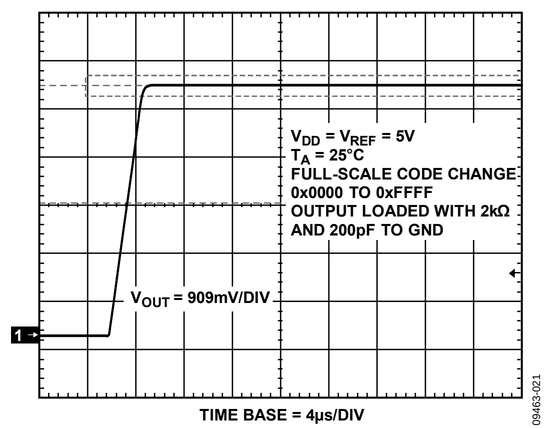

Figure 20. Full-Scale Settling Time, 5 V

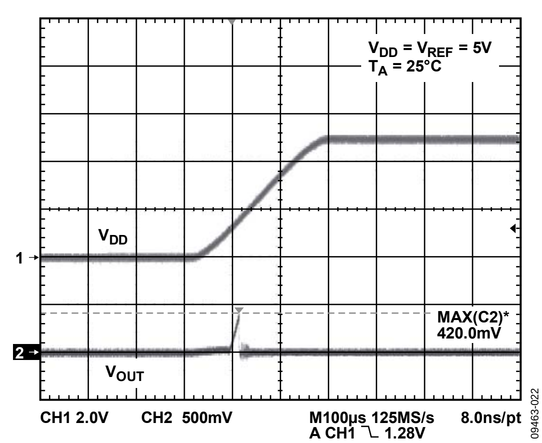

Figure 21. Power-On Reset to 0 V

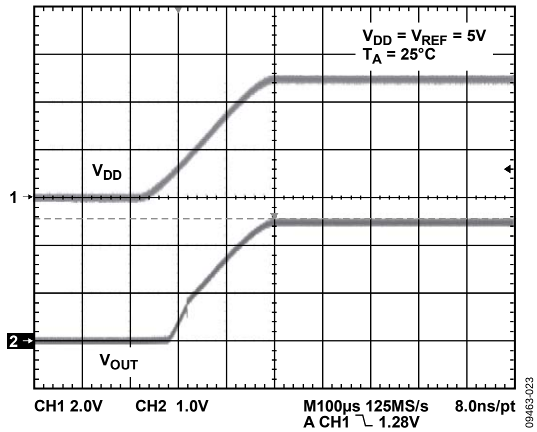

Figure 22. Power-On Reset to Midscale

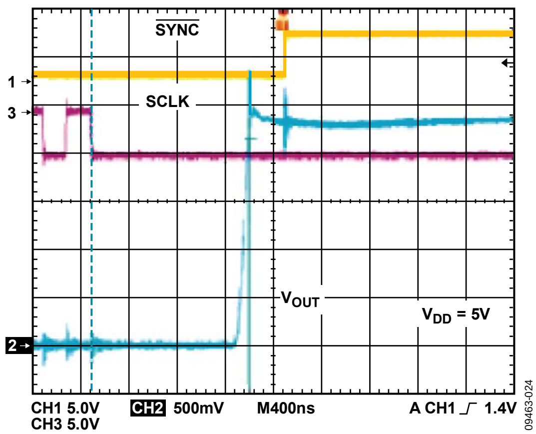

Figure 23. Exiting Power-Down to Midscale

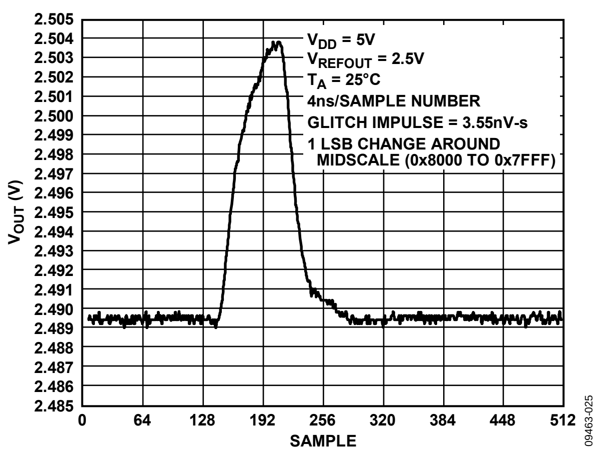

Figure 24. Digital-to-Analog Glitch Impulse (Negative)

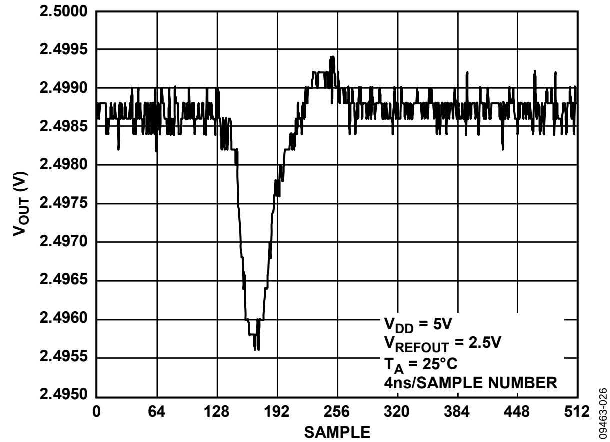

Figure 25. Analog Crosstalk

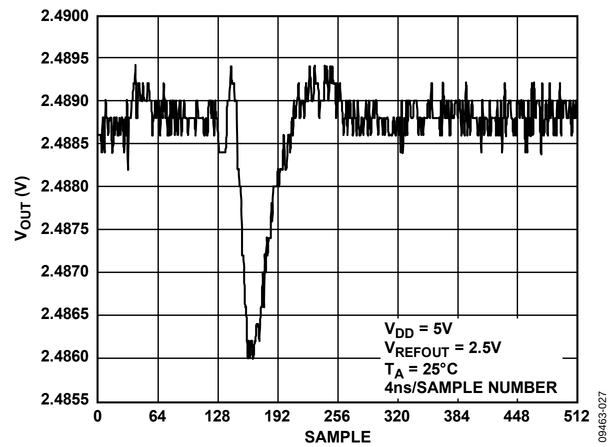

Figure 26. DAC-to-DAC Crosstalk

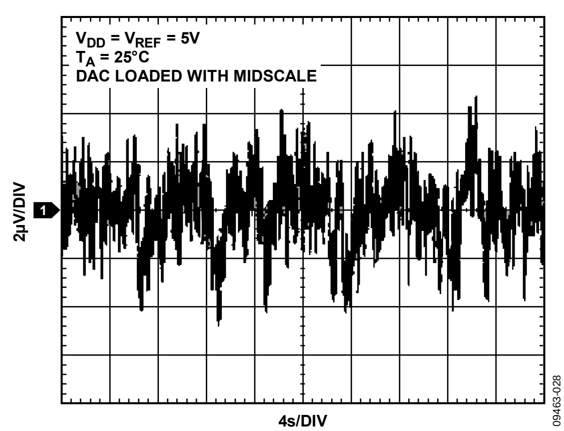

Figure 27. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

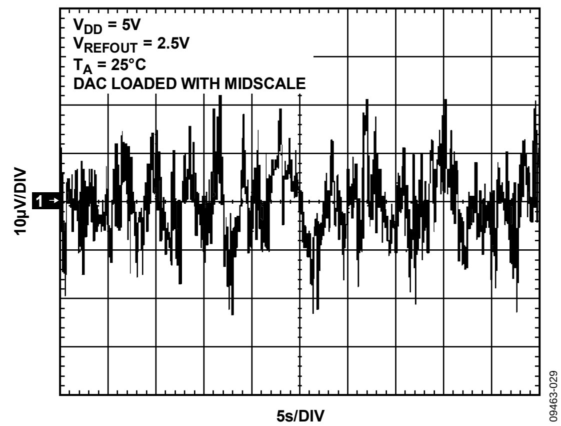

Figure 28. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

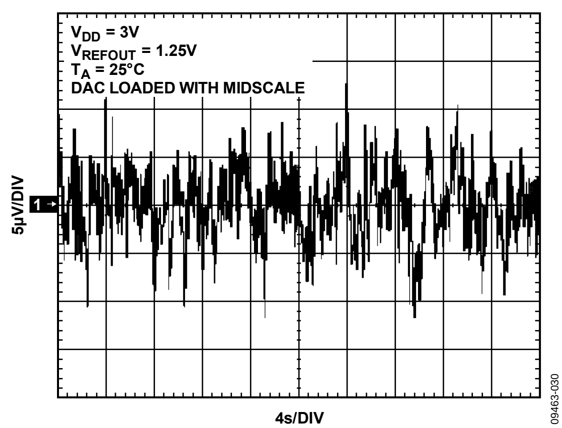

Figure 29. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

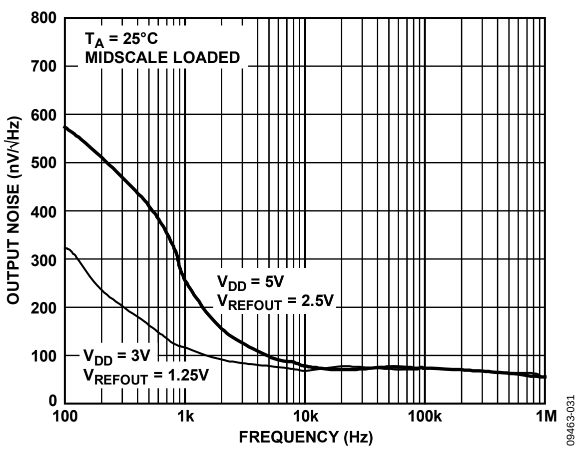

Figure 30. Noise Spectral Density, Internal Reference

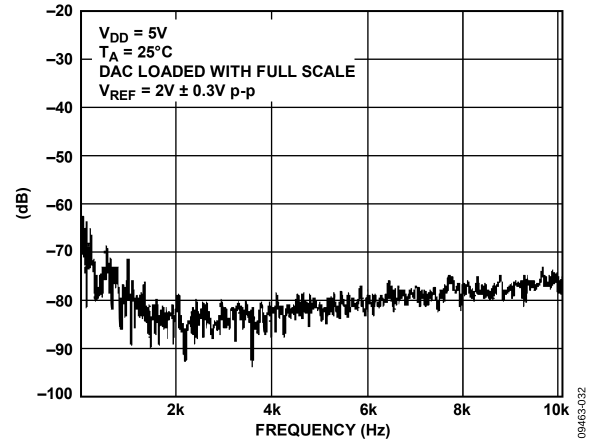

Figure 31. Total Harmonic Distortion

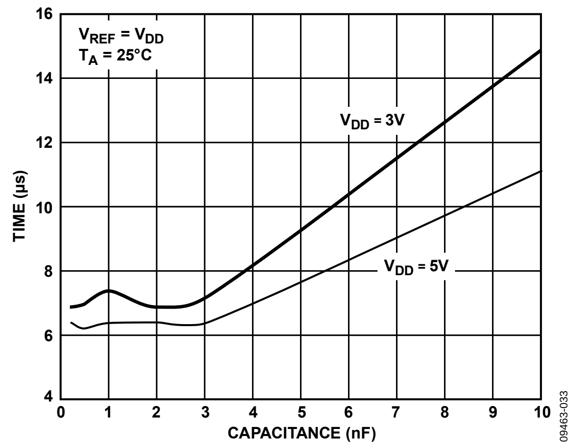

Figure 32. Settling Time vs. Capacitive Load

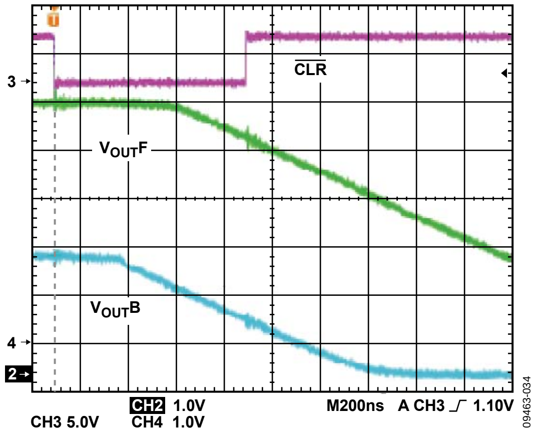

Figure 33. Hardware $\overline{CLR}$

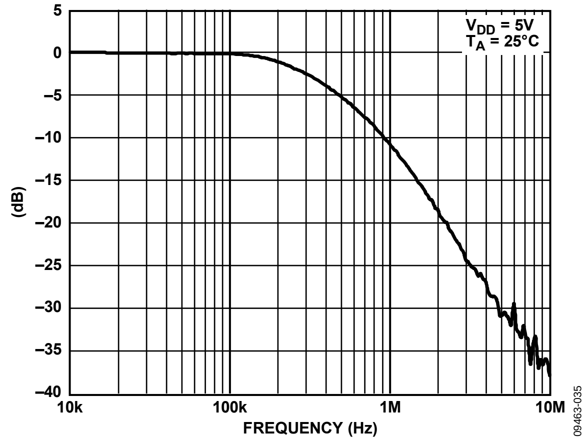

Figure 34. Multiplying Bandwidth

OUTLINE DIMENSIONS

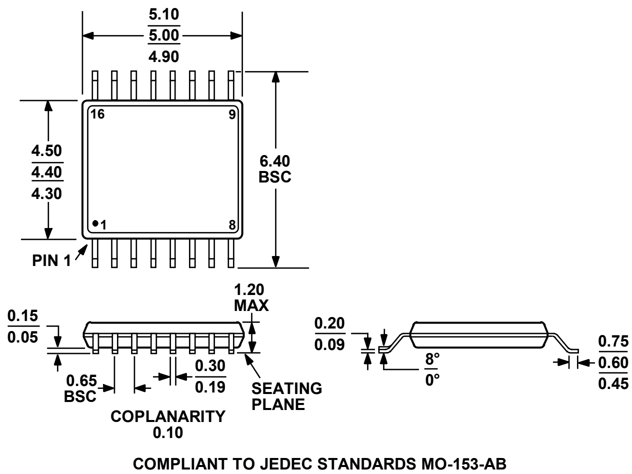

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Power-On Reset to Code	Accuracy LSB (INL)	Internal Reference (V)	Temperature Range	Package Description	Package Option
AD5668SRU-EP-1	Zero	±21	1.25	−55°C to +125°C	16-Lead TSSOP	RU-16
AD5668SRU-EP-1RL7	Zero	±21	1.25	−55°C to +125°C	16-Lead TSSOP	RU-16
AD5668SRUZ-EP-1	Zero	±21	1.25	−55°C to +125°C	16-Lead TSSOP	RU-16
AD5668SRUZ-EP-1RL7	Zero	±21	1.25	−55°C to +125°C	16-Lead TSSOP	RU-16

[1] Z= RoHS Compliant Part.

D09463-0-1/18(B)