TPIC6C596 Power Logic 8-Bit Shift Register

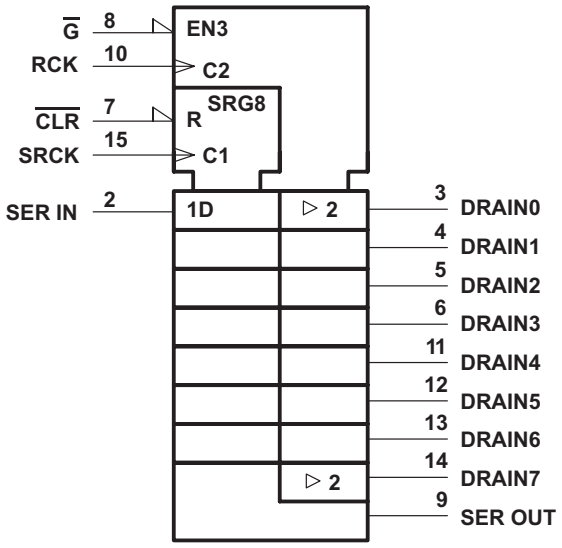
1 Features

- Low $R_{DS(on)}$, 7 Ω (Typical)
- Avalanche Energy, 30 mJ
- Eight Power DMOS Transistor Outputs of 100-mA Continuous Current
- 250-mA Current Limit Capability
- ESD Protection, 2500 V
- Output Clamp Voltage, 33 V
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption

2 Applications

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls
- Automotive Relay or Solenoids Drivers

Logic Symbol



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

3 Description

The TPIC6C596 device is a monolithic, medium-voltage, low-current, 8-bit shift register designed for use in systems that require relatively moderate load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other low-current or medium-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear ($\overline{CLR}$) is high. When $\overline{CLR}$ is low, all registers in the device are cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability.

The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 33 V and 100 mA continuous sink-current capability. Each output provides a 250-mA maximum current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2500 V of ESD protection when tested using the human body model and the 200-V machine model.

The TPIC6C596 device is characterized for operation over the operating case temperature range of −40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPIC6C596	SOIC (16)	9.90 mm × 3.91 mm
	PDIP (16)	19.30 mm × 6.35 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

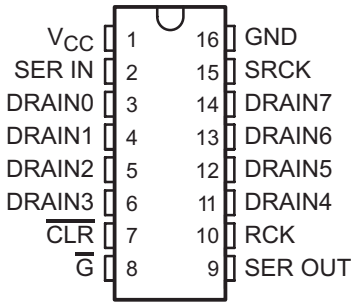
4 Revision History

Changes from Revision C (April 2005) to Revision D **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

D, N, or PW Packages
16-Pin SOIC, PDIP, and TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLR	7	I	Shift register clear, active-low
DRAIN0	3	O	Open-drain output
DRAIN1	4	O	Open-drain output
DRAIN2	5	O	Open-drain output
DRAIN3	6	O	Open-drain output
DRAIN4	11	O	Open-drain output
DRAIN5	12	O	Open-drain output
DRAIN6	13	O	Open-drain output
DRAIN7	14	O	Open-drain output
G	8	I	Output enable, active-low
GND	16	—	Power ground
RCK	10	I	Register clock
SER IN	2	I	Serial data input
SER OUT	9	O	Serial data output
SRCK	15	I	Shift register clock
VCC	1	I	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage (2)	–0.3	7	V
V_I	Logic input voltage	–0.3	7	V
V_{DS}	Power DMOS drain-to-source voltage (3)	–0.3	33	V
	Continuous source-to-drain diode anode current		250	mA
	Pulsed source-to-drain diode anode current (4)		500	mA
I_D	Pulsed drain current, each output, all outputs on, T_C = 25°C (4)		250	mA
I_D	Continuous drain current, each output, all outputs on, T_C = 25°C (4)		100	mA
I_{DM}	Peak drain current single output, T_C = 25°C (4)		250	mA
E_{AS}	Single-pulse avalanche energy (see Figure 11)		30	mJ
I_{AS}	Avalanche current (5)		200	mA
	Continuous total dissipation	See *Thermal Information*		
T_C	Operating case temperature	–40	125	°C
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Each power DMOS source is internally connected to GND.
(4) Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
(5) DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 1.5 H, I_{AS} = 200 mA (see Figure 11).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Logic supply voltage	4.5		5.5	V
V_{IH}	High-level input voltage	0.85 V_{CC}			V
V_{IL}	Low-level input voltage			0.15 V_{CC}	V
	Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V, all outputs on (1) (2) (see Figure 7)			250	mA
t_{su}	Setup time, SER IN high before SRCKM ↑ (see Figure 9)	15			ns
t_h	Hold time, SER IN high after SRCKM ↑, (see Figure 9)	15			ns
t_w	Pulse duration (see Figure 9)	40			ns
T_C	Operating case temperature	–40		125	°C

(1) Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
(2) Technique should limit $T_J - T_C$ to 10°C maximum.

6.4 Thermal Information

THERMAL METRIC(1)		TPIC6C596			UNIT
		PW (TSSOP)	D (SOIC)	N (PDIP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.7	83.7	51.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	45.1	38.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	41.2	31.4	
ψ_{JT}	Junction-to-top characterization parameter	5	12.1	23.6	
ψ_{JB}	Junction-to-board characterization parameter	54.2	40.9	31.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA		33	37		V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA			0.85	1.2	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = − 20 µA,	V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = − 4 mA,	V_{CC} = 4.5 V	4	4.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 µA,	V_{CC} = 4.5 V		0.005	0.1	V
		I_{OL} = 4 mA,	V_{CC} = 4.5 V		0.3	0.5	
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$			1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0			–1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off		20	200	µA
			All outputs on		150	500	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, All outputs off,	C_L = 30 pF, See Figure 9 and Figure 2		1.2	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, T_C = 85°C	$I_N = I_D$, See (1)(2)(3)		90		mA
I_{DSX}	OFF-state drain current	V_{DS} = 30 V,	V_{CC} = 5.5 V		0.1	0.2	µA
		V_{DS} = 30 V T_C = 125°C	V_{CC} = 5.5 V		0.15	0.3	
$r_{DS(on)}$	Static drain-source ON-state resistance	I_D = 50 mA, V_{CC} = 4.5 V	See (1) and (2) and Figure 3 and Figure 4		6.5	9	Ω
		I_D = 50 mA, T_C = 125°C, V_{CC} = 4.5 V			9.9	12	
		I_D = 100 mA, V_{CC} = 4.5 V			9.9	10	

(1) Technique should limit $T_J - T_C$ to 10°C maximum.
(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
(3) Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

6.6 Switching Characteristics

V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 75 mA, See Figure 5, Figure 8 and Figure 9		80		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			50		ns
t_r	Rise time, drain output			100		ns
t_f	Fall time, drain output			80		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30 pF, I_D = 75 mA, See Figure 9		15		ns
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 75 mA(1)			10	MHz
t_a	Reverse-recovery-current rise time	I_F = 100 mA, di/dt = 10 A/µs(2) (3), See Figure 10		100		ns
t_{rr}	Reverse-recovery time			120		

(1) This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK → SEROUT propagation delay and setup time plus some timing margin.
(2) Technique should limit $T_J - T_C$ to 10°C maximum.
(3) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

6.7 Typical Characteristics

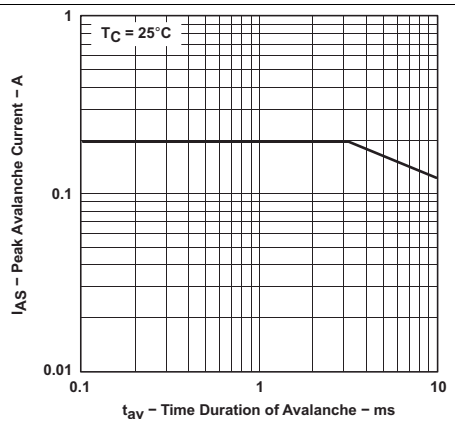


Figure 1. Peak Avalanche Current vs Time Duration of Avalanche

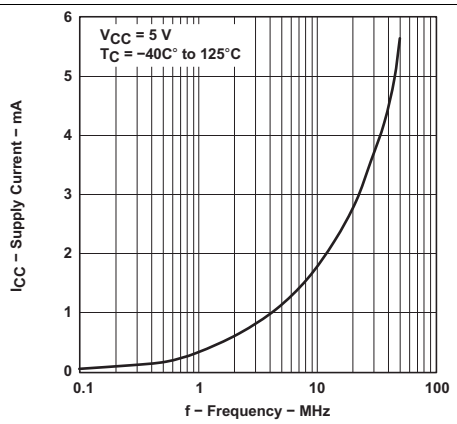
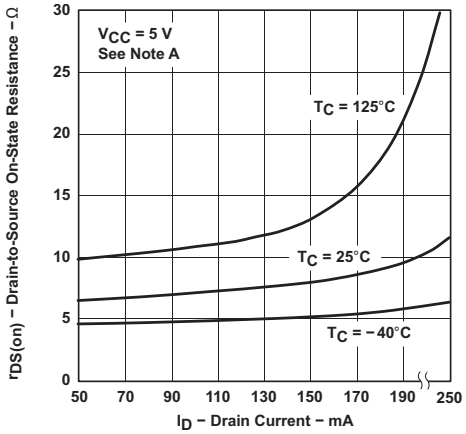


Figure 2. Supply Current vs Frequency



Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 3. Drain-to-Source ON-State Resistance vs Drain Current

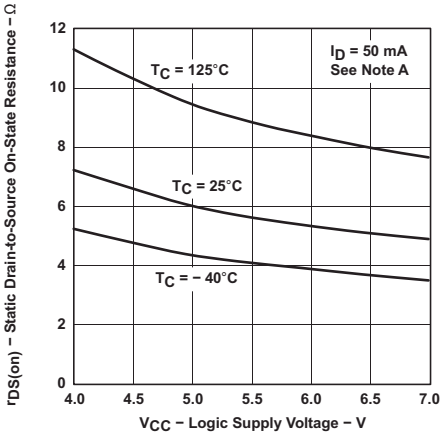
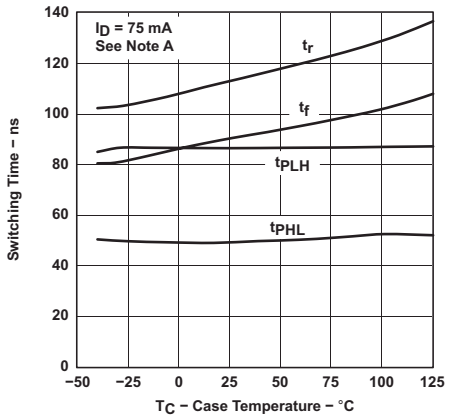


Figure 4. Static Drain-to-Source ON-State Resistance vs Logic Supply Voltage



Technique should limit $T_J - T_C$ to 10°C maximum

Figure 5. Switching Time vs Case Temperature

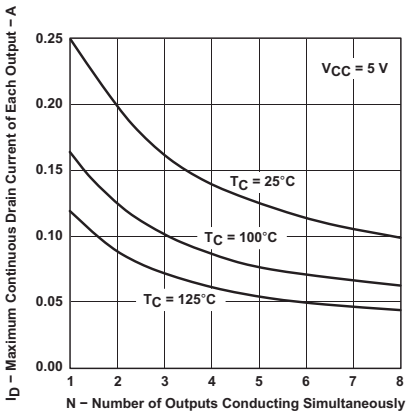


Figure 6. Maximum Continuous Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

Typical Characteristics (continued)

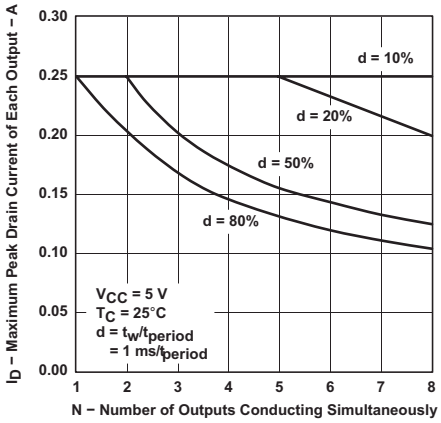
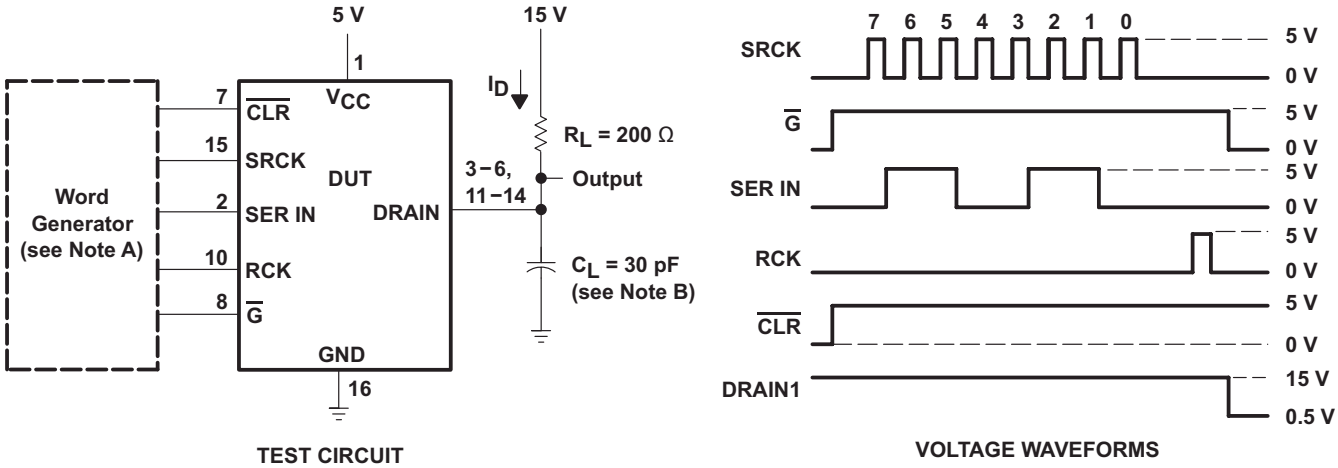


Figure 7. Maximum Peak Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

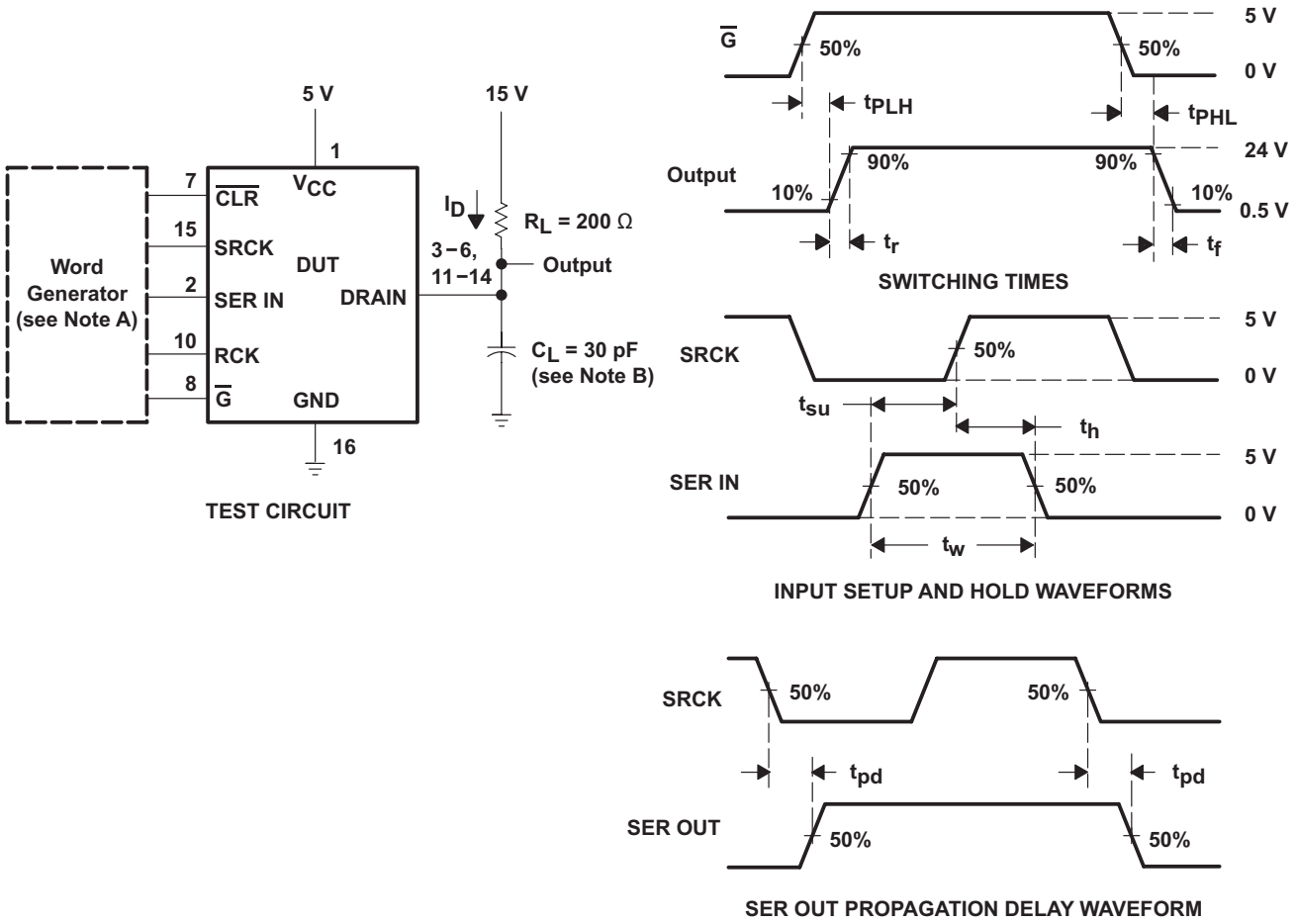
7 Parameter Measurement Information



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 8. Resistive-Load Test Circuit and Voltage Waveforms

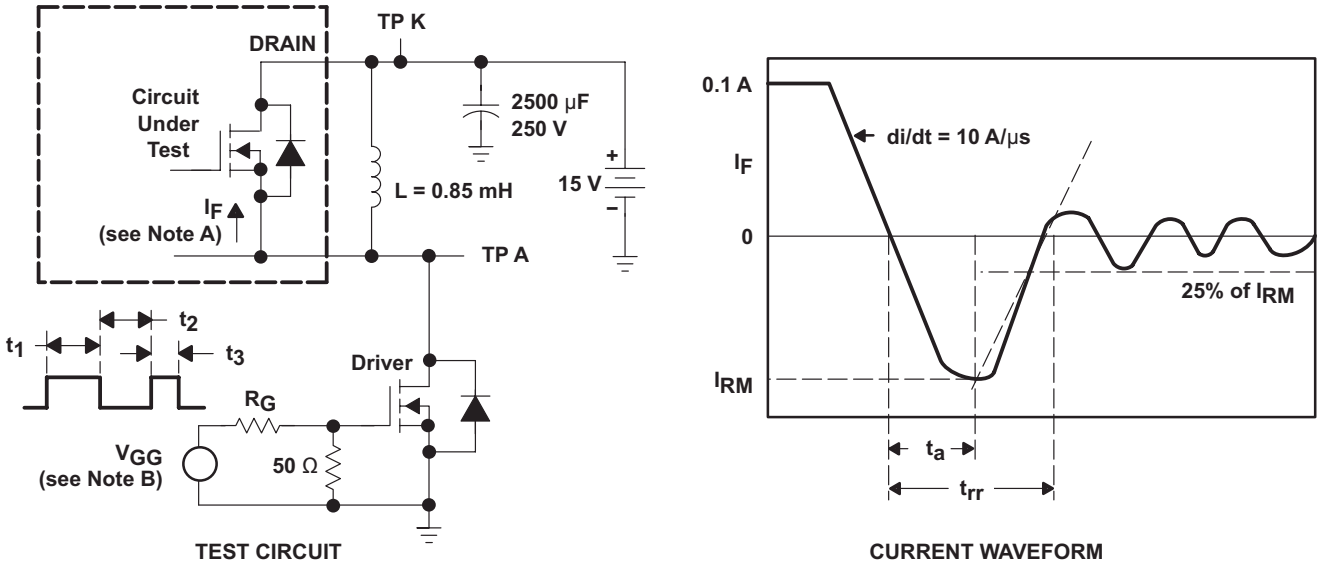
Parameter Measurement Information (continued)



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 9. Test Circuit, Switching Times, and Voltage Waveforms

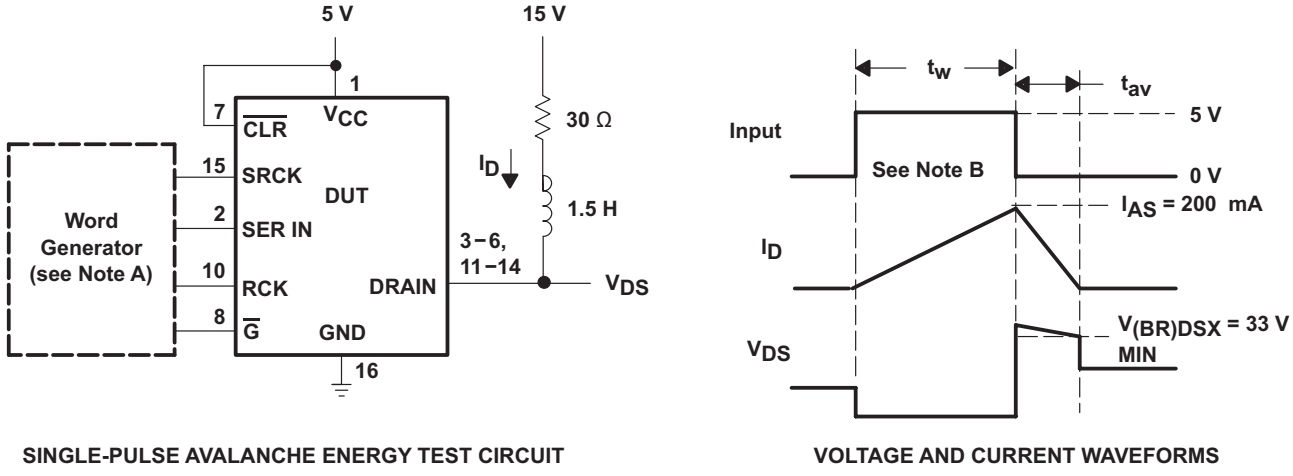
Parameter Measurement Information (continued)



NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

B. The V_{GG} amplitude and R_G are adjusted for di/dt = 10 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.1 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.

Figure 10. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, Z_O = 50 Ω.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 200 mA.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 30 mJ.

Figure 11. Single-Pulse Avalanche Energy Test Circuit and Waveforms

8 Detailed Description

8.1 Overview

The TPIC6C596 device is a monolithic, medium-voltage, low-current 8-bit shift register designed to drive relatively moderate load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection, so it can also drive relays, solenoids, and other low-current or medium-voltage loads.

8.2 Functional Block Diagram

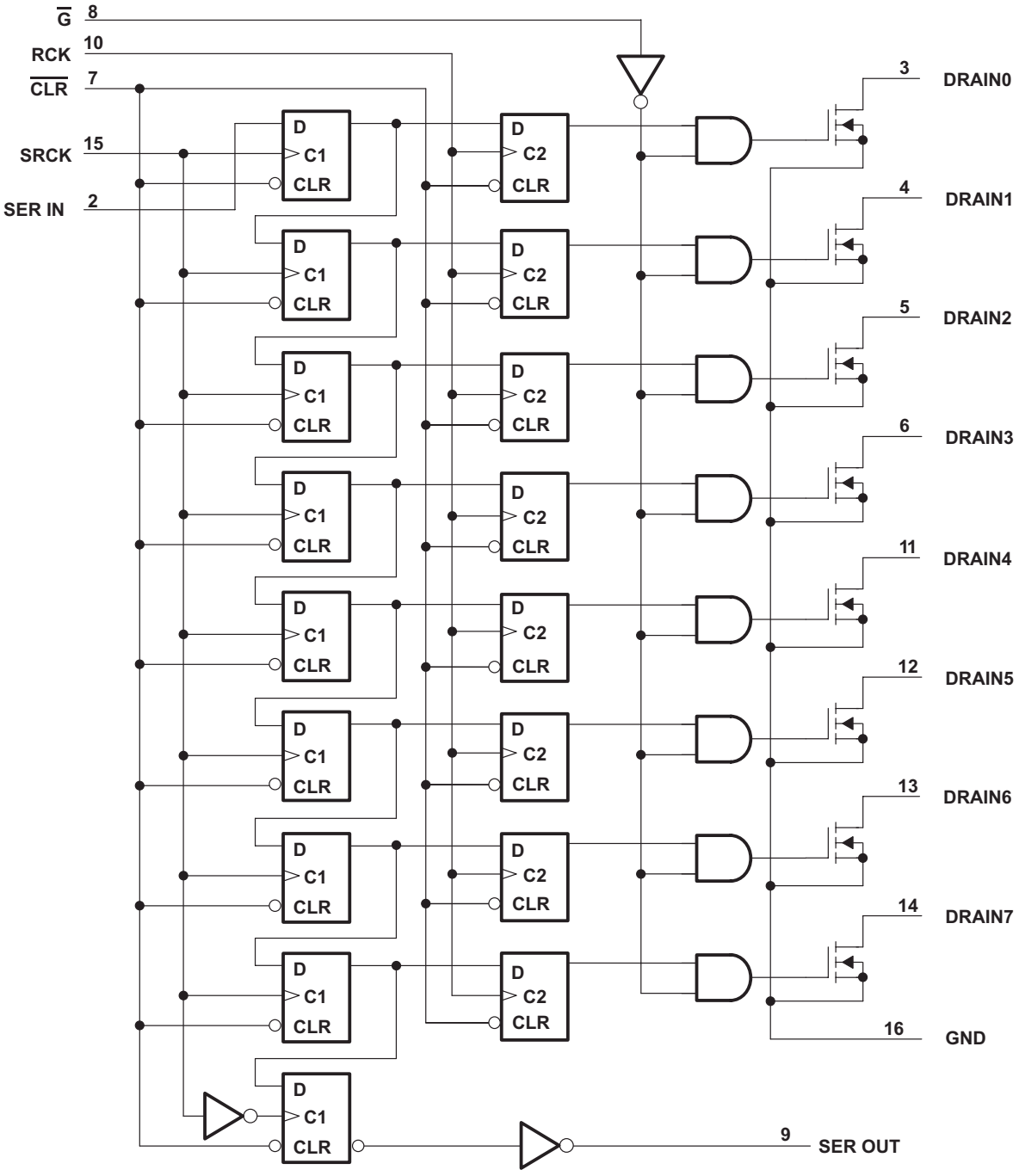


Figure 12. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Serial-In Interface

The TPIC6C596 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear (CLR) is high.

8.3.2 Clear Register

A logical low on $\overline{CLR}$ clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.3 Output Control

Holding the output enable ($\overline{G}$) high holds all data in the output buffers low, and all drain outputs are off. Holding $\overline{G}$ low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sink-current. This pin can also be used for global PWM dimming.

8.4 Device Functional Modes

8.4.1 Operation With V(VIN) < 4.5 V (Minimum $V_{(VIN)}$)

This device works normally during 4.5 V ≤ V(VIN) ≤ 5.5 V, when operation voltage is lower than 4.5 V. The behavior of device can't be ensured, including communication interface and current capability.

8.4.2 Operating With 5.5 V < V(VIN) < 6 V

This device works normally during this voltage range, but reliability issues may occurs while the device works for a long time in this voltage range.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPIC6C596 device is a serial-in parallel-out, Power+LogicE 8-bit shift register with low-side switch DMOS outputs rating of a 100 mA per channel. The device is designed to drive resistive and inductive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The TPIC6C596 device is an enhancement of the TPIC6C595 device, where the shift register serial output (SER OUT) is clocked on the falling edge of the serial clock to provide additional hold-time in applications where several devices are cascaded.

9.1.1 Cascaded Application

The serial output (SEROUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. Connect the device (SEROUT) pin to the next device (SERIN) for daisy Chain. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

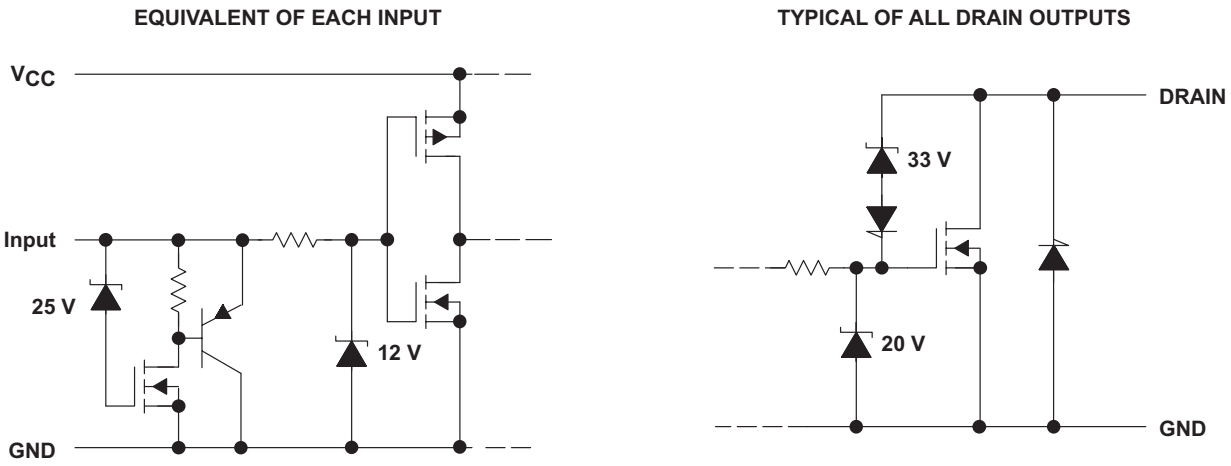


Figure 13. Schematic of Inputs and Outputs

9.2 Typical Application

The typical application of TPIC6C596 device is an automotive cluster driver. In this example, two TPIC6C596 power shift registers are cascaded and used to turn on LEDs in the cluster panel. In this case, the LED must be updated after all 16 bits of data have been loaded into the serial shift registers. The MCU outputs the data to the serial input (SER IN) while clocking the shift register clock (SRCK). After the 16th clock, a pulse to the register clock (RCK) transfers the data to the storage registers. If output enable ($\overline{G}$) is low, then the LEDs are turned on corresponding to the status word with ones being on and zeros off. With this simple scheme, MCU can use the SPI interface to turn on 16 LEDs using only two ICs as illustrated in Figure 14.

Typical Application (continued)

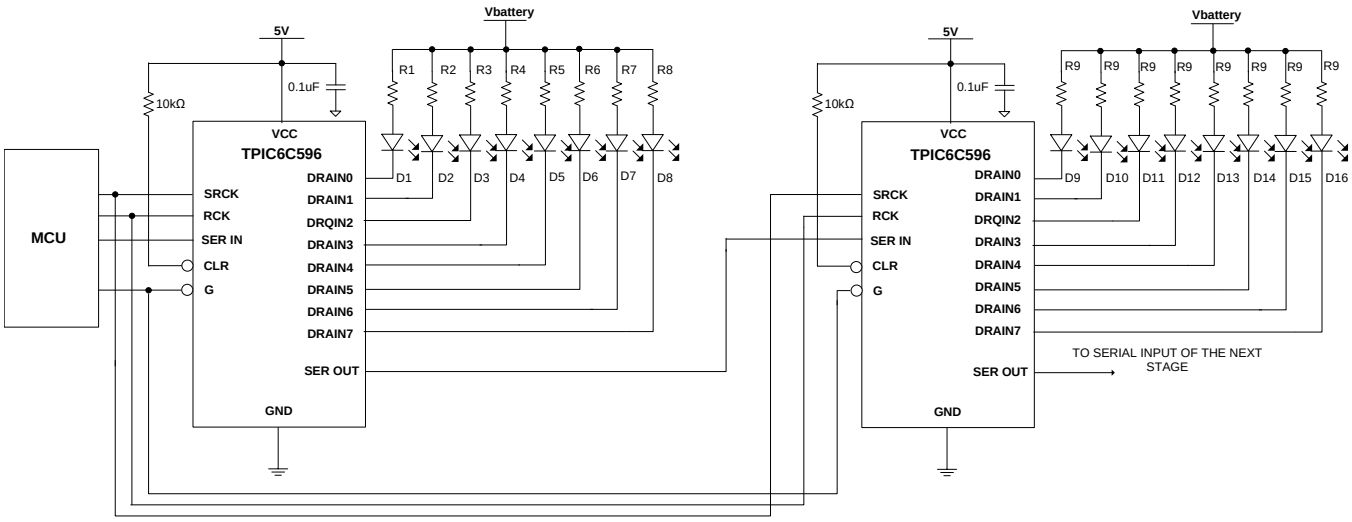


Figure 14. Typical Application Schematic

9.2.1 Design Requirements

Table 1 lists the design parameters for Figure 14.

Table 1. Design Parameters

DESIGN PARAMTER	EXAMPLE VALUE
Vsupply	9 to16 V
V (D1), V (D2), V (D3), V (D4), V (D5), V (D6),V (D7), V (D8)	2 V
V (D9), V (D10),V (D11), V (D12), V (D13), V (D14),V (D15), V (D16)	3.3 V
I (D1), I (D2), I (D3), I (D4), I (D5), I (D6),I (D7), I (D8)	20 mA when Vbattery is 12 V
I (D9), I (D10), I (D11), I (D12), I (D13), I (D14),I (D15), I (D16)	30 mA when Vbattery is 12 V

9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters. The designer must know the following:

- Vsupply: LED supply is connected directly to the car battery, which has a voltage range from 9 V to 16 V, or fixed voltage. This application connects to the battery directly.
- V(Dx): LED forward voltage
- I(Dx): LED setting current when battery is 12 V.

9.2.2.1 R1, R2, R3, R4, R5, R6, R7, R8 R1 = R2 = R3 = R4 = R5 = R6 = R7 = R8 = (Vsupply – V (Dx)) / I (Dx) = (12 V – 2 V) / 0.02 A = 500 Ω

When Vsupply is 9 V, I (D1) = I (D2) = I (D3) = I (D4) = I (D5) = I (D6) = I (D7) = I (D8) = (Vsupply – V(Dx)) / Rx = 14 mA.

When Vsupply is 16 V, I (D9) = I (D10) = I (D11) = I (D12) = I (D13) = I (D14) = I (D15) = I (D16) =(Vsupply – V(Dx)) / Rx= 43.8 mA.

NOTE

If designers can accept the current variation when battery voltage is changing, they can connect the device directly to the battery. If a designer need the less variation of current, they need to use the voltage regulator as supply voltage of LED, or change to constant current LED driver directly

9.2.3 Application Curve

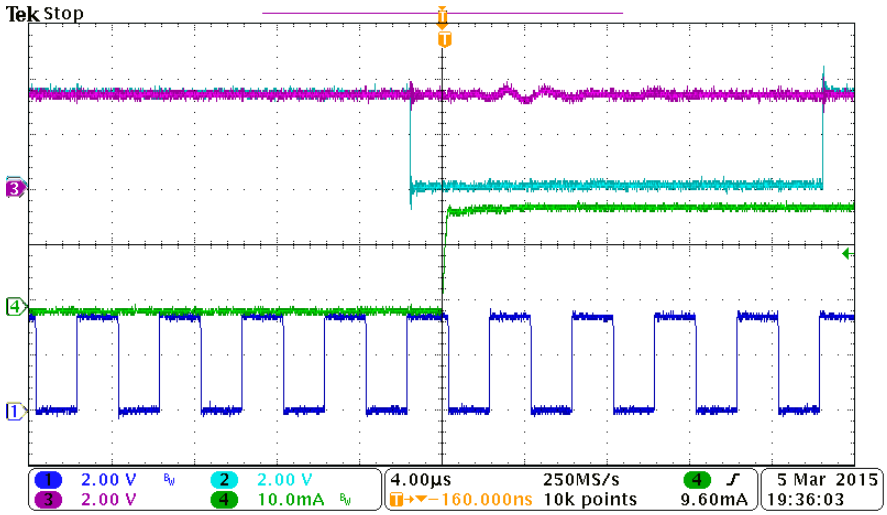


Figure 15. CH1 is SRCK, CH2 is RCK, CH3 is SER IN and CH4 is D1 Current

10 Power Supply Recommendations

The TPIC6C596 device is designed to operate from an input voltage supply range from 4.5 V and 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the VCC pin.

11 Layout

11.1 Layout Guidelines

There is no special layout requirement for the digital signal pin; the only requirement is placing the ceramic bypass capacitors near the corresponding pin. Because the TPIC6C596 device does not have a thermal shutdown protection function, to prevent thermal damage, T_J must be less than 150°C. If the total sink current is high, the power dissipation might be large. The devices are currently not available in the thermal pad package, so good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board, because the major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

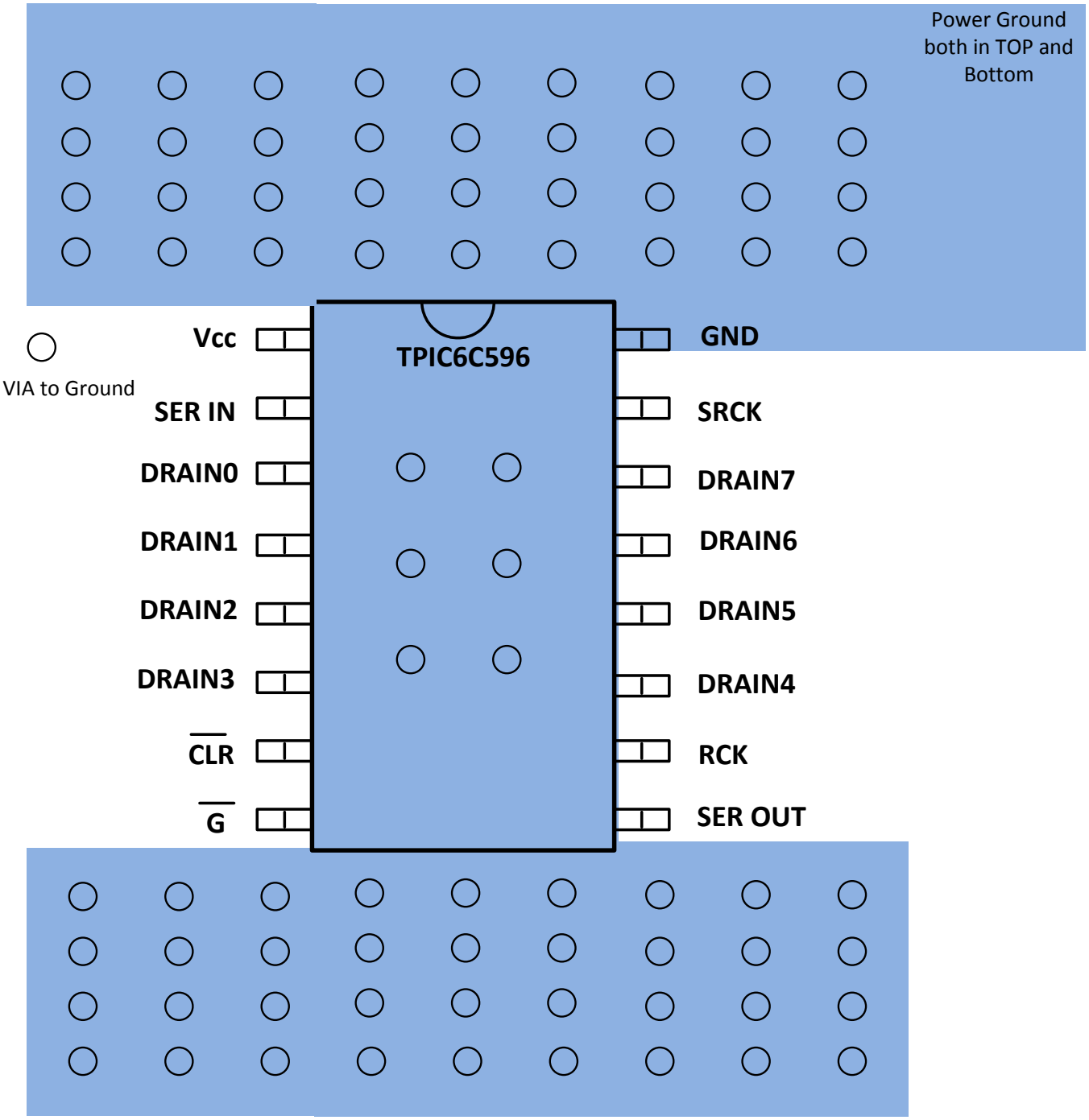
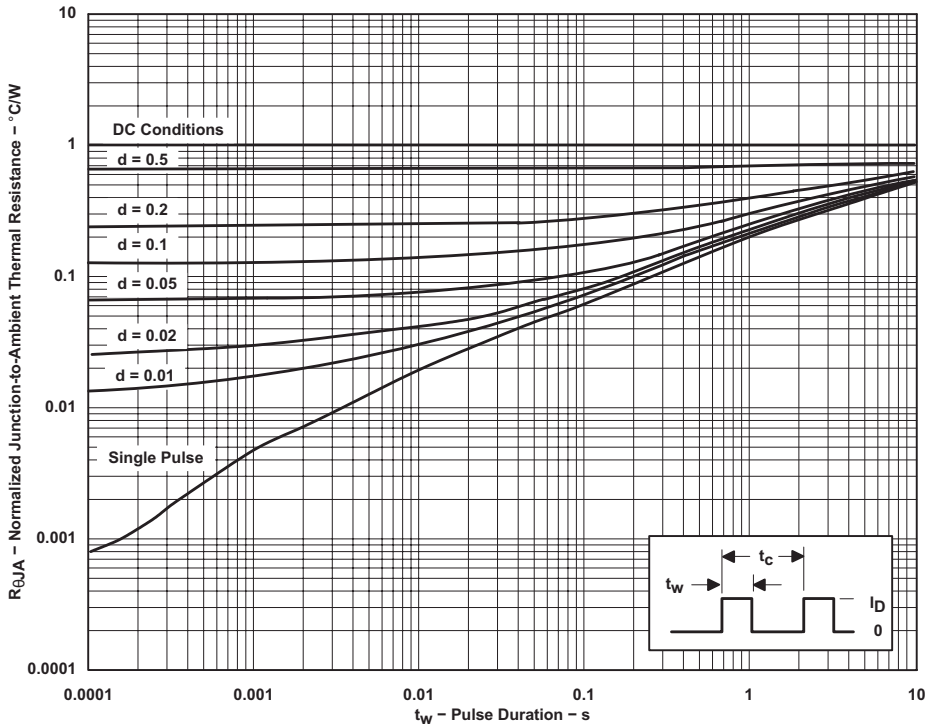


Figure 16. Recommended Layout Example

11.3 Thermal Considerations



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 17. D Package†, Normalized Junction-to-Ambient Thermal Resistance vs Pulse Duration

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC6C596D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6C596	Samples
TPIC6C596DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6C596	Samples
TPIC6C596DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6C596	Samples
TPIC6C596DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6C596	Samples
TPIC6C596DRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6C596Q	Samples
TPIC6C596N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 125	TPIC6C596	Samples
TPIC6C596PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6C596PW	Samples
TPIC6C596PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		6C596PW	Samples
TPIC6C596PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6C596PW	Samples
TPIC6C596PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		6C596PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

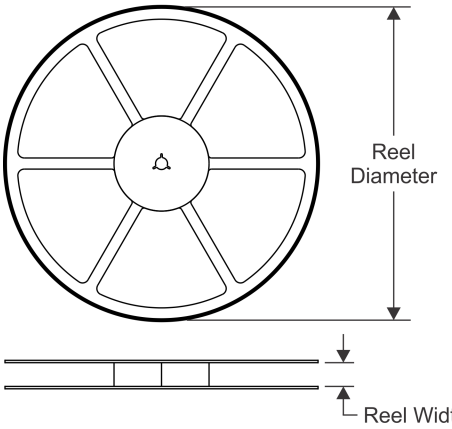
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

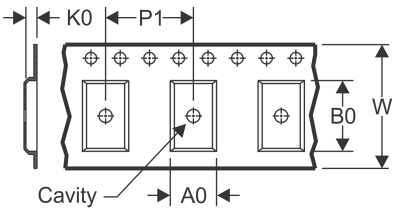
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

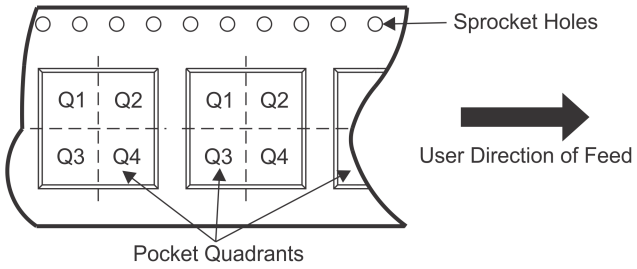


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

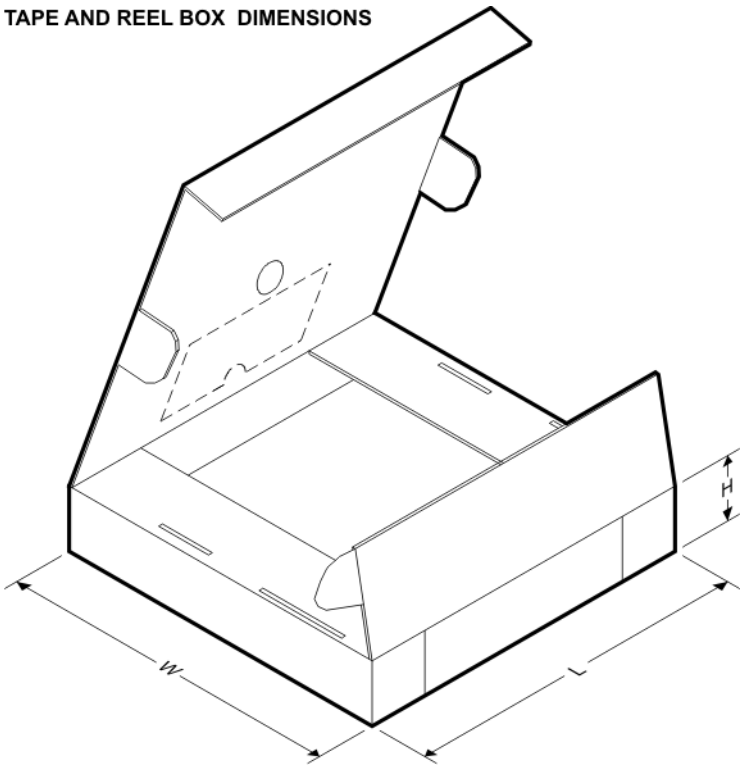
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6C596DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPIC6C596DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPIC6C596DRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPIC6C596PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPIC6C596PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

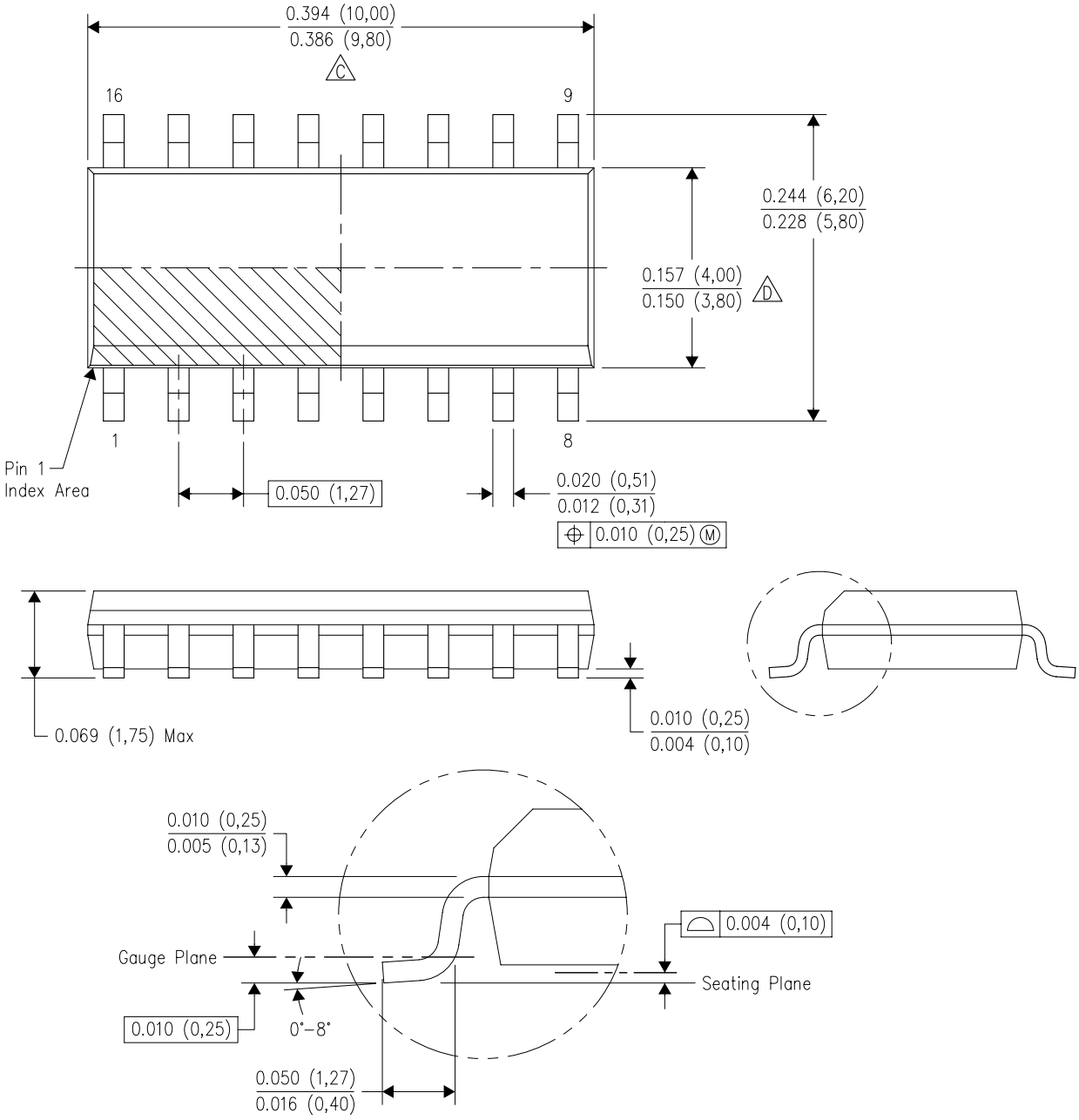
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

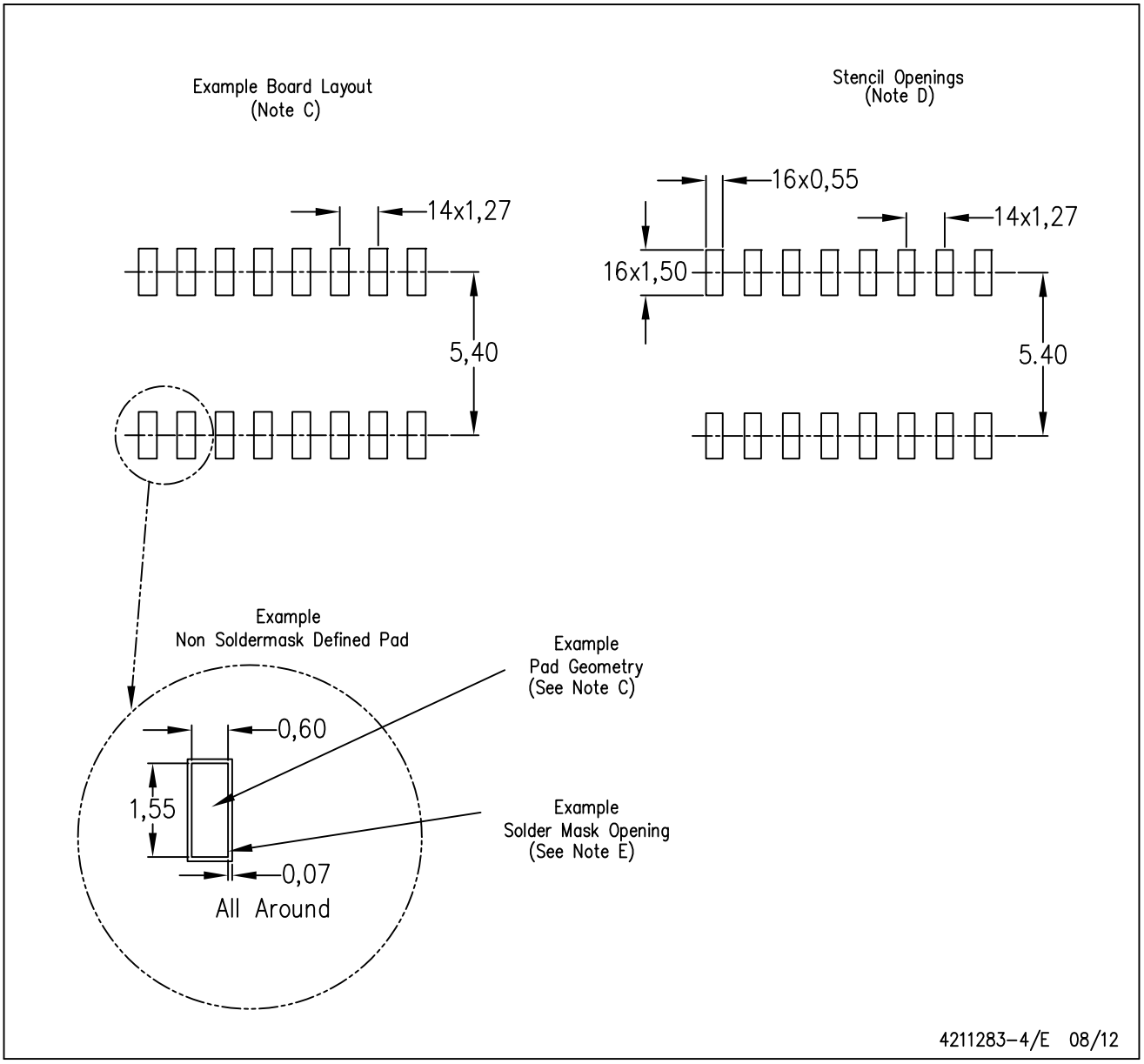
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6C596DR	SOIC	D	16	2500	367.0	367.0	38.0
TPIC6C596DRG4	SOIC	D	16	2500	350.0	350.0	43.0
TPIC6C596DRQ1	SOIC	D	16	2500	350.0	350.0	43.0
TPIC6C596PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
TPIC6C596PWRG4	TSSOP	PW	16	2000	350.0	350.0	43.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



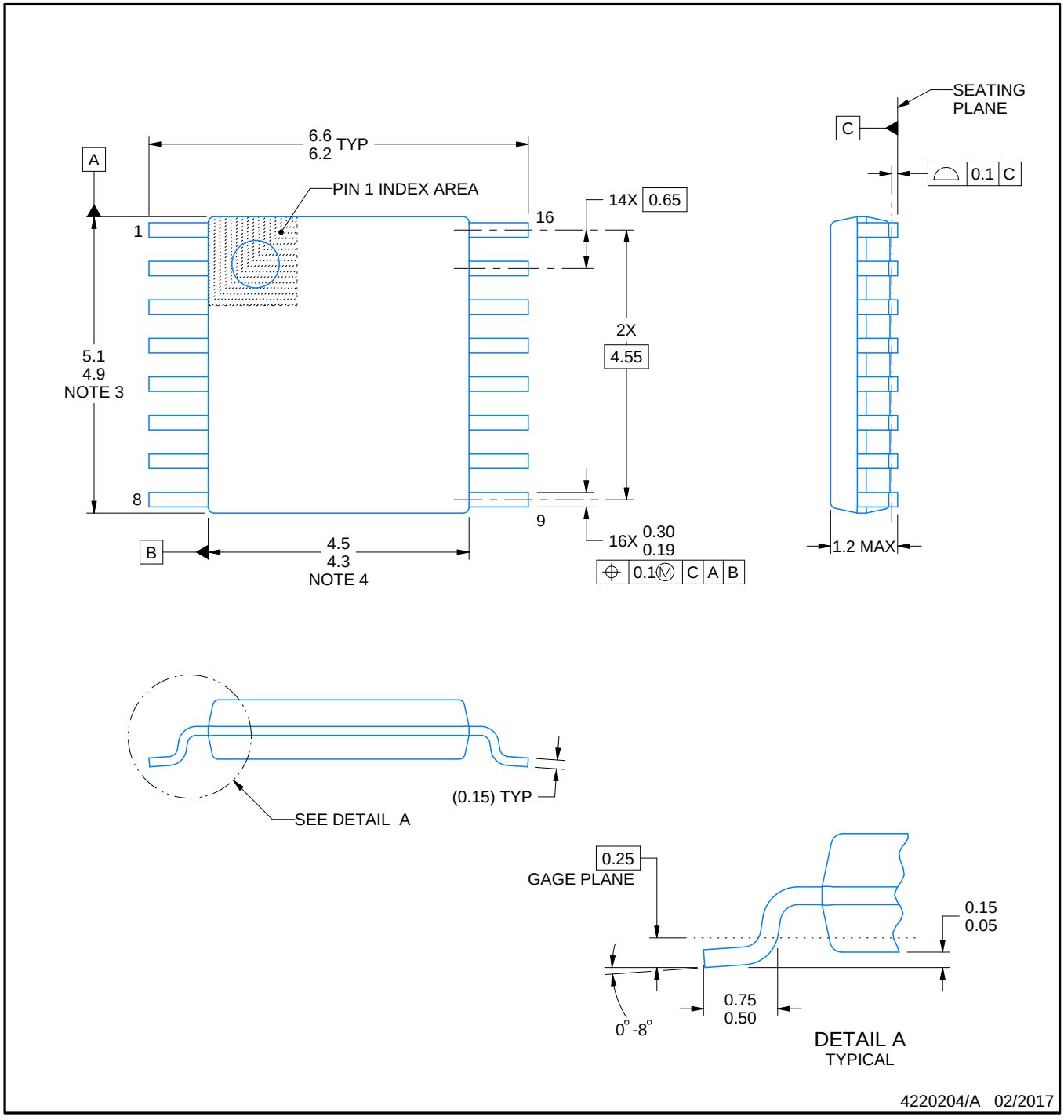
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

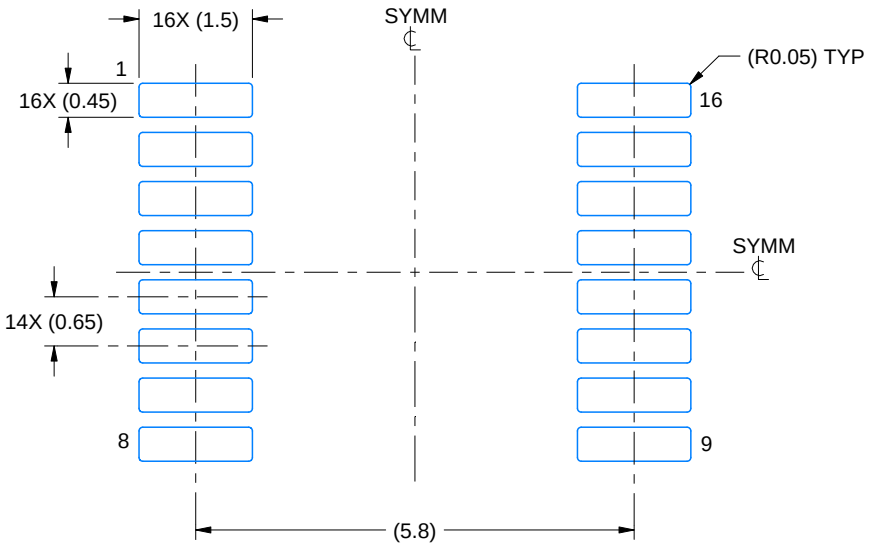
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

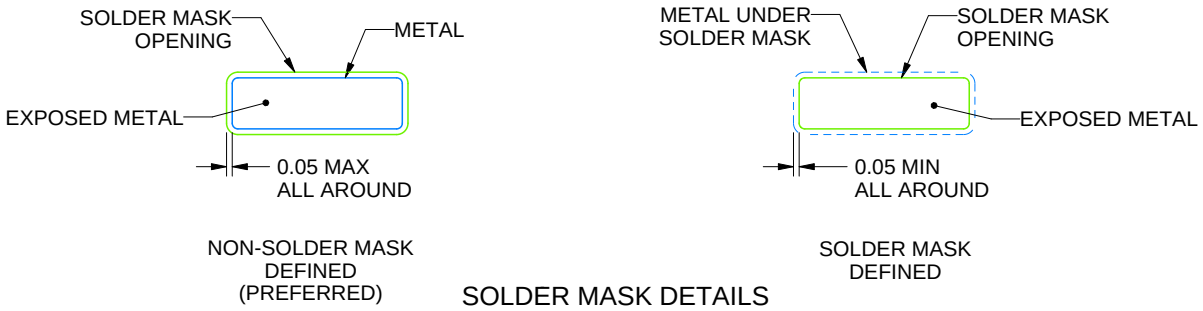


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

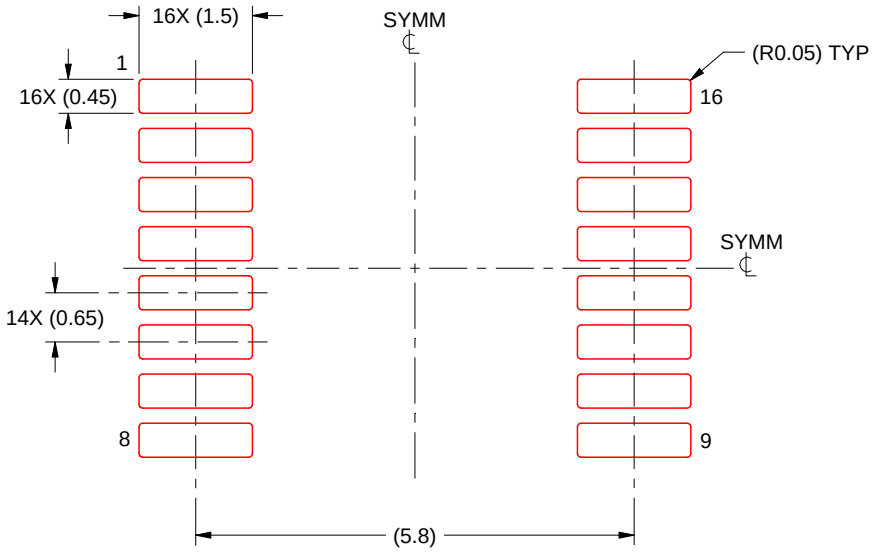


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

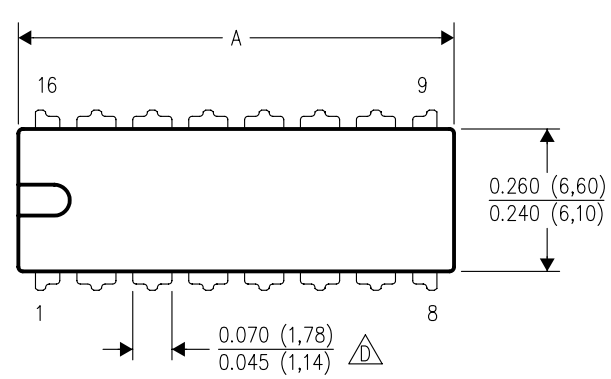
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

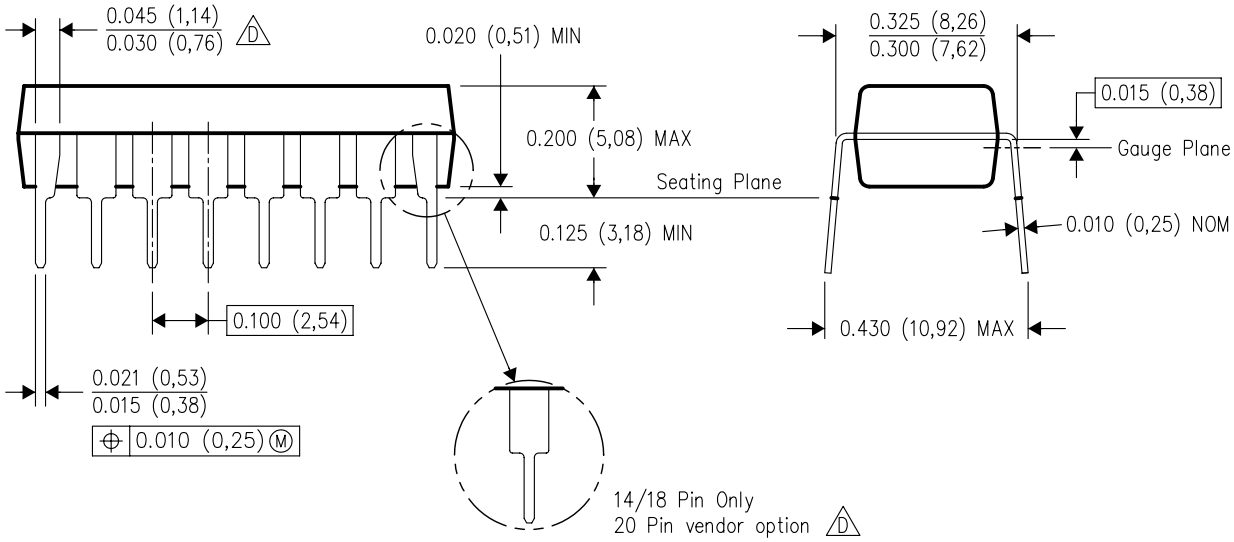
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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