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# FXWA9306 Dual Bi-Directional I<sup>2</sup>C-Bus<sup>®</sup> and SMBus Voltage-Level Translator

## Features

- 2-Bit Bi-Directional Translator for SDA and SCL Lines in Mixed-Mode I<sup>2</sup>C-Bus Applications
- Standard-Mode, Fast-Mode, and Fast-Mode-Plus I<sup>2</sup>C-Bus and SMBus Compatible
- Less than 1.5ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I<sup>2</sup>C-Bus Devices and Multiple Masters
- Allows Voltage Level Translation Between:
  - V<sub>CCA</sub> = 1.0 to 3.6V and V<sub>CCB</sub> = 1.8- 5.0V
- Supports I<sup>2</sup>C Clock Stretching and Multi-Master
- Provides Bi-directional Voltage Translation without Direction Pin
- Low 3.5Ω On-State Connection Between Input and Output Ports; Provides Less Signal Distortion
- Open-Drain I<sup>2</sup>C-Bus I/O Ports (A0, A1, B0, and B1)
- 5V-Tolerant I<sup>2</sup>C-Bus I/O Ports to Support Mixed-Mode Signal Operation
- Lock-Up-Free Operation
- Flow-Through Pinout for Simpler Printed-Circuit Board Trace Routing
- Packaged in 8-Terminal Leadless MicroPak™ (1.6mm x 1.6mm) and MSOP8 (TSSOP8)

## Description

The FXWA9306 is a dual, bi-directional, I<sup>2</sup>C-bus and SMBus, voltage-level translator with an enable (OE) input that is operational from 1.0V to 3.6V (V<sub>CCA</sub>) and 1.8V to 5.5V (V<sub>CCB</sub>) without requiring a direction pin.

As with standard I<sup>2</sup>C-bus systems, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The FXWA9306 has a standard open-drain configuration of the I<sup>2</sup>C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-Mode, Fast-Mode, and Fast Mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2MHz.

All channels have the same electrical characteristics and there is a minimum deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices and at the same time protects less-ESD resistant devices.

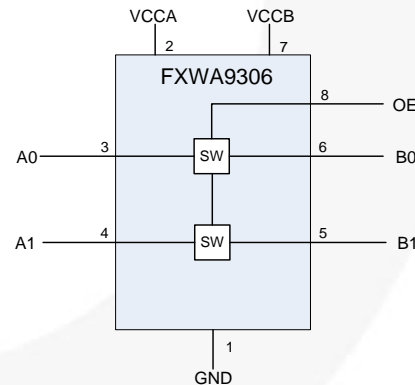


Figure 1. Block Diagram

## Ordering Information

| Part Number | Operating Temperature Range | Top Mark | Package                        | Packing Method              |
|-------------|-----------------------------|----------|--------------------------------|-----------------------------|
| FXWA9306L8X | -40 to +85°C                | LT       | 8-Lead, MicroPak™, 1.6mm Wide  | 5000 Units on Tape and Reel |
| FXMA9306MUX | -40 to +85°C                | 9306     | 8-Lead, MSOP Package, 3mm Wide | 4000 Units on Tape and Reel |

## Pin Configuration

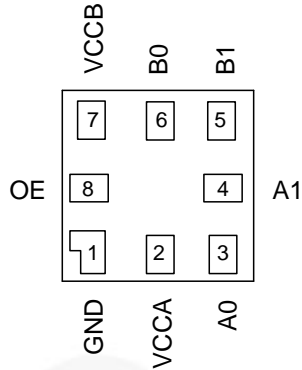


Figure 2. MicroPak™ (Top-Through View)

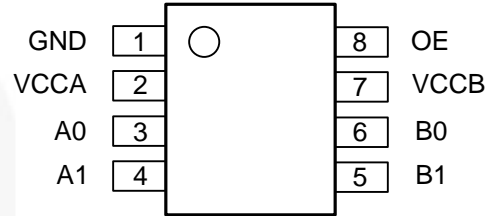


Figure 3. MSOP (Top-Through View)

## Pin Definitions

| Pin # | Name             | Description   |
|-------|------------------|---|
| 1     | GND              | Ground  |
| 2     | V <sub>CCA</sub> | Low Voltage A-Side Power Supply   |
| 3     | A <sub>0</sub>   | A-Side Input or 3-State Output. Connect to V <sub>CCA</sub> through a pull-up resistor. |
| 4     | A <sub>1</sub>   | A-Side Input or 3-State Output. Connect to V <sub>CCA</sub> through a pull-up resistor. |
| 5     | B <sub>1</sub>   | B-Side Input or 3-State Output. Connect to V <sub>CCB</sub> through a pull-up resistor. |
| 6     | B <sub>0</sub>   | B-Side Input or 3-State Output. Connect to V <sub>CCB</sub> through a pull-up resistor. |
| 7     | V <sub>CCB</sub> | High Voltage B-Side Power Supply  |
| 8     | OE               | Output Enable Input; connect to V <sub>CCB</sub> and pull-up through a high resistor.   |

## Truth Table

| Control          | Outputs   |
|------------------|---|
| OE               |   |
| LOW Logic Level  | 3-State   |
| HIGH Logic Level | Normal Operation; A <sub>0</sub> = B <sub>0</sub> , A <sub>1</sub> = B <sub>1</sub> |

### Note:

1. If the OE pin is driven LOW, the FXWA9306 is disabled and the A<sub>0</sub>, A<sub>1</sub>, B<sub>0</sub>, and B<sub>1</sub> pins are forced into 3-state.
2. OE references V<sub>CCB</sub> and the OE logic levels should be at least 1V higher than V<sub>CCA</sub>, for best translator operation.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol             | Parameter  |   | Min. | Max.             | Units |
|--------------------|--|---|------|------------------|-------|
| $V_{CCA}, V_{CCB}$ | Supply Voltage   |   | -0.5 | 7.0              | V     |
| $V_{IN}$           | DC Input Voltage   | A Port  | -0.5 | 7.0              |       |
|                    |  | B Port  | -0.5 | 7.0              |       |
|                    |  | Control Input (OE)                                  | -0.5 | 7.0              |       |
| $V_O$              | Output Voltage <sup>(3)</sup>                              | $A_n$ Outputs 3-State                               | -0.5 | 7.0              | V     |
|                    |  | $B_n$ Outputs 3-State                               | -0.5 | 7.0              |       |
|                    |  | $A_n$ Outputs Active                                | -0.5 | $V_{CCA} + 0.5V$ |       |
|                    |  | $B_n$ Outputs Active                                | -0.5 | $V_{CCB} + 0.5V$ |       |
| $I_{CH}$           | DC Channel Current   |   |      | 90               | mA    |
| $I_{IK}$           | DC Input Diode Current                                     | At $V_{IN} < 0V$                                    |      | -50              | mA    |
| $I_{OK}$           | DC Output Diode Current                                    | At $V_O < 0V$                                       |      | -50              | mA    |
|                    |  | At $V_O > V_{CC}$                                   |      | +50              |       |
| $I_{OH} / I_{OL}$  | DC Output Source/Sink Current                              |   | -50  | +50              | mA    |
| $I_{CC}$           | DC $V_{CC}$ or Ground Current per Supply Pin               |   |      | ±100             | mA    |
| $T_{STG}$          | Storage Temperature Range                                  |   | -65  | +150             | °C    |
| $I_{LATCHUP}$      | Latch-up Performance Above $V_{CC}$ and below GND at 125°C |   |      | ±100             | mA    |
| ESD                | Electrostatic Discharge Capability                         | Human Body Model, JESD22-A114-A                     |      | > 4000           | V     |
|                    |  | Human Body Model, Pin to Pin, B Port <sup>(4)</sup> |      | > 8000           |       |
|                    |  | Charged Device Model, JESD22-A115-A                 |      | > 1000           |       |

### Notes:

- $I_O$  absolute maximum rating must be observed.
- Test conditions: B0 and B1 vs.  $V_{CCB}$ , B0 and B1 vs. GND,  $V_{CCB}$  vs. GND

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol         | Parameter                               |                    | Min. | Max. | Units |
|----------------|---|--------------------|------|------|-------|
| $V_{CCA}$      | Power Supply Operating                  |                    | 1.0  | 5.5  | V     |
| $V_{CCB}$      | Power Supply Operating                  |                    | 1.8  | 5.5  | V     |
| $V_{IN}$       | Input Voltage                           | A Port             | 0    | 5.5  | V     |
|                |   | B Port             | 0    | 5.5  |       |
|                |   | Control Input (OE) | 0    | 5.5  |       |
| $\theta_{JA}$  | Thermal Resistance, Junction to Ambient |                    |      | 470  | C°/W  |
| $I_{SW(pass)}$ | Pass Switch Current                     |                    | 0    | 64   | mA    |
| $T_A$          | Free Air Operating Temperature          |                    | -40  | +85  | °C    |

### Notes:

- All unused inputs and I/O pins must be held at  $V_{CCI}$  or GND.
- $V_{CCA} \leq V_{CCB} - 1V$  for best results in level-shifting applications.

## DC Electrical Characteristics

Unless otherwise noted, values are at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ; all typical values are at  $T_A = 25^{\circ}\text{C}$ .

| Symbol         | Parameter                                       | Conditions  | Min.                                      | Typ. | Max. | Unit          |          |
|----------------|---|---|---|------|------|---------------|----------|
| $V_{IK}$       | Input Clamping Voltage                          | $I_I = -18\text{mA}$ ; $V_{I(OE)} = 0\text{V}$  |   |      | -1.2 | V             |          |
| $I_{IH}$       | High-Level Input Current                        | $V_I = 5\text{V}$ ; $V_{I(OE)} = 0\text{V}$   |   |      | 5    | $\mu\text{A}$ |          |
| $C_{i(OE)}$    | OE Pin Input Capacitance                        | $V_I = 3\text{V}$ or $0\text{V}$  |   | 7.1  |      | pF            |          |
| $C_{i/O(off)}$ | Off-State I/O Pin Capacitance<br>A0, A1, B0, B1 | $V_O = 3\text{V}$ or $0\text{V}$ ; $V_{I(OE)} = 0\text{V}$                                |   | 4    | 6    | pF            |          |
| $C_{i/O(on)}$  | On-State I/O Pin Capacitance<br>A0, A1, B0, B1  | $V_O = 3\text{V}$ or $0\text{V}$ ; $V_{I(OE)} = 3\text{V}$                                |   | 9.3  | 12.5 | pF            |          |
| $R_{ON}^{(7)}$ | On-State Resistance A0/B0,<br>A1/B1             | $V_I = 0\text{V}$ ;<br>$I_O = 64\text{mA}$  | $V_{I(OE)} = 4.5\text{V}$                 |      | 2.4  | 5.0           | $\Omega$ |
|                |   |   | $V_{I(OE)} = 3\text{V}$                   |      | 3.0  | 6.0           |          |
|                |   |   | $V_{I(OE)} = 2.3\text{V}$                 |      | 3.8  | 8.0           |          |
|                |   |   | $V_{I(OE)} = 1.5\text{V}$                 |      | 9.0  | 20.0          |          |
| $V_{OL}$       | Voltage Output Low                              | $V_{CCA} = 1\text{V}$ ,<br>$V_{PUD} = 5\text{V}$ ,<br>$I_{OL} = 3\text{mA}$<br>(B->A Dir) | $V_{IN} \text{ (B0 or B1)} = 0.1\text{V}$ |      |      | 0.15          | V        |
|                |   |   | $V_{IN} \text{ (B0 or B1)} = 0.2\text{V}$ |      |      | 0.25          |          |
|                |   |   | $V_{IN} \text{ (B0 or B1)} = 0.3\text{V}$ |      |      | 0.35          |          |
|                |   |   | $V_{IN} \text{ (B0 or B1)} = 0.4\text{V}$ |      |      | 0.45          |          |

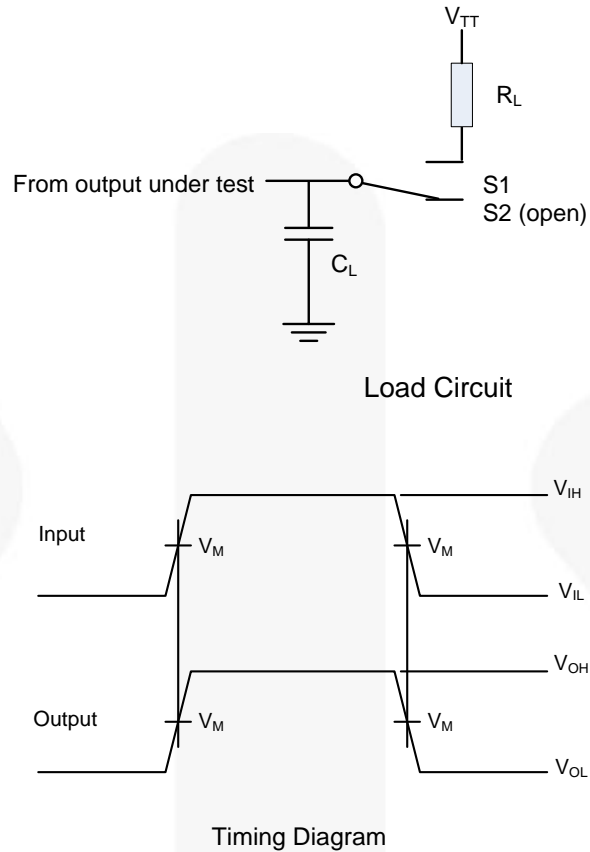
### Notes:

7. Measured by the voltage drop between the A0 and B0 or A1 and B1 terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two terminals.

## AC Electrical Characteristics

T<sub>A</sub> = -40°C to +85°C. Direction is from B port to A port (translating down). Values guaranteed by design.

| Symbol           | Parameter   | Conditions   | Load Condition:  | Min:                  | Max. | Units |    |
|------------------|---|--|--|-----------------------|------|-------|----|
| t <sub>PLH</sub> | Low-to-High Propagation Delay, from (Input) B0 or B1 to (Output) A0 or A1 | V <sub>I(OE)</sub> = 3.3V; V <sub>IH</sub> = 3.3V;<br>V <sub>IL</sub> = 0V; V <sub>M</sub> = 1.15V;<br>V <sub>CCA</sub> = 2.3V   | C <sub>L</sub> = 15pF  | 0                     | 0.60 | ns    |    |
|                  |   |  | C <sub>L</sub> = 30pF  | 0                     | 1.20 |       |    |
|                  |   |  | C <sub>L</sub> = 50pF  | 0                     | 2.00 |       |    |
| t <sub>PHL</sub> | High-to-Low Propagation Delay, from (Input) B0 or B1 to (Output) A0 or A1 |  | V <sub>I(OE)</sub> = 3.3V; V <sub>IH</sub> = 3.3V;<br>V <sub>IL</sub> = 0V; V <sub>M</sub> = 1.15V;<br>V <sub>CCA</sub> = 2.3V   | C <sub>L</sub> = 15pF | 0    | 0.75  | ns |
|                  |   |  |  | C <sub>L</sub> = 30pF | 0    | 1.50  |    |
|                  |   |  |  | C <sub>L</sub> = 50pF | 0    | 2.00  |    |
| t <sub>PLH</sub> | Low-to-High Propagation Delay, from (Input) B0 or B1 to (Output) A0 or A1 | V <sub>I(OE)</sub> = 2.5V; V <sub>IH</sub> = 2.5V;<br>V <sub>IL</sub> = 0V; V <sub>M</sub> = 0.75V;<br>V <sub>CCA</sub> = 1.5V   |  | C <sub>L</sub> = 15pF | 0    | 0.60  | ns |
|                  |   |  |  | C <sub>L</sub> = 30pF | 0    | 1.20  |    |
|                  |   |  |  | C <sub>L</sub> = 50pF | 0    | 2.00  |    |
| t <sub>PHL</sub> | High-to-Low Propagation Delay, from (Input) B0 or B1 to (Output) A0 or A1 |  | V <sub>I(OE)</sub> = 2.5V; V <sub>IH</sub> = 2.5V;<br>V <sub>IL</sub> = 0V; V <sub>M</sub> = 0.75V;<br>V <sub>CCA</sub> = 1.5V   | C <sub>L</sub> = 15pF | 0    | 0.75  | ns |
|                  |   |  |  | C <sub>L</sub> = 30pF | 0    | 1.50  |    |
|                  |   |  |  | C <sub>L</sub> = 50pF | 0    | 2.00  |    |
| t <sub>PLH</sub> | Low-to-High Propagation Delay, from (Input) A0 or A1 to (Output) B0 or B1 | V <sub>I(OE)</sub> = 3.3V; V <sub>IH</sub> = 2.3V;<br>V <sub>IL</sub> = 0V; V <sub>TT</sub> = 3.3V;<br>V <sub>M</sub> = 1.15V; V <sub>CCA</sub> = 2.3V;<br>R <sub>L</sub> = 300Ω |  | C <sub>L</sub> = 15pF | 0    | 0.50  | ns |
|                  |   |  |  | C <sub>L</sub> = 30pF | 0    | 1.00  |    |
|                  |   |  |  | C <sub>L</sub> = 50pF | 0    | 1.75  |    |
| t <sub>PHL</sub> | High-to-Low Propagation Delay, from (Input) A0 or A1 to (Output) B0 or B1 |  | V <sub>I(OE)</sub> = 3.3V; V <sub>IH</sub> = 2.3V;<br>V <sub>IL</sub> = 0V; V <sub>TT</sub> = 3.3V;<br>V <sub>M</sub> = 1.15V; V <sub>CCA</sub> = 2.3V;<br>R <sub>L</sub> = 300Ω | C <sub>L</sub> = 15pF | 0    | 0.80  | ns |
|                  |   |  |  | C <sub>L</sub> = 30pF | 0    | 1.65  |    |
|                  |   |  |  | C <sub>L</sub> = 50pF | 0    | 2.75  |    |
| t <sub>PLH</sub> | Low-to-High Propagation Delay, from (Input) A0 or A1 to (Output) B0 or B1 | V <sub>I(OE)</sub> = 2.5V; V <sub>IH</sub> = 1.5V;<br>V <sub>IL</sub> = 0V; V <sub>TT</sub> = 2.5V;<br>V <sub>M</sub> = 0.75V; V <sub>CCA</sub> = 1.5V;<br>R <sub>L</sub> = 300Ω |  | C <sub>L</sub> = 15pF | 0    | 0.50  | ns |
|                  |   |  |  | C <sub>L</sub> = 30pF | 0    | 1.00  |    |
|                  |   |  |  | C <sub>L</sub> = 50pF | 0    | 1.75  |    |
| t <sub>PHL</sub> | High-to-Low Propagation Delay, from (Input) A0 or A1 to (Output) B0 or B1 |  | V <sub>I(OE)</sub> = 2.5V; V <sub>IH</sub> = 1.5V;<br>V <sub>IL</sub> = 0V; V <sub>TT</sub> = 2.5V;<br>V <sub>M</sub> = 0.75V; V <sub>CCA</sub> = 1.5V;<br>R <sub>L</sub> = 300Ω | C <sub>L</sub> = 15pF | 0    | 1.00  | ns |
|                  |   |  |  | C <sub>L</sub> = 30pF | 0    | 2.00  |    |
|                  |   |  |  | C <sub>L</sub> = 50pF | 0    | 3.30  |    |

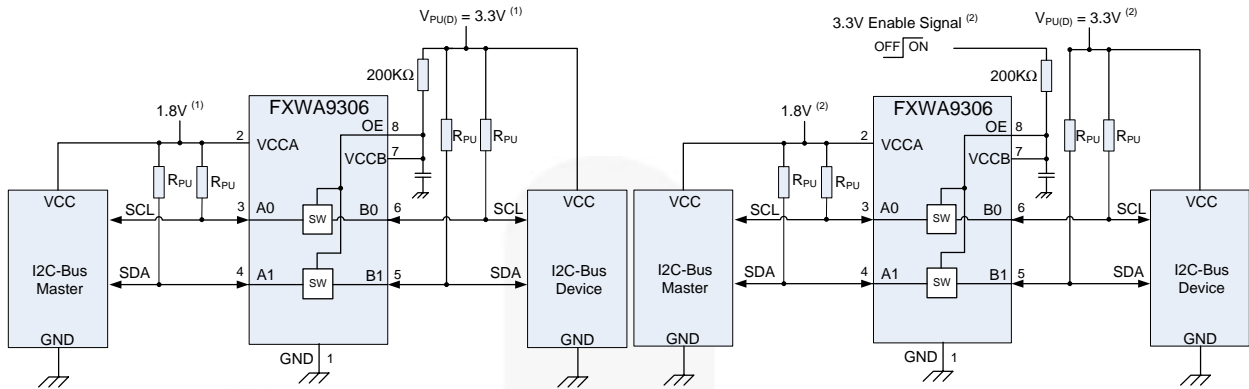


**Figure 4. Load Circuit**

**Notes:**

8. S1 = translating up (A-to-B direction), S2 = translating down (B-to-A direction).
9.  $C_L$  includes probe and jig capacitance.
10. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{MHz}$ ;  $Z_O = 50\Omega$ ;  $t_r \leq 2\text{ns}$ ;  $t_f \leq 2\text{ns}$ .
11. The outputs are measured one at a time, with one transmission per measurement.

## Application Information



**Figure 5. Application (Switch Always Enabled)**

**Figure 6. Application (Switch Enable Control)**

### Note:

12. The applied voltages at  $V_{CCA}$  and  $V_{PU(D)}$  should be such that  $V_{CCB}$  is at least 1V higher than  $V_{CCA}$  for best translator operation.

## Bi-directional Translation

For the bi-directional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the OE input must be connected to  $V_{CCB}$  and both pins pulled to HIGH side  $V_{PU(D)}$  through a pull-up resistor (typically 200kΩ). This allows  $V_{CCB}$  to regulate the OE input. A filter capacitor on  $V_{CCB}$  is recommended. The I<sup>2</sup>C-bus master output can be totem-pole or open-drain (pull-up resistors may be required) and the I<sup>2</sup>C-bus device output can be totem-pole or open-drain (pull-up resistors are required to pull the B0 and B1 outputs to  $V_{PU(D)}$ ). However, if either output is totem-pole, data must be uni-directional or the outputs must be 3-

stateable and be controlled by some direction-controlled mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ( $V_{CCA}$ ) is connected to the processor core power supply voltage. When  $V_{CCB}$  is connected through a 200kΩ resistor to a 3.3V - 5.5V  $V_{PU(D)}$  power supply, and  $V_{CCA}$  is set between 1.0V and ( $V_{PU(D)} - 1V$ ), the output of each A0 and A1 has a maximum output voltage equal to  $V_{CCA}$  and the output of each B0 and B1 has a maximum output voltage equal to  $V_{PU(D)}$ .

**Table 1. Application Operating Conditions (refer to Figure 6)**

All typical values are at  $T_A = 25^\circ\text{C}$ .

| Symbol              | Parameter              | Conditions            | Min.            | Typ. | Max. | Unit |
|---------------------|------------------------|-----------------------|-----------------|------|------|------|
| $V_{BIAS}(V_{CCB})$ | Reference Bias Voltage |                       | $V_{CCA} + 0.6$ | 2.1  | 5.0  | V    |
| $V_{I(OE)}$         | OE Pin Input Voltage   |                       | $V_{CCA} + 0.6$ | 2.1  | 5.0  | V    |
| $V_{CCA}$           | Reference Voltage      |                       | 0               | 1.5  | 4.4  | V    |
| $I_{SW(pass)}$      | Pass Switch Current    |                       |                 | 14   |      | mA   |
| $I_{REF}$           | Reference Current      | Transistor            |                 | 5    |      | μA   |
| $T_A$               | Ambient Temperature    | Operating in Free Air | -40             |      | +85  | °C   |

## Sizing Pull-Up Resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the on state to about 15mA. This ensures a pass voltage of 260mV to 350mV. If the current through the pass transistor is higher than 15mA, the pass voltage is higher in the on state. To set the current through each pass transistor at 15mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{PU(D)} - 0.35V}{0.015A} \quad (1)$$

Table 2 summarizes the resistor reference voltages and currents at 15mA, 10mA, and 3mA. The resistor values shown in the +10% column or a larger value should be used to ensure that the pass voltage of the transistor would be 350mV or less. The external driver must be able to sink the total current from the resistors on both sides of the of the FXWA9306 device at 0.175V, although the 15mA only applies to the current flowing through the FXWA9306 device.



**Table 2. Application Operating Conditions**

Calculated for  $V_{OL} = 0.35V$ ; assumes output driver  $V_{OL} = 0.175V$  at stated current.

| $V_{PU(D)}$ | Pull-Up Resistor Value ( $\Omega$ ) |                      |         |                      |         |                      |
|-------------|-------------------------------------|----------------------|---------|----------------------|---------|----------------------|
|             | 15mA                                |                      | 10mA    |                      | 3mA     |                      |
|             | Nominal                             | +10% <sup>(13)</sup> | Nominal | +10% <sup>(13)</sup> | Nominal | +10% <sup>(13)</sup> |
| 5.0V        | 310                                 | 341                  | 465     | 512                  | 1550    | 1705                 |
| 3.3V        | 197                                 | 217                  | 295     | 325                  | 983     | 1082                 |
| 2.5V        | 143                                 | 158                  | 215     | 237                  | 717     | 788                  |
| 1.8V        | 97                                  | 106                  | 145     | 160                  | 483     | 532                  |
| 1.5V        | 77                                  | 85                   | 115     | 127                  | 383     | 422                  |
| 1.2V        | 57                                  | 63                   | 85      | 94                   | 283     | 312                  |

**Note:**

13. +10% to compensate for  $V_{CC}$  range and resistor tolerance.

**Maximum Frequency Calculation**

The maximum frequency is totally dependent upon the specifics of the application. The FXWA9306 behaves like a wire with the additional characteristics of transistor device physics and should be capable of performing at higher frequencies if used correctly.

Here are some guidelines to follow that help maximize the performance of the device:

- Keep trace lengths to a minimum by placing the FXWA9306 close to the processor.
- The trace length should be less than half the time of flight to reduce ringing and reflections.
- The faster the edge of the signal, the higher the chance of ringing.
- The greater the drive strength (up to 15mA), the higher the frequency the device can use.

In a 3.3V to 1.8V direction level shift, if the 3.3V side is being driven by a totem-pole type driver; no pull-up resistor is needed on the 3V side. The capacitance and

line length of concern is on the 1.8V side because it is driven through the on resistance of the FXWA9306. If the line length on the 1.8V side is long enough, there can be a reflection at the chip / terminating end of the wire when the transition time is shorter than the time of flight of the wire. This is because the FXWA9306 looks like a high-impedance path compared to the wire. If the wire is too long and the lumped capacitance is not excessive, the signal is only slightly degraded by the series resistance added by passing through the FXWA9306. If the lumped capacitance is large, the rise time deteriorates. The fall time is much less affected and if the rise time is slowed down too much, the duty cycle of the clock is degraded and, at some point, the clock is no longer useful. So, the principle design consideration is to minimize the wire length and the capacitance on the 1.8V side for the clock path. A pull-up resistor on the 1.8V side can be used to trade a slower fall time for a faster rise time and can also reduce overshoot in some cases.

**Additional Note**

The FXWA9306 is not a bus buffer that provides both level translation and physical capacitance isolation to either side of the bus when both sides are connected. The FXWA9306 only isolates the sides when the device is disabled and provides level translation when active.

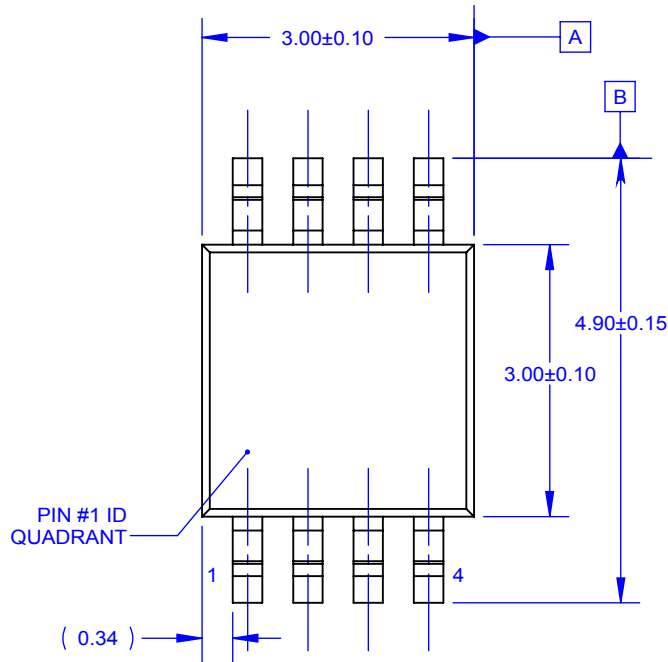
The FXWA9306 can be used to run two buses: one at 400kHz operating frequency and the other at 100kHz operating frequency. If the two buses are operating at different frequencies, the 100kHz bus must be isolated when the 400kHz operation of the bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400kHz because of the delays added to the translator.

When the A1 or B1 port is LOW, the clamp is in the ON-state and a low-resistance connection exists between the A1 and B1 ports. Assuming the higher voltage is on the B1 port, when the B1 port is HIGH, the voltage on the A1 port is limited by the voltage set by  $V_{CCA}$ . When the A1 port is HIGH, the B1 port is pulled to the drain pull-up supply voltage ( $V_{PU(D)}$ ) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The A0/B0 channel also functions as the A1/B1 channel-

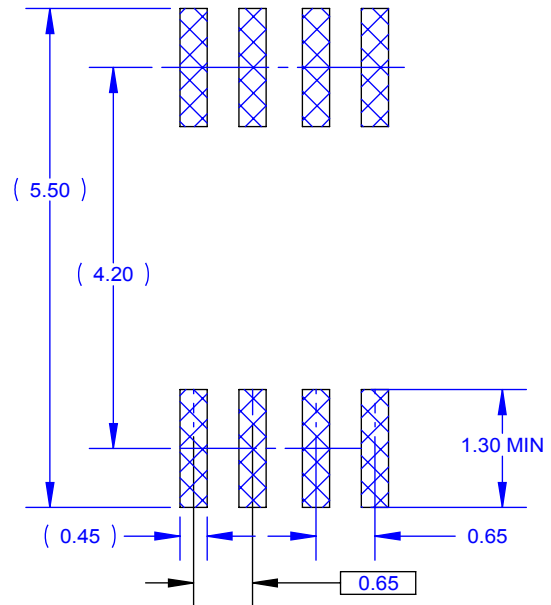
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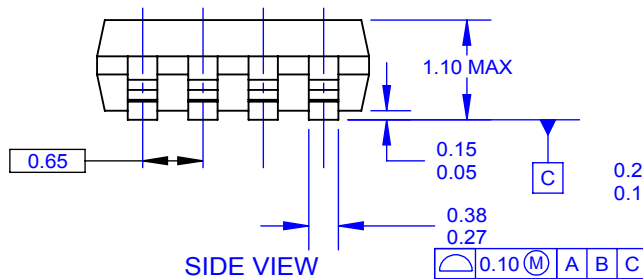
| NBR | DESCRIPTION   | DATE      | BY/APP'D   |
|-----|---|-----------|------------|
| B   | REDREW FORMER NSC DWG   | 07JUN2006 | H.ALLEN    |
| 3   | * REMOVE SITE ADDRESS AND CHANGE REVISION TO NUMERICAL.<br>* CHANGE LEAD WIDTH FROM 0.27-0.38 TO 0.22-0.40.<br>* CHANGE STAND OFF FROM 0.05MIN TO 0.00MIN.<br>* CHANGE LEAD THICKNESS FROM 0.13MIN TO 0.08MIN.<br>* CHANGE FOOT LENGTH FROM 0.70MAX TO 0.80MAX. | 20AUG2009 | KHLEE/FSSZ |
| 4   | * REVERT LEAD WIDTH TO PREV REV 0.27-0.38.<br>* REVERT STAND OFF TO 0.05MIN.<br>* REVERT LEAD THICKNESS TO 0.13MIN.<br>* REVERT FOOT LENGTH TO 0.70MAX.   | 24SEP2009 | KHLEE/FSSZ |



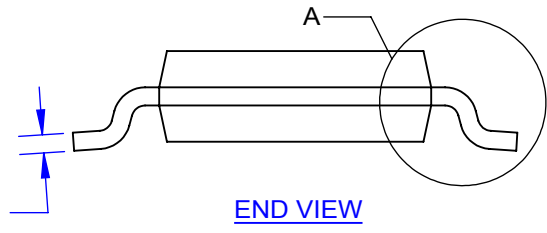
TOP VIEW



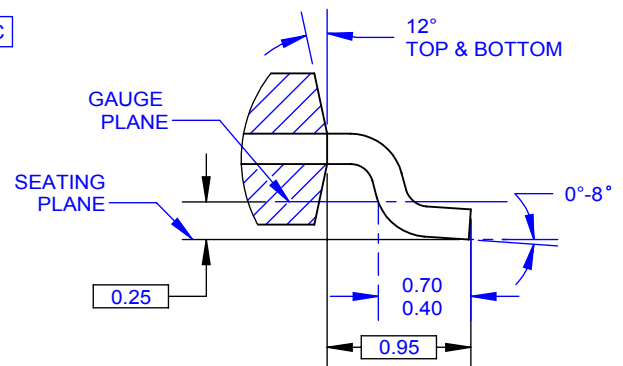
LAND PATTERN RECOMMENDATION



SIDE VIEW



END VIEW

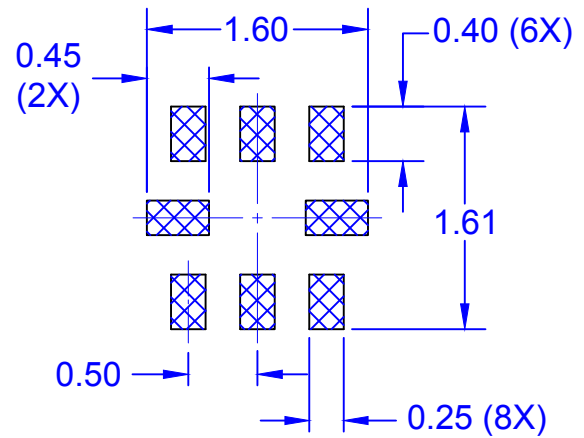
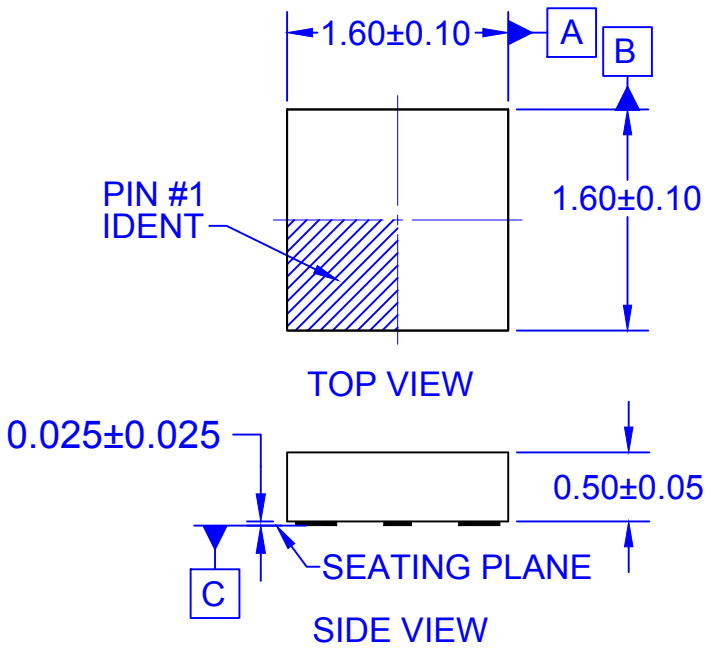


DETAIL A  
SCALE 20 : 1

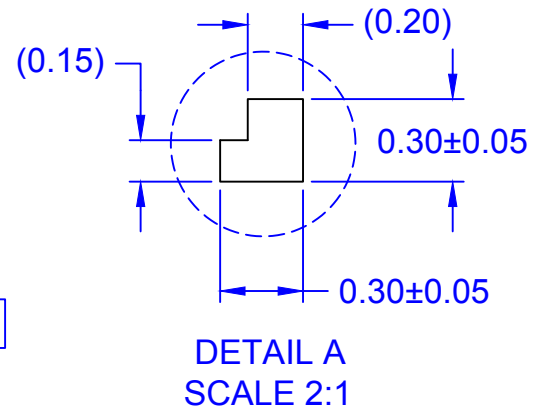
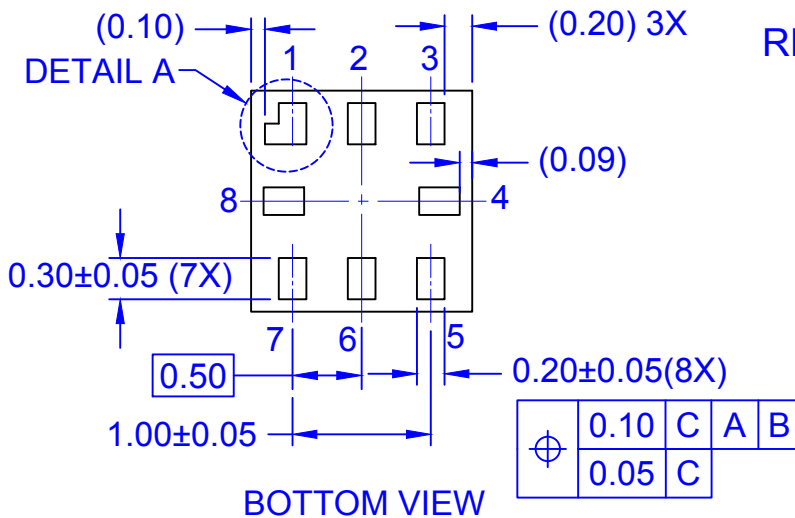
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| APPROVALS              |  | DATE    | <br>8LD, MSOP, JEDEC MO-187, 3.0MM WIDE |          |                           |       |
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### RECOMMENDED LAND PATTERN



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