TS5A23157 Dual 10-Ω SPDT Analog Switch

1 Features

- Low ON-State Resistance (15 Ω at 125°C)
- 125°C Operation
- Control Inputs are 5-V Tolerant
- Specified Break-Before-Make Switching
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion
- 1.8-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

3 Description

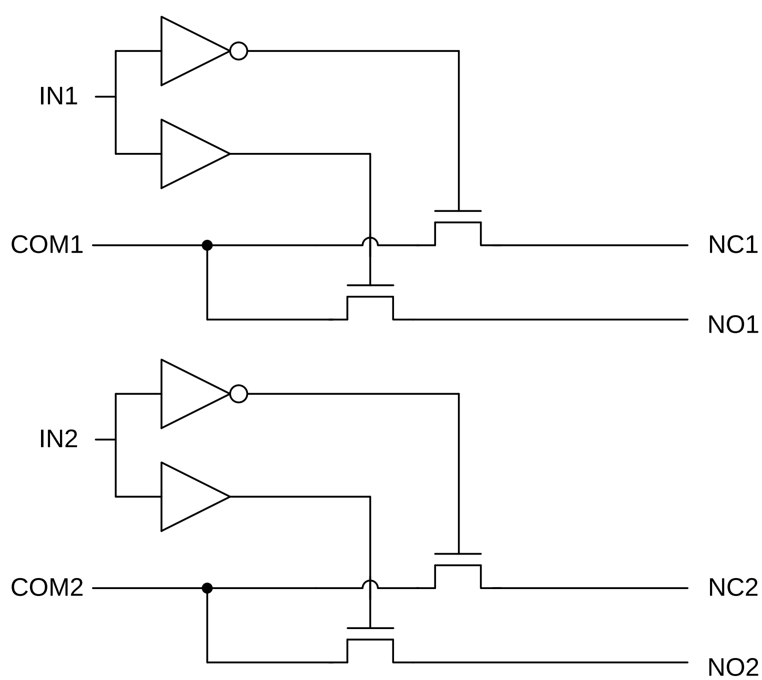
The TS5A23157 device is a dual single-pole double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to 5.5 V (peak) can be transmitted in either direction.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23157DGS	VSSOP (10)	3.00 mm × 3.00 mm
TS5A23157RSE	UQFN (10)	2.00 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2015) to Revision F — **Page**

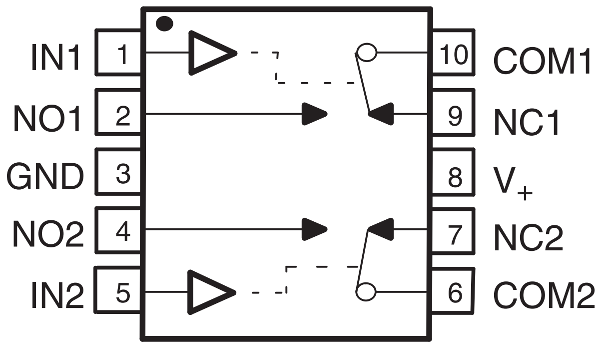
- Changed *Feature* From: Low ON-State Resistance (10 Ω) To: Low ON-State Resistance (15 Ω at 125℃) 1
- Added *Feature* : 125℃ Operation 1
- Added Junction Temperature To the *Absolute Maximum Ratings* table 4
- Changed the Operating temperature MAX value From: 85°C To: 125°C in the *Recommended Operating Conditions* table 4
- Changed the *Thermal Information* table 4
- Changed r_{on} in the *Electrical Characteristics for 5-V Supply* table 5
- Changed V_{IH} in the *Electrical Characteristics for 5-V Supply* table 5
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 5-V Supply* table 5
- Changed r_{on} in the *Electrical Characteristics for 3.3-V Supply* table 7
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 3.3-V Supply* table 7
- Changed r_{on} in the *Electrical Characteristics for 2.5-V Supply* table 8
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 2.5-V Supply* table 8
- Changed r_{on} in the *Electrical Characteristics for 1.8-V Supply* table 9
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 1.8-V Supply* table 9

Changes from Revision D (October 2013) to Revision E — **Page**

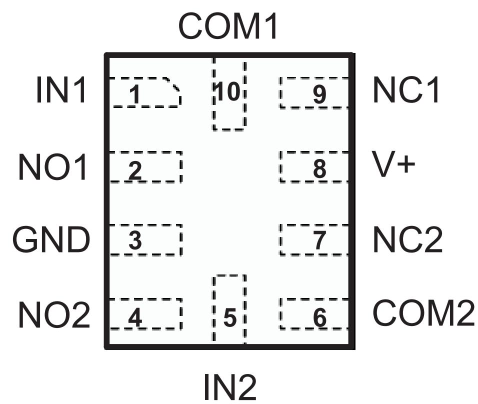
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



RSE Package
10-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN1	I	Select pin for switch 1
2	NO1	I/O	Normally open I/O for switch 1
3	GND	—	Ground
4	NO2	I/O	Normally open I/O for switch 2
5	IN2	I	Select pin for switch 2
6	COM2	I/O	Common I/O for switch 2
7	NC2	I/O	Normally closed I/O for switch 2
8	V+	—	Power supply pin
9	NC1	I/O	Normally closed I/O for switch 1
10	COM1	I/O	Common I/O for switch 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_+	Supply voltage[2]		–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage[2][3][4]		–0.5	$V_+ + 0.5$	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, $V_{COM} < 0$ or V_{NC}, V_{NO}, $V_{COM} > V_+$		±50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+		±50	mA
V_{IN}	Digital input voltage[2][3]		–0.5	6.5	V
I_{IK}	Digital input clamp current	$V_{IN} < 0$		–50	mA
	Continuous current through V_+ or GND			±100	mA
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TS5A23157		UNIT
		DGS (VSSOP)	RSE (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.5	215.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	99.1	140.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	132.4	137.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.1	13.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	130.5	137.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP [1]	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, see Figure 9	Full	4.5 V			10	Ω
				-40 to 125°C				15	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 3.15 V, I_{COM} = –30 mA,	Switch ON, see Figure 9	25°C	4.5 V		0.15		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, see Figure 9	25°C	4.5 V		4		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	5.5 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2) [2]									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
				-40 to 125°C	4.75 V to 5.25 V	3.1			
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	5.5 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	4.5 V to 5.5 V	1.7		5.7	ns
				-40 to 125°C	4.75 V to 5.25 V	1.2		8.7	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	4.5 V to 5.5 V	0.8		3.8	ns
				-40 to 125°C	4.75 V to 5.25 V	0.5		6.8	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	4.5 V to 5.5 V	0.5			ns
Q_C	Charge injection	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	See Figure 17	25°C	5 V		7		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch OFF, see Figure 11	25°C	5 V		5.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 11	25°C	5 V		2.8		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	4.5 V		220		MHz

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	4.5 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	4.5 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	4.5 V		0.01%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	5.5 V			500	µA

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 9	Full	3 V			18	Ω
				-40 to 125°C				23	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, see Figure 9	25°C	3 V		0.2		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 11	25°C	3 V		9		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turn-on time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	3 V to 3.6 V	2.5		7.6	ns
				-40 to 125°C		2.0		10.6	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	3 V to 3.6 V	1.5		5.3	ns
				-40 to 125°C		1.0		8.3	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = $V_+/2$, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	3 V to 3.6 V	0.5			ns
Q_C	Charge injection	R_L = 50 Ω, C_L = 0.1 nF,	see Figure 17	25°C	3.3 V		3		pC
BW	Bandwidth	R_L = 50 Ω, Switch ON,	see Figure 14	25°C	3 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	3 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	3 V		0.015%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	3.6 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[(1)]	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 9	Full	2.3 V			45	Ω
				-40 to 125°C				50	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, see Figure 9	25°C	2.3 V		0.5		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 9	25°C	2.3 V		27		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	2.7 V	–1	0.05	1	μA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	2.7 V	–0.1		0.1	μA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	2.7 V	–0.1		0.1	μA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)[(2)]									
V_{IH}	Input logic high			Full		$V_+ \times 0.7$			V
V_{IL}	Input logic low			Full				$V_+ \times 0.3$	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	2.7 V	–1	0.05	1	μA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	2.3 V to 2.7 V	3.5		14	ns
				-40 to 125°C		2.5		17	
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	2.3 V to 2.7 V	2		7.5	ns
				-40 to 125°C		1.5		10.5	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	2.3 V to 2.7 V	0.5			ns
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	2.3 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	2.3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	2.3 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	2.3 V		0.025%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			1	μA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	2.7 V			500	μA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[(1)]	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –4 mA,	Switch ON, see Figure 9	Full	1.65 V			140	Ω
				-40 to 125°C				180	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.15 V, I_{COM} = –4 mA,	Switch ON, see Figure 9	25°C	1.65 V		1		Ω
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –4 mA,	Switch ON, see Figure 9	25°C	1.65 V		110		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)[(2)]									
V_{IH}	Input logic high			Full		$V_+ \times 0.75$			V
V_{IL}	Input logic low			Full				$V_+ \times 0.25$	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	1.65 V to 1.95 V	7		24	ns
				-40 to 125°C		5.5		27	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	1.65 V to 1.95 V	3		13	ns
				-40 to 125°C		2		16	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = $V_+/2$, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	1.65 V to 1.95 V	0.5			ns
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	1.8 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	1.8 V		–60		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	1.8 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	1.8 V		0.015%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	1.95 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.9 Typical Characteristics

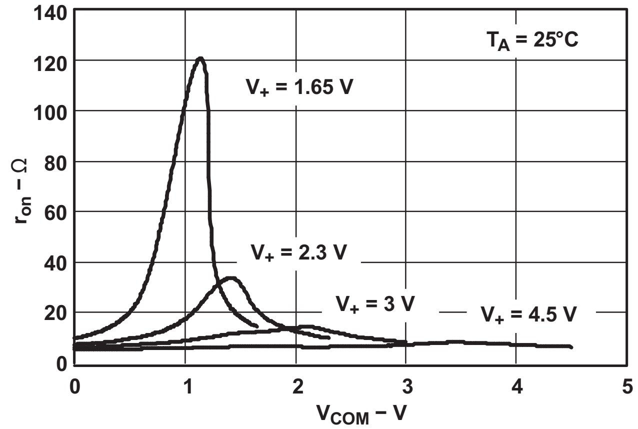


Figure 1. r_{on} vs V_{COM}

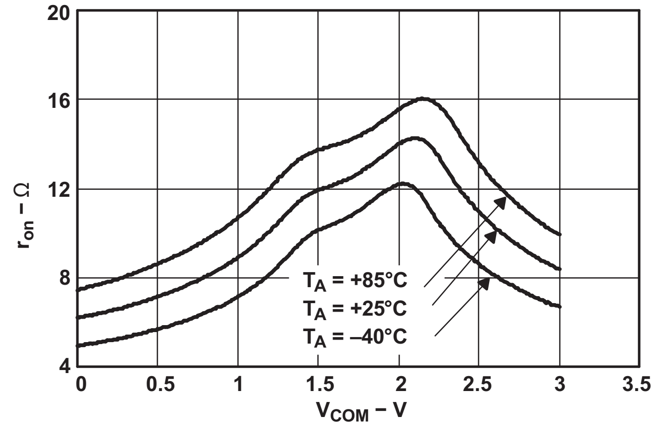


Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)

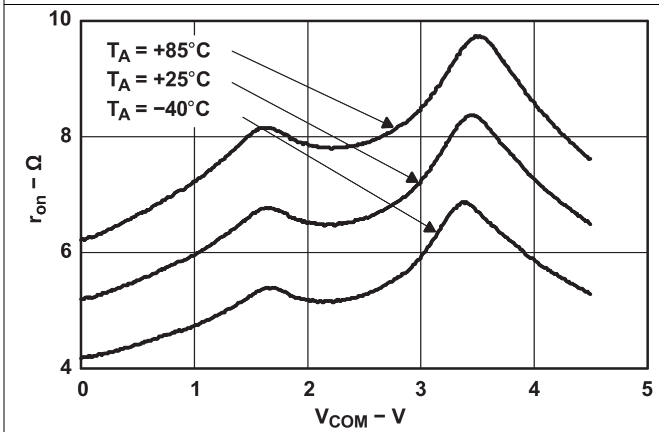


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

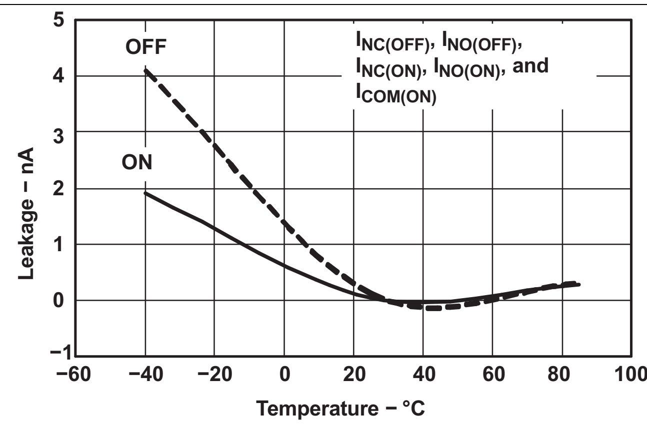


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5$ V)

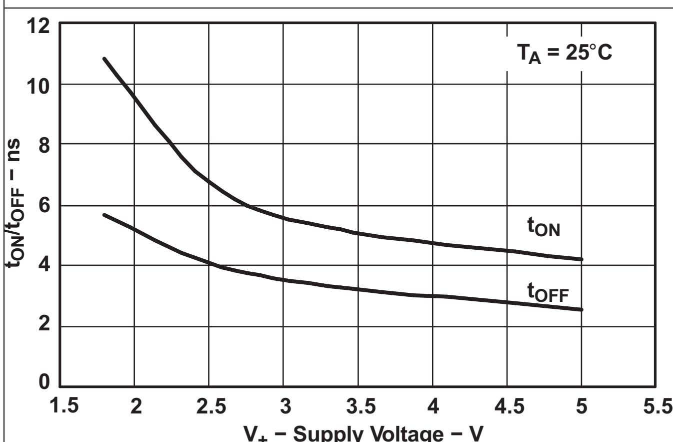


Figure 5. t_{ON} and t_{OFF} vs V_+

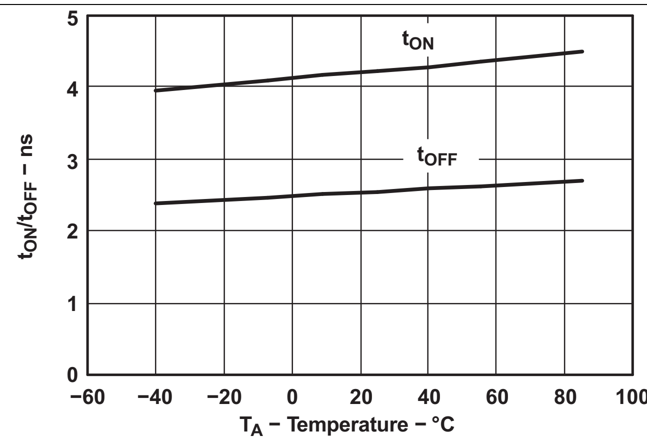


Figure 6. t_{ON} and t_{OFF} vs Temperature ($V_+ = 5$ V)

Typical Characteristics (continued)

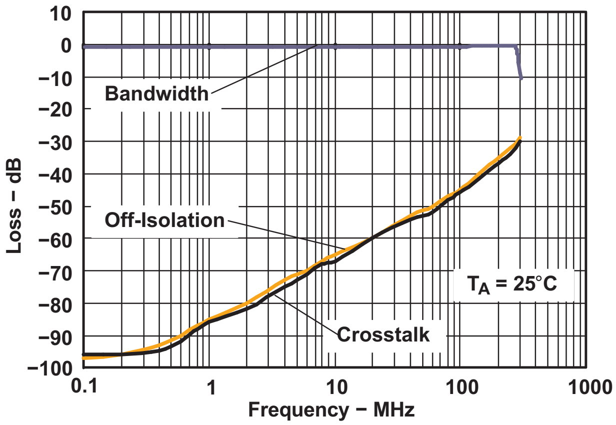


Figure 7. Frequency Response (V_+ = 3 V)

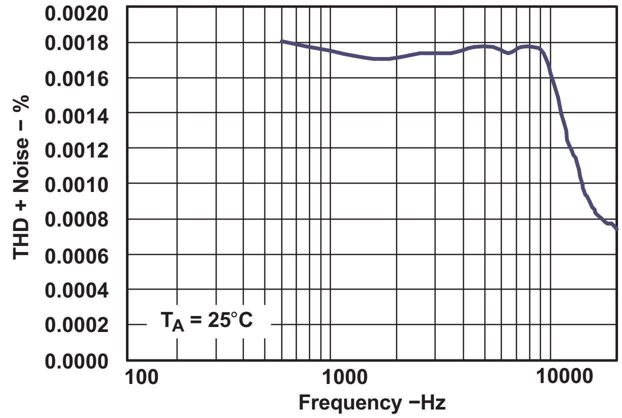
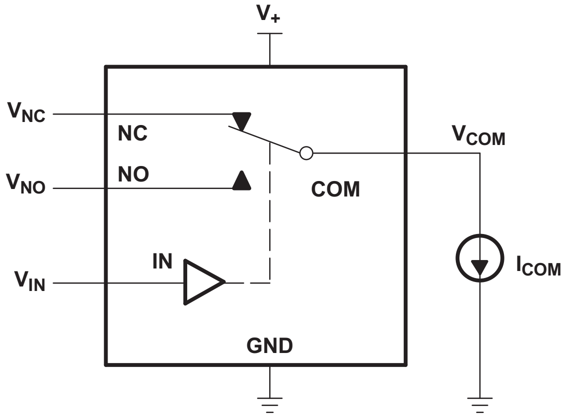


Figure 8. Total Harmonic Distortion (THD) vs Frequency (V_+ = 3 V)

7 Parameter Measurement Information

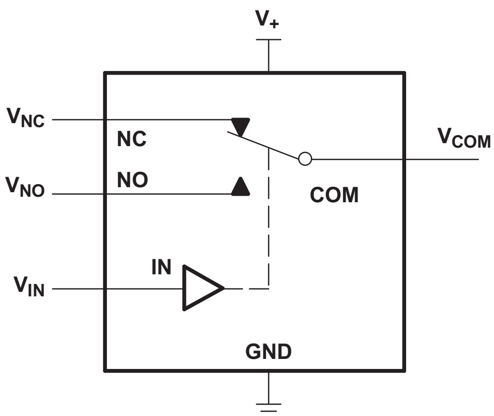


Channel ON

$r_{on} = \frac{V_{COM} \quad V_{NO/NC}}{I_{COM}}\ \Omega$

$V_{IN} = V_{IH}$ or V_{IL}

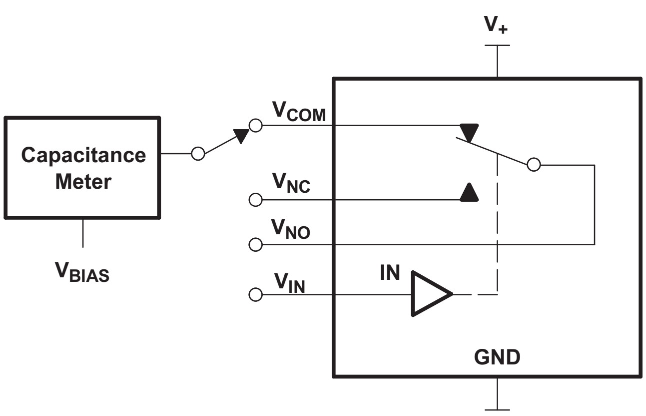
Figure 9. ON-State Resistance (r_{on})



OFF-State Leakage Current
Channel OFF
$V_{IN} = V_{IH}$ or V_{IL}
V_{NC} or V_{NO} = 0 to V_+
or
V_{COM} = 0 to V_+

ON-State Leakage Current
Channel ON
$V_{IN} = V_{IH}$ or V_{IL}
V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open
or
V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+

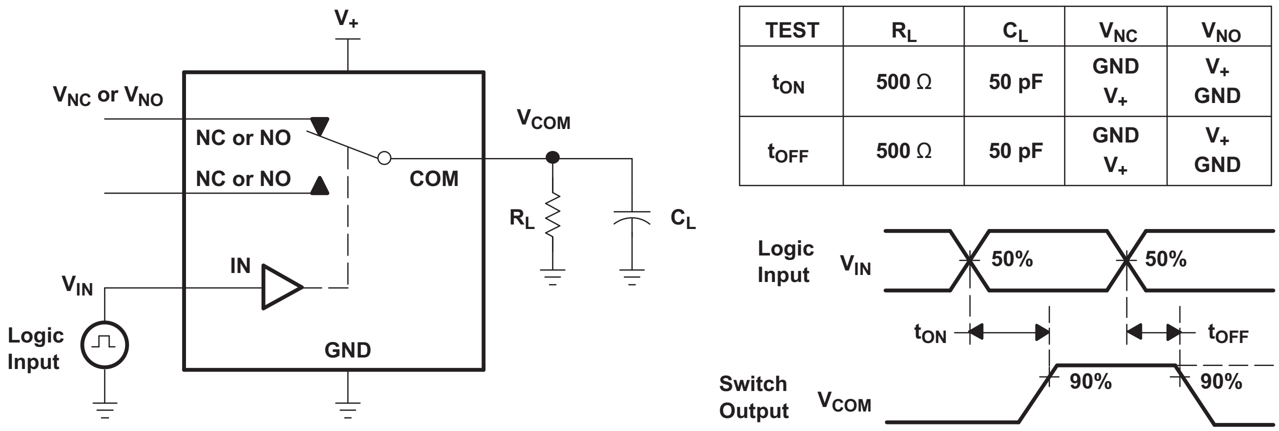
Figure 10. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)



$V_{BIAS} = V_+$ or GND
$V_{IN} = V_{IH}$ or V_{IL}
Capacitance is measured at NC, NO, COM, and IN inputs during ON and OFF conditions.

Figure 11. Capacitance (C_{IN}, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)



TEST	R_L	C_L	V_{NC}	V_{NO}
t_{ON}	500 Ω	50 pF	GND V_+	V_+ GND
t_{OFF}	500 Ω	50 pF	GND V_+	V_+ GND

Figure 12. Turnon (t_{ON}) and Turnoff (t_{OFF}) Time

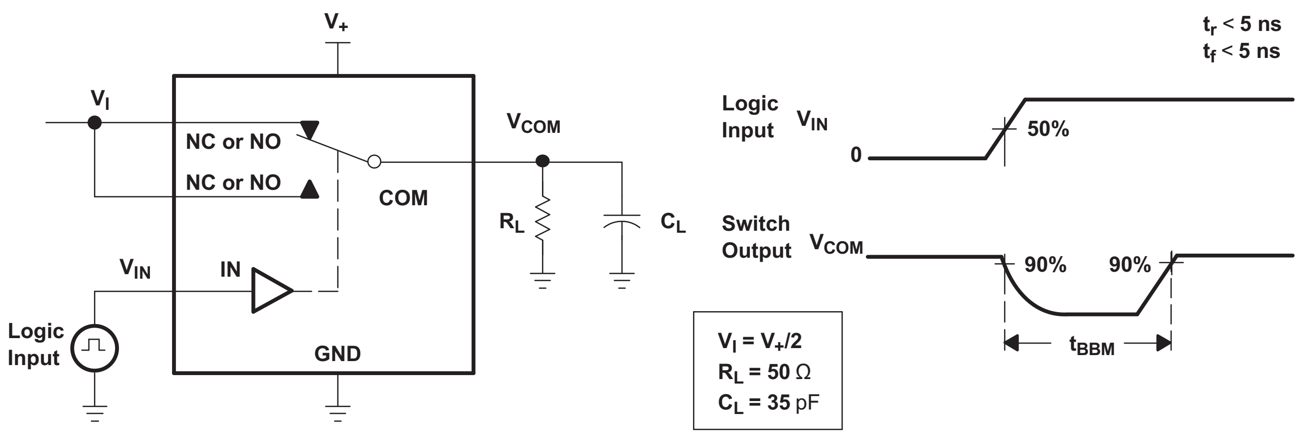


Figure 13. Break-Before-Make (t_{BBM}) Time

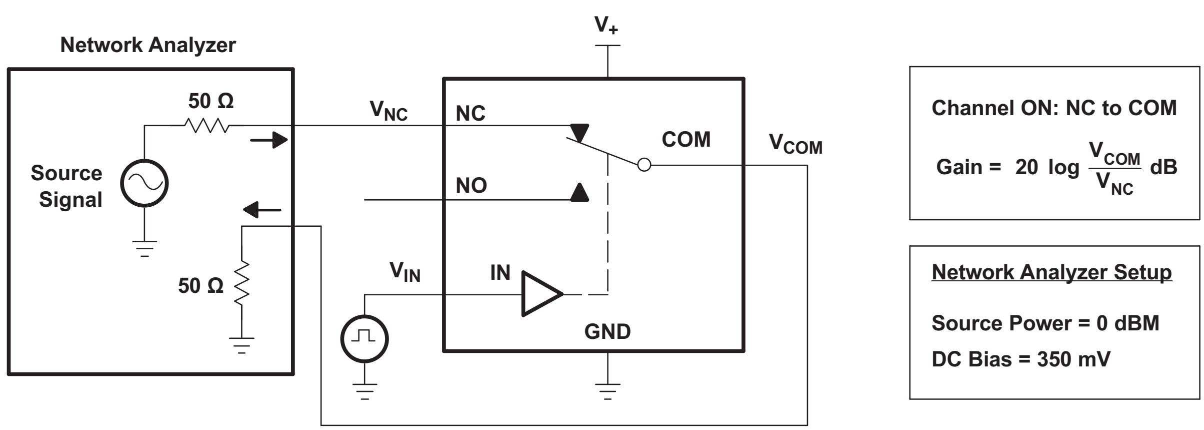


Figure 14. Frequency Response (BW)

Parameter Measurement Information (continued)

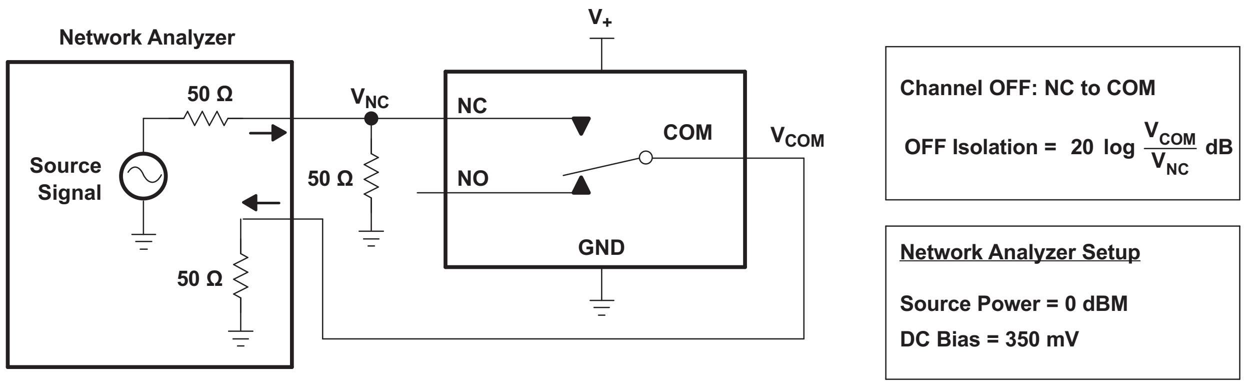


Figure 15. OFF Isolation (O_{ISO})

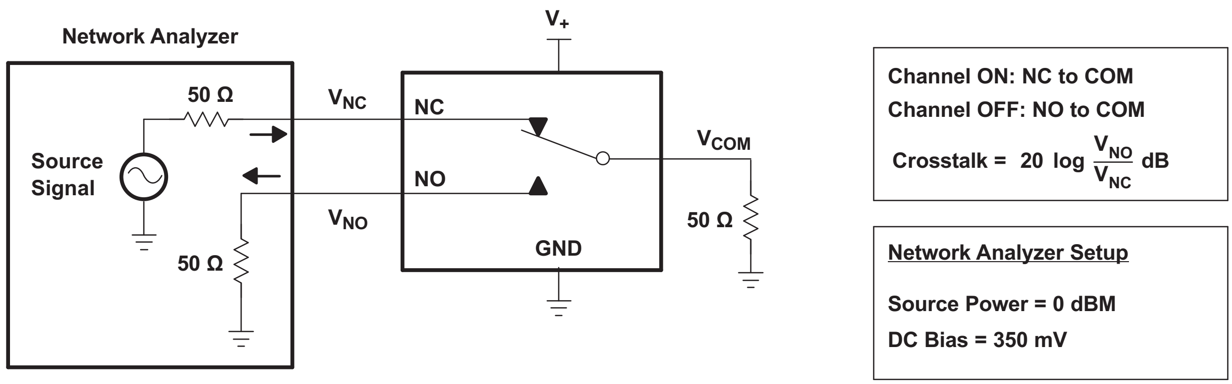


Figure 16. Crosstalk (X_{TALK})

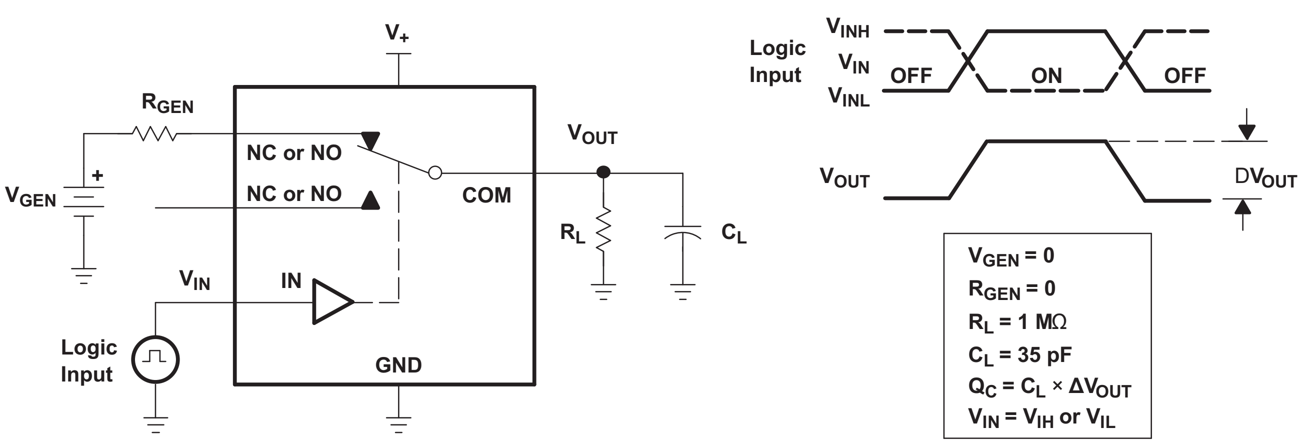


Figure 17. Charge Injection (Q_C)

Parameter Measurement Information (continued)

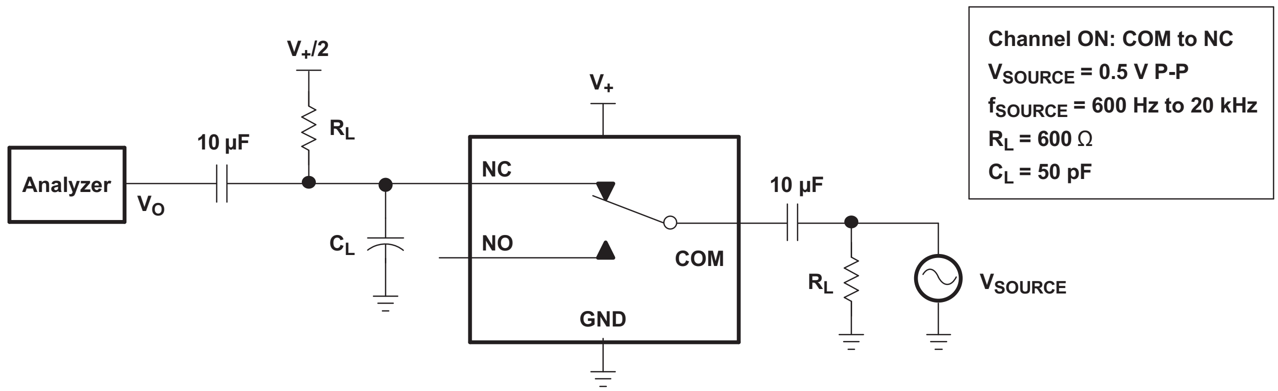


Figure 18. Total Harmonic Distortion (THD)

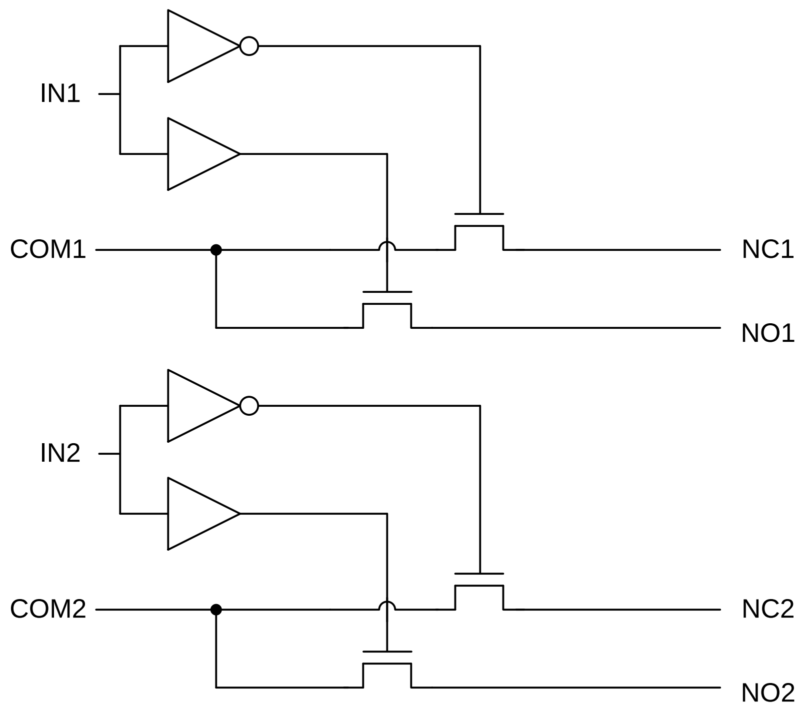
8 Detailed Description

8.1 Overview

The TS5A23157 is a dual single-pole-double-throw (SPDT) solid-state analog switch. The TS5A23157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin when the IN pin is low. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A23157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A23157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without V_{CC}.

8.4 Device Functional Modes

Table 1 lists the functional modes for TS5A23157.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

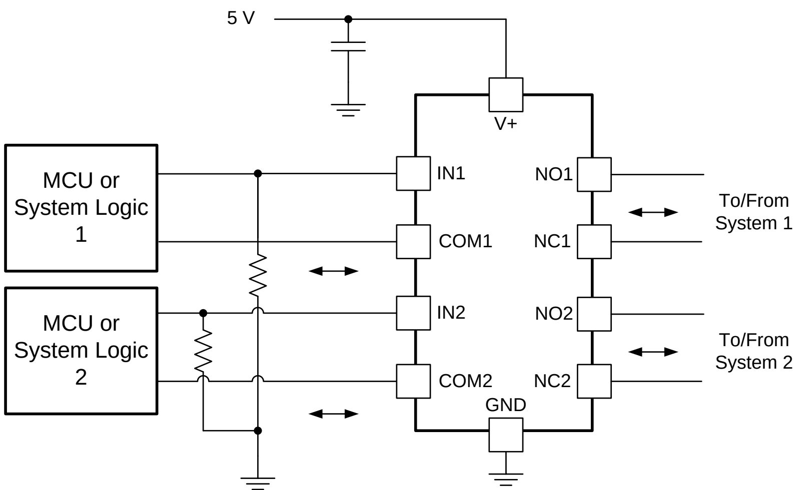


Figure 19. System Schematic for TS5A23157

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

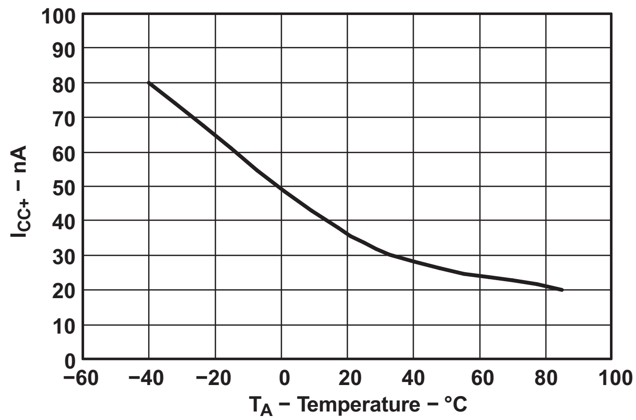


Figure 20. Power-Supply Current vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

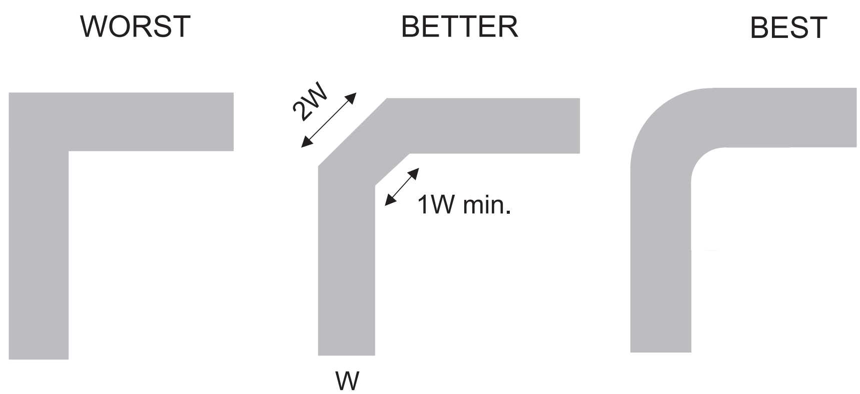


Figure 21. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulombs (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance and ΔV_O is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. OFF isolation, O_{ISO} = 20 LOG (V_{NC}/V_{COM}) dB, V_{COM} is the input and V_{NC} is the output.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured at a specific frequency and in dB. Crosstalk, X_{TALK} = 20 log (V_{NC1}/V_{NO1}), V_{NO1} is the input and V_{NC1} is the output.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the dc gain. Gain is measured from the equation, 20 log (V_{NC}/V_{COM}) dB, where V_{NC} is the output and V_{COM} is the input.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

Table 3. Summary of Characteristics

CONFIGURATION	2:1 MULTIPLEXER/DEMULTIPLEXER (2 × SPDT)
Number of channels	2
ON-state resistance (r_{on})	10 Ω
ON-state resistance match between channels (Δr_{on})	0.15 Ω
ON-state resistance flatness ($r_{on(flat)}$)	4 Ω
Turnon/turnoff time (t_{ON}/t_{OFF})	5.7 ns/3.8 ns
Break-before-make time (t_{BBM})	0.5 ns
Charge injection (Q_C)	7 pC
Bandwidth (BW)	220 MHz
OFF isolation (O_{SIO})	–65 dB at 10 MHz
Crosstalk 9XTALK)	–66 dB at 10 MHz
Total harmo nic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}$/$I_{NC(OFF)}$)	±1 µA
Package options	10-pin DGS and RSE

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23157DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)	Samples
TS5A23157DGSRE4	LIFEBUY	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)	
TS5A23157DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)	Samples
TS5A23157DGST	LIFEBUY	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	
TS5A23157RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS5A23157 :

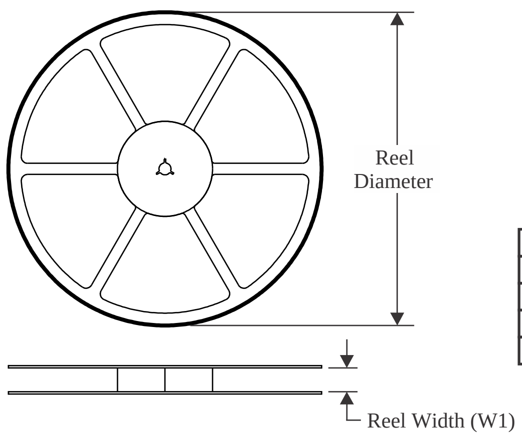
- Automotive : TS5A23157-Q1

NOTE: Qualified Version Definitions:

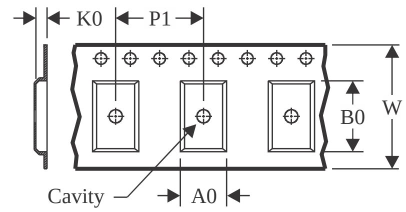
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

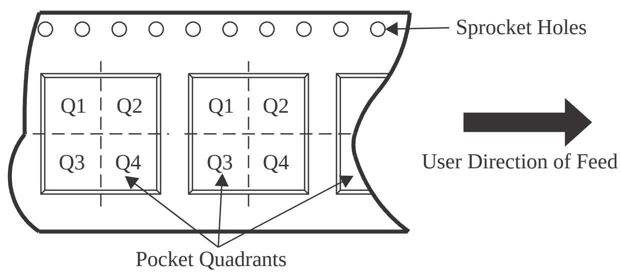


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

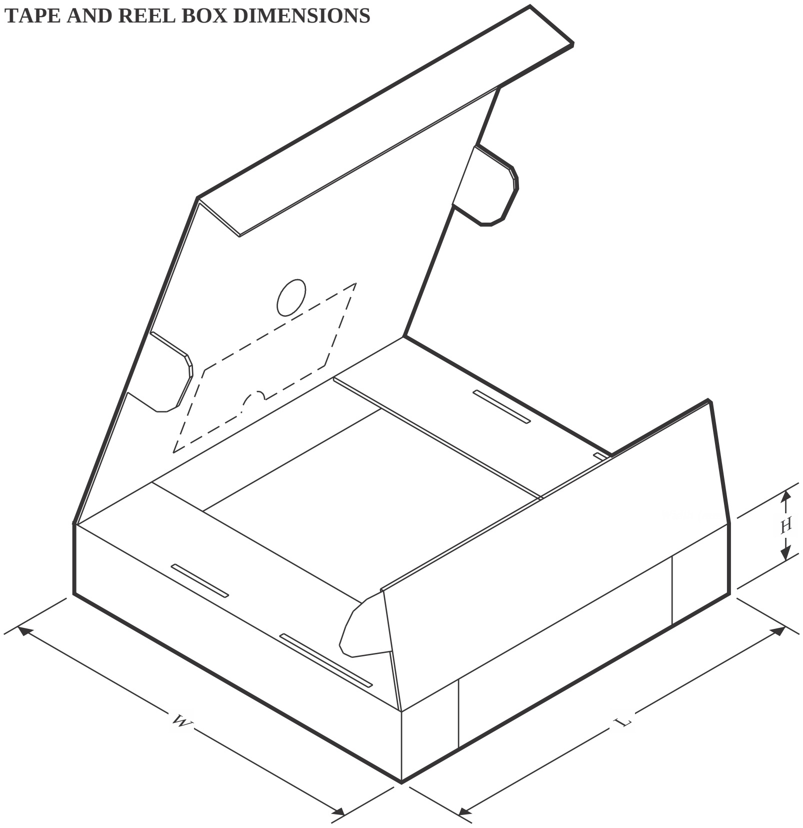
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

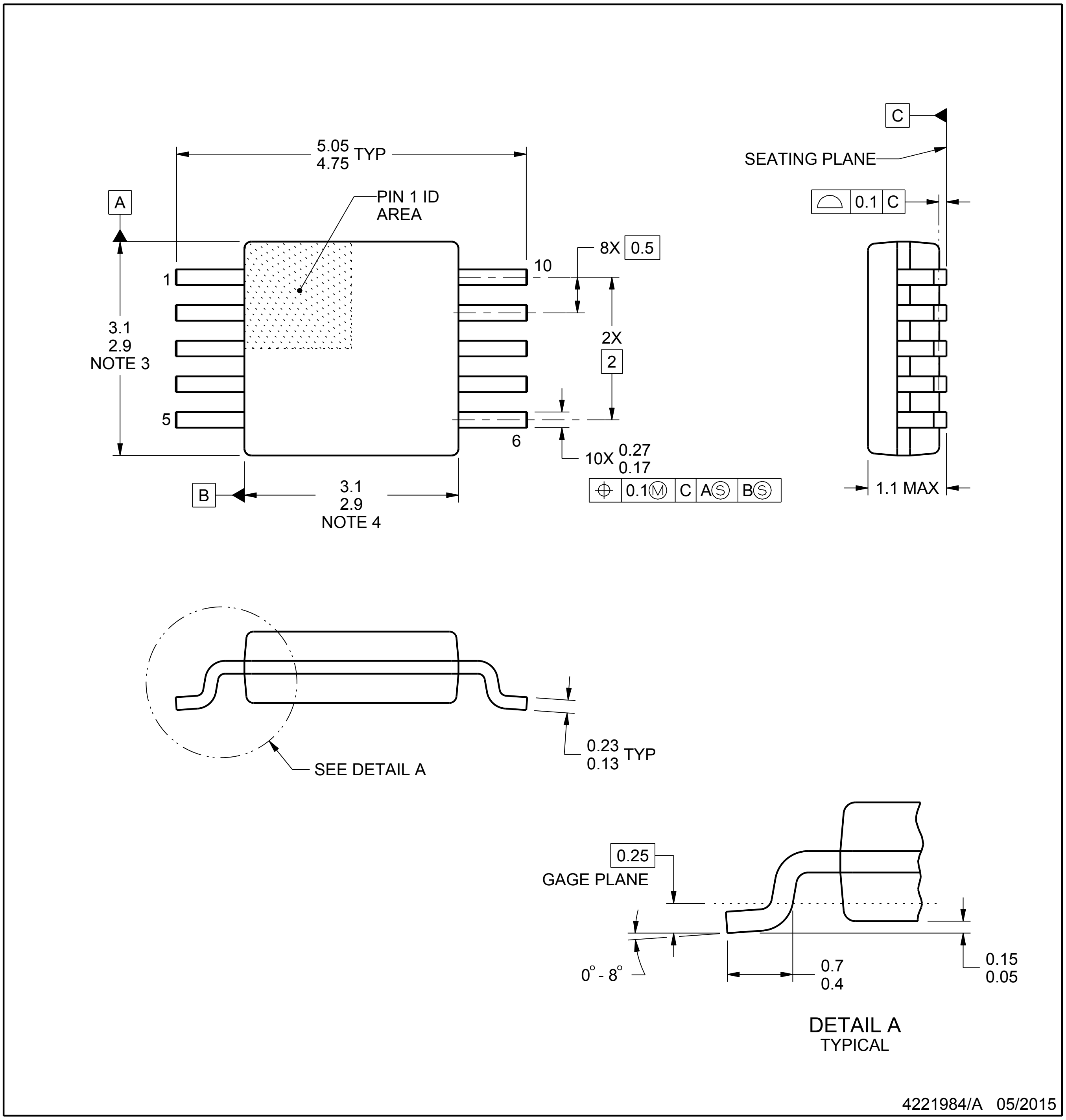
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23157DGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TS5A23157RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



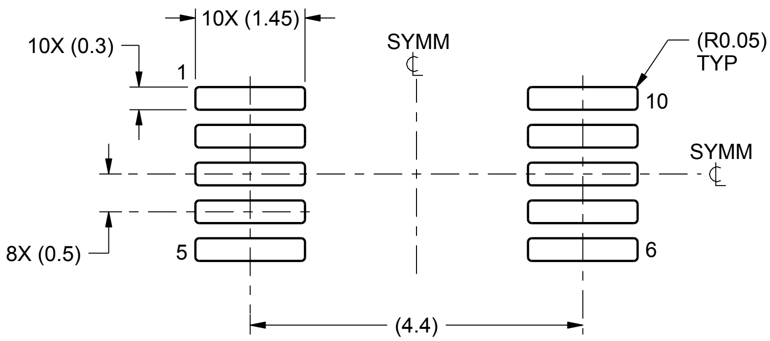
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TS5A23157DGST	VSSOP	DGS	10	250	203.0	203.0	35.0
TS5A23157RSER	UQFN	RSE	10	3000	189.0	185.0	36.0

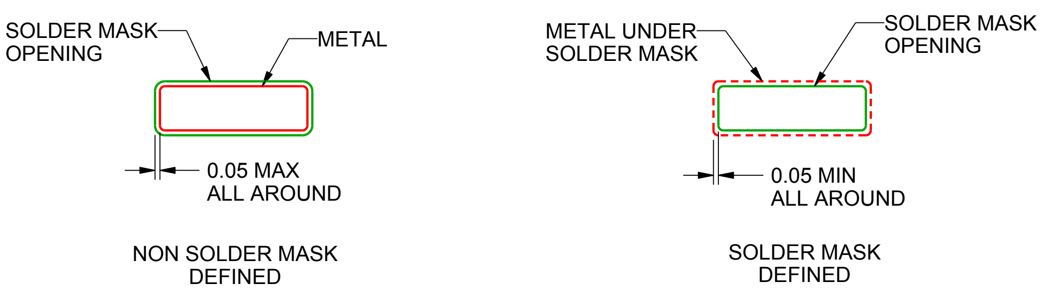


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

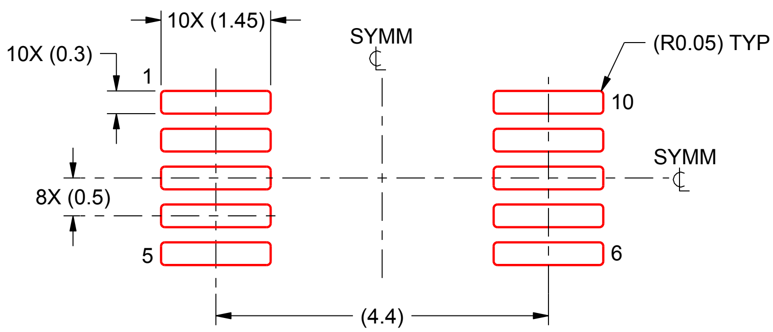


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

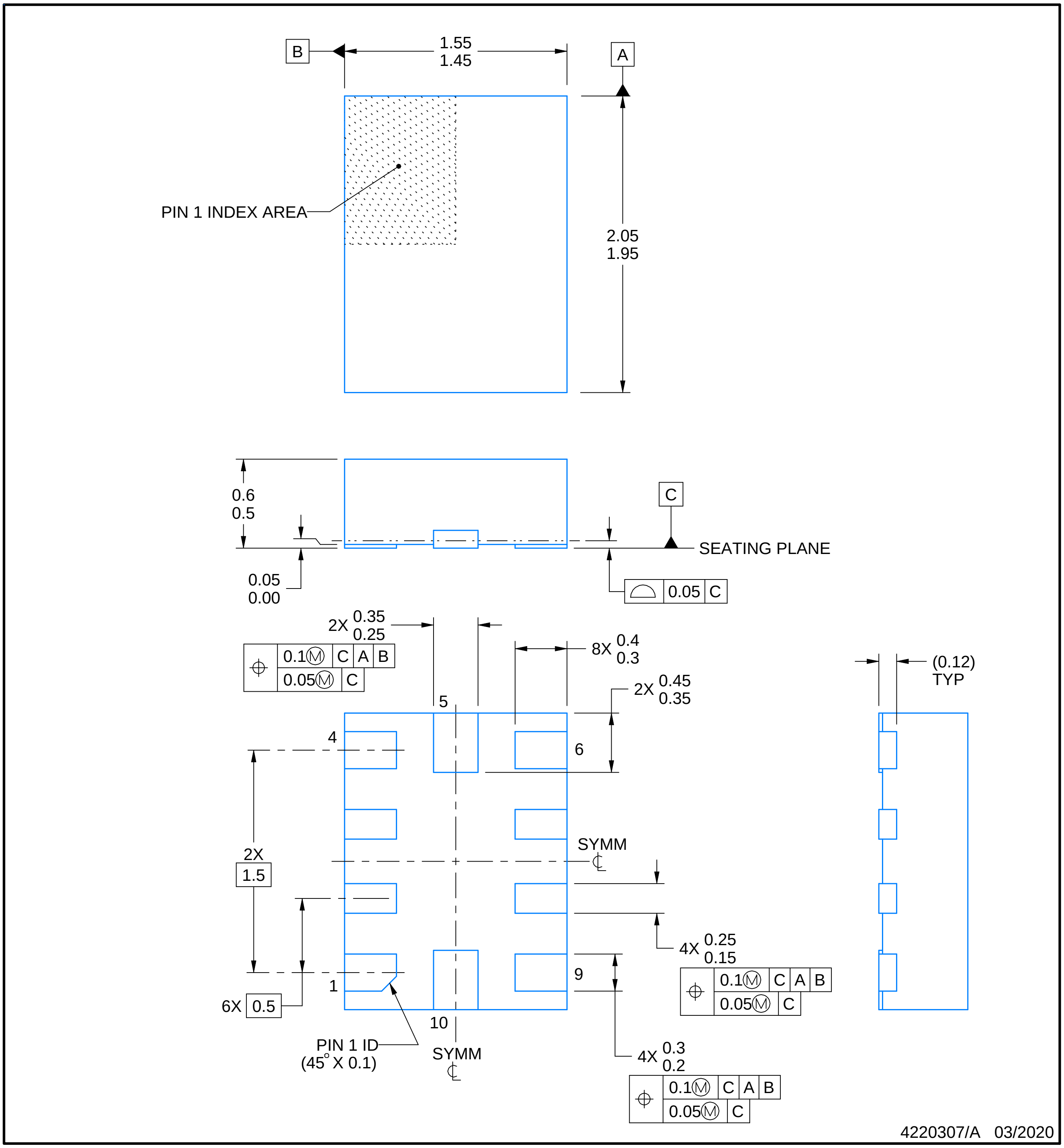
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RSE0010A

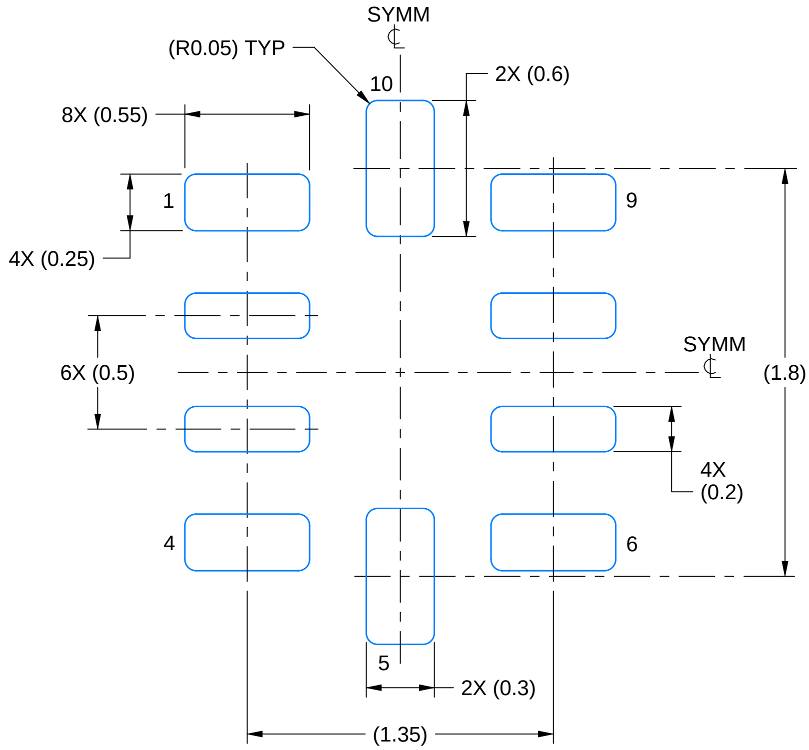
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

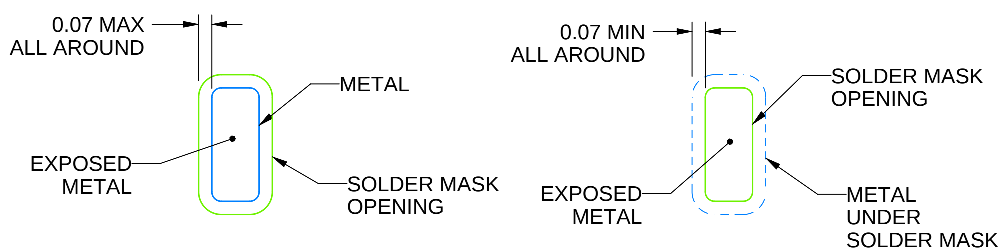


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

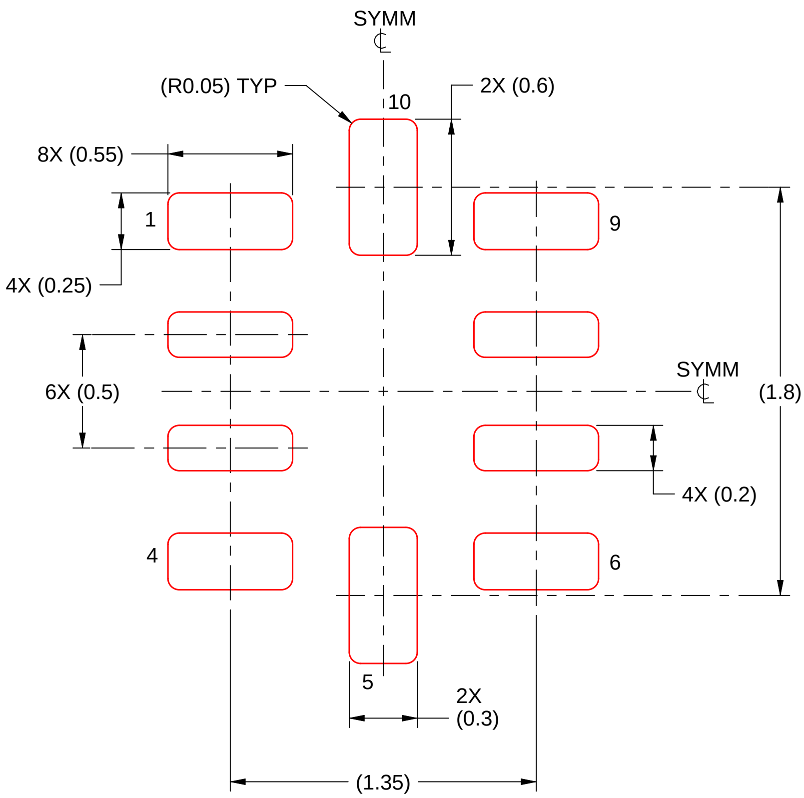
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.