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March 2015

FDD8444

N-Channel PowerTrench $^{\circledR}$ MOSFET 40V, 50A, 5.2m Ω

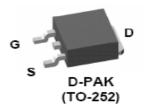
Features

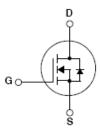
- Typ $r_{DS(on)}$ = 4m Ω at V_{GS} = 10V, I_D = 50A
- Typ $Q_{g(10)}$ = 89nC at V_{GS} = 10V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant



Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems





MOSFET Maximum Ratings $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
	Drain Current Continuous (V _{GS} = 10V) (Note	145	
I_D	Continuous (V_{GS} = 10V, with $R_{\theta JA}$ = 52°C/W)	20	Α
	Pulsed	Figure 4	
E _{AS}	Single Pulse Avalanche Energy (Note 2	2) 535	mJ
D	Power Dissipation	153	W
P_{D}	Derate above 25°C	1.02	W/°C
T_J , T_{STG}	Operating and Storage Temperature	-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.98	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO-252, 1in ² copper pad area	52	°C/W

Package Marking and Ordering Information

Parameter

Gate to Source Leakage Current

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8444	FDD8444	TO-252AA	13"	16mm	2500 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Off Cha	aracteristics					
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40	-	-	V
ı	Zero Gate Voltage Drain Current	V _{DS} = 32V	-	-	1	
DSS	Zero Gale Voltage Drain Current	$V_{00} = 0V$ $T_{1} = 150$	ეºC -	_	250	μΑ

 $V_{GS} = \pm 20V$

Test Conditions

Min

Тур

Max

±100

Units

On Characteristics

Symbol

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	2.5	4	V
		$I_D = 50A, V_{GS} = 10V$		4	5.2	
r _{DS(on)}	Drain to Source On Resistance	$I_D = 50A, V_{GS} = 10V,$ $T_J = 175^{\circ}C$	ı	7.2	9.4	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz	-	6195	-	pF	
C _{oss}	Output Capacitance		-	585	-	pF	
C _{rss}	Reverse Transfer Capacitance	- 1 - 11VII 12		-	332	-	pF
R_G	Gate Resistance	f = 1MHz		-	1.9	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V _{GS} = 0 to 10V		-	89	116	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0$ to 5V	7		43	56	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	$V_{GS} = 0 \text{ to } 2V$ $V_{DD} = 20V$	-	11	14.3	nC
Q_{gs}	Gate to Source Gate Charge		┘ I _D = 50A I _a = 1.0mA	-	23	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau		ig 1.0m/	-	11	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	20	-	nC

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units

Switching Characteristics

t _{on}	Turn-On Time		-	-	135	ns
t _{d(on)}	Turn-On Delay Time		-	12	-	ns
t _r	Turn-On Rise Time	$V_{DD} = 20V, I_D = 50A$	-	78	-	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10V, R_{GS} = 2 Ω	-	48	-	ns
t _f	Turn-Off Fall Time		-	15	-	ns
t _{off}	Turn-Off Time		-	-	95	ns

Drain-Source Diode Characteristics

V _{SD} Source to Drain Diode	Course to Drain Diade Voltage	I _{SD} = 50A	-	0.9	1.25	\/
	Source to Drain Diode Voltage	I _{SD} = 25A	-	0.8	1.0	V
t _{rr}	Reverse Recovery Time	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	39	51	ns
Q _{rr}	Reverse Recovery Charge		-	45	59	nC

Package current limitation is 50A.
 Starting T_J = 25°C, L = 0.67mH, I_{AS} = 40A

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

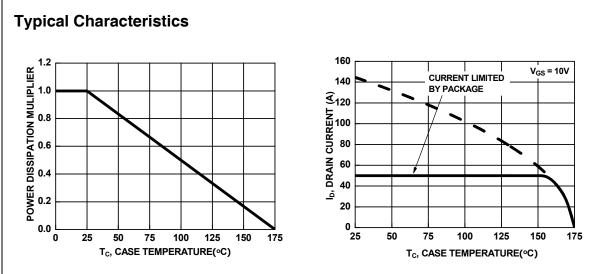


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

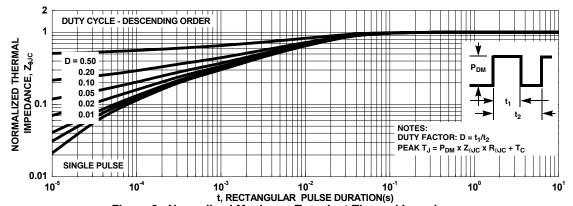


Figure 3. Normalized Maximum Transient Thermal Impedance

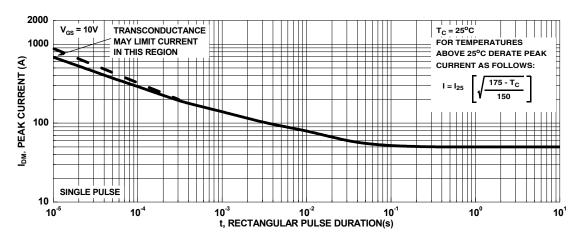


Figure 4. Peak Current Capability

Typical Characteristics

100

80

60

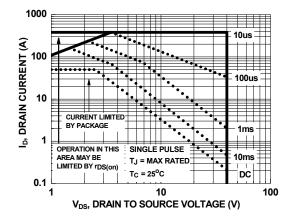
40

20

2.0

 $V_{DD} = 5\dot{V}$

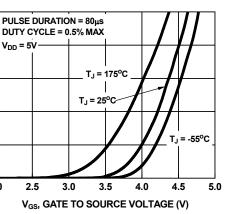
ID, DRAIN CURRENT (A)



500 $t_{AV} = (L)(I_{AS})/(1.3*RATED BV_{DSS})$ € $t_{AV} = (L/R)In[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) +1]$ IAS, AVALANCHE CURRENT 100 STARTING T_J = 25°C 10 STARTING T_J = 150° 0.01 0.1 10 100 1000 tAV, TIME IN AVALANCHE (ms)

Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to Fairchild Application Notes AN7514 and AN7515 Figure 6. Unclamped Inductive Switching Capability



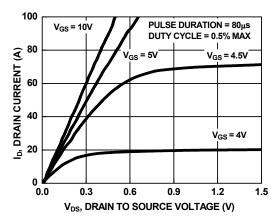
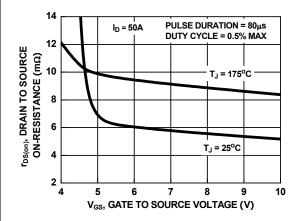


Figure 7. Transfer Characteristics

Figure 8. Saturation Characteristics



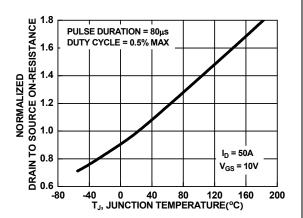


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

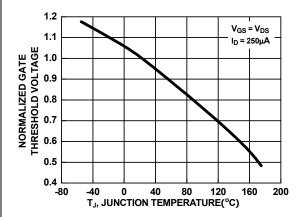


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

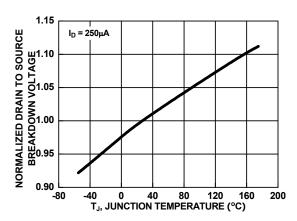


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

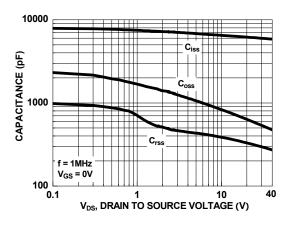


Figure 13. Capacitance vs Drain to Source Voltage

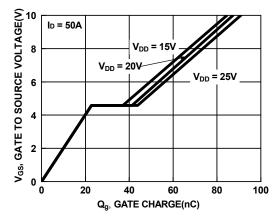


Figure 14. Gate Charge vs Gate to Source Voltage



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