3.3 VOLT CMOS ASYNCHRONOUS FIFO
512 x 9, 1,024 x 9,
2,048 x 9, 4,096 x 9,
8,192 x 9, 16,384 x 9

IDT72V01, IDT72V02
IDT72V03, IDT72V04
IDT72V05, IDT72V06

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES:

- **3.3V family uses less power than the 5 Volt 7201/7202/7203/7204/7205/7206 family**
- **512 x 9 organization (72V01)**
- **1,024 x 9 organization (72V02)**
- **2,048 x 9 organization (72V03)**
- **4,096 X 9 organization (72V04)**
- **8,192 x 9 organization (72V05)**
- **16,384 X 9 organization (72V06)**
- **Functionally compatible with 720x family**
- **Low-power consumption**
  - *— Active: 180 mW (max.)*
  - *— Power-down: 18 mW (max.)*
- **15 ns access time**
- **Asynchronous and simultaneous read and write**
- **Fully expandable by both word depth and/or bit width**
- **Status Flags: Empty, Half-Full, Full**
- **Auto-retransmit capability**
- **Available in 32-pin PLCC**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**

DESCRIPTION:

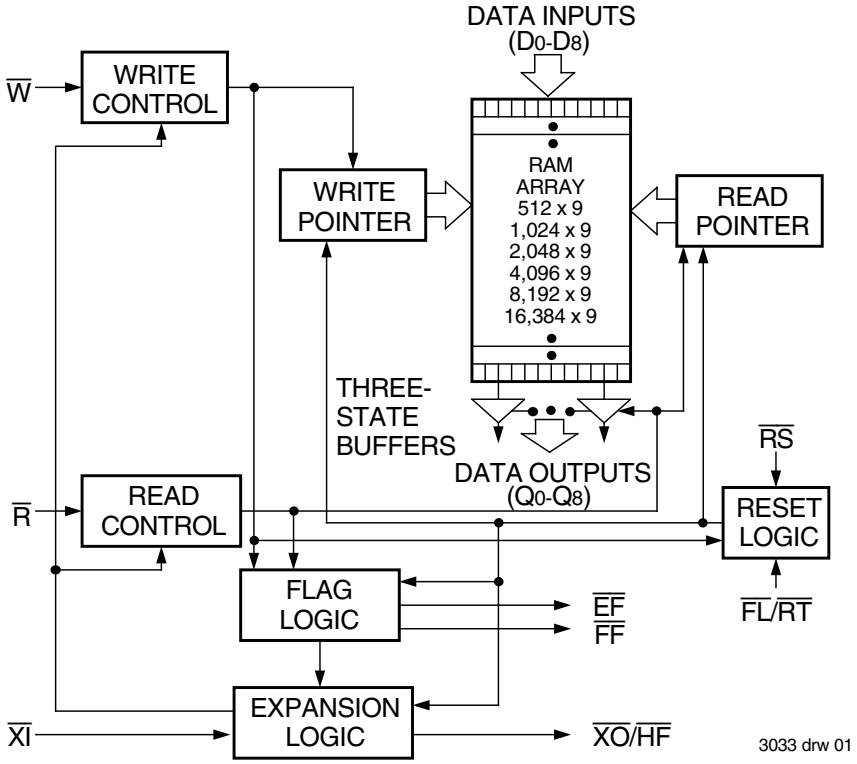
The IDT72V01/72V02/72V03/72V04/72V05/72V06 are dual-port FIFO memories that operate at a power supply voltage (Vcc) between 3.0V and 3.6V. Their architecture, functional operation and pin assignments are identical to those of the IDT7201/7202/7203/7204/7205/7206. These devices load and empty data on a first-in/first-out basis. They use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a maximum data access time as fast as 25 ns.

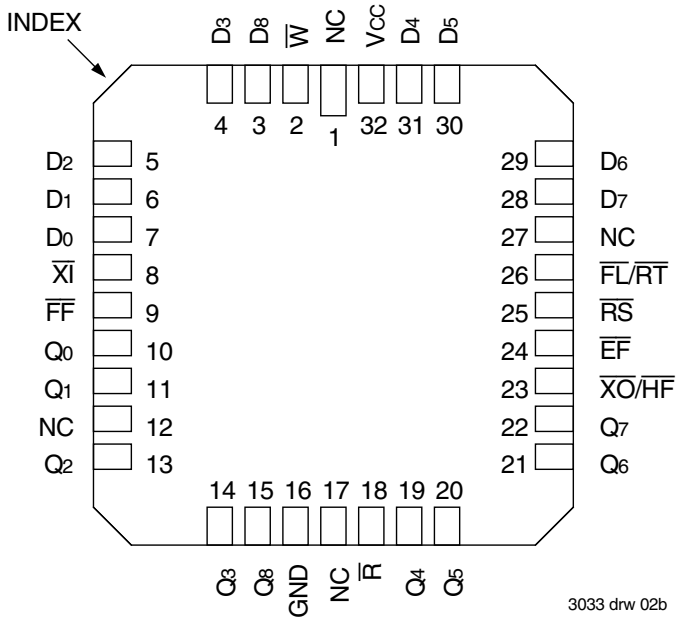
The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. They also feature a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed LOW to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

These FIFOs are fabricated using high-speed CMOS technology. It has been designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PLCC (J32-1, order code: J)
TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Rating	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}[1]	Input High Voltage	2.0	—	V_{CC}+0.5	V
V_{IL}[2]	Input Low Voltage	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Industrial	–40	—	85	°C

NOTES:
1. For $\overline{RT}/\overline{RS}/\overline{XI}$ input, V_{IH} = 2.6V (commercial).
   For $\overline{RT}/\overline{RS}/\overline{XI}$ input, V_{IH} = 2.8V (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C; Industrial: V_{CC} = 3.3V ± 0.3V, T_A = –40°C to +85°C)

Symbol	Parameter	IDT72V01 IDT72V02 IDT72V03 IDT72V04 Commercial & Industrial[1] t_A = 15, 25, 35 ns		IDT72V05 IDT72V06 Commercial & Industrial[1] t_A = 15, 25, 35 ns		Unit
		Min.	Max.	Min.	Max.	
I_{LI}[2]	Input Leakage Current (Any Input)	–1	1	–1	1	µA
I_{LO}[3]	Output Leakage Current	–10	10	–10	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	0.4	—	0.4	V
I_{CC1}[4,5]	Active Power Supply Current	—	60	—	75	mA
I_{CC2}[4,6]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	5	—	5	mA

NOTES:
1. Industrial temperature range product for the 25ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
3. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. Tested with outputs open (I_{OUT} = 0).
5. Tested at f = 20 MHz.
6. All Inputs = V_{CC} - 0.2V or GND + 0.2V.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1]

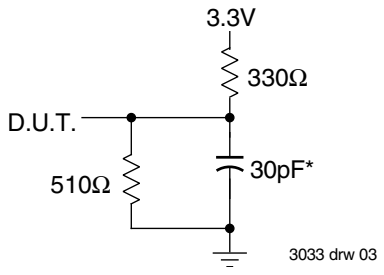
(Commercial: V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C; Industrial: V_{CC} = 3.3V ± 0.3V, T_A = –40°C to +85°C)

		Commercial		Com'l and Ind'l[2]		Commercial		
		IDT72V01L15 IDT72V02L15 IDT72V03L15 IDT72V04L15 IDT72V05L15 IDT72V06L15		IDT72V01L25 IDT72V02L25 IDT72V03L25 IDT72V04L25 IDT72V05L25 IDT72V06L25		IDT72V01L35 IDT72V02L35 IDT72V03L35 IDT72V04L35 IDT72V05L35 IDT72V06L35		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Shift Frequency	—	40	—	28.5	—	22.2	MHz
t_{RC}	Read Cycle Time	25	—	35	—	45	—	ns
t_A	Access Time	—	15	—	25	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[3]	15	—	25	—	35	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[4]	3	—	3	—	3	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[4,5]	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[4]	—	15	—	18	—	20	ns
t_{WC}	Write Cycle Time	25	—	35	—	45	—	ns
t_{WPW}	Write Pulse Width[3]	15	—	25	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	ns
t_{DS}	Data Setup Time	11	—	15	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	25	—	35	—	45	—	ns
t_{RS}	Reset Pulse Width[3]	15	—	25	—	35	—	ns
t_{RSS}	Reset Setup Time[4]	15	—	25	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	25	—	35	—	45	—	ns
t_{RT}	Retransmit Pulse Width[3]	15	—	25	—	35	—	ns
t_{RTS}	Retransmit Setup Time[4]	15	—	25	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	25	—	35	—	45	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	25	—	35	—	45	ns
t_{RTF}	Retransmit Low to Flags Valid	—	25	—	35	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	15	—	25	—	30	ns
t_{RFF}	Read High to Full Flag High	—	15	—	25	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	15	—	25	—	35	—	ns
t_{WEF}	Write High to Empty Flag High	—	15	—	25	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	15	—	25	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	25	—	35	—	45	ns
t_{RHF}	Read High to Half-Full Flag High	—	25	—	35	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	15	—	25	—	35	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	15	—	25	—	35	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	15	—	25	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[3]	15	—	25	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Setup Time	10	—	10	—	10	—	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for the 25ns speed grade is available as a standard device. All other speed grades are available by special order.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN ($D_0 - D_8$)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to HIGH after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs ($Q_0 - Q_8$) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

These FIFOs can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 512/1,024/2,048/4,096/8,192/16,384 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go LOW after 512/1,024/2,048/4,096/8,192/16,384 writes to the IDT72V01/72V02/72V03/72V04/72V05/72V06.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

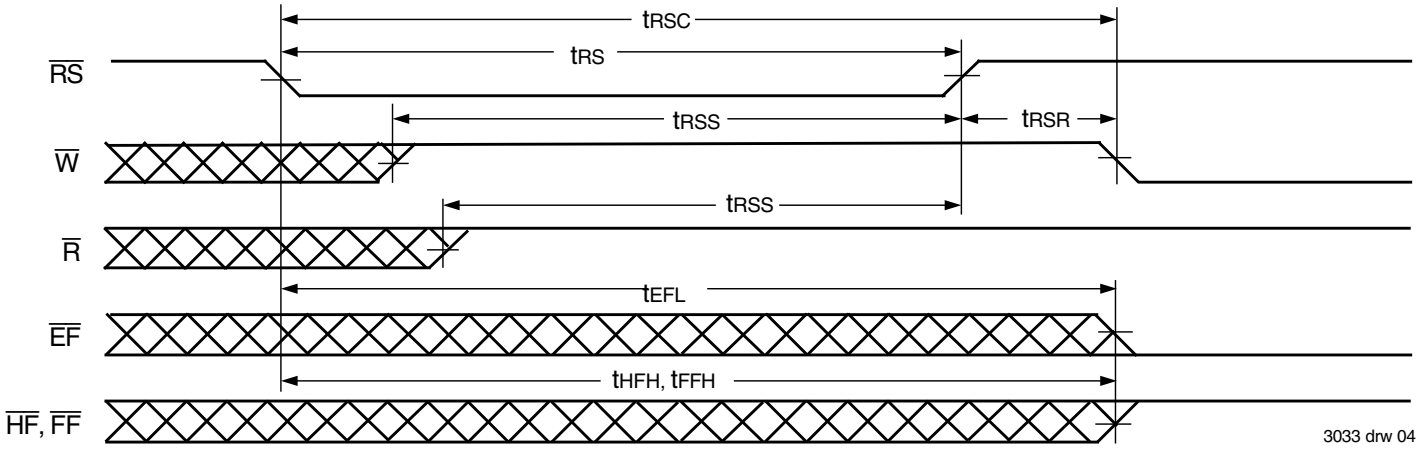
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS ($Q_0 - Q_8$)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a HIGH state.



NOTES:
1. EF, FF, HF may change status during Reset, but flags will be valid at tRSC.
2. W and R = VIH around the rising edge of RS.

Figure 2. Reset

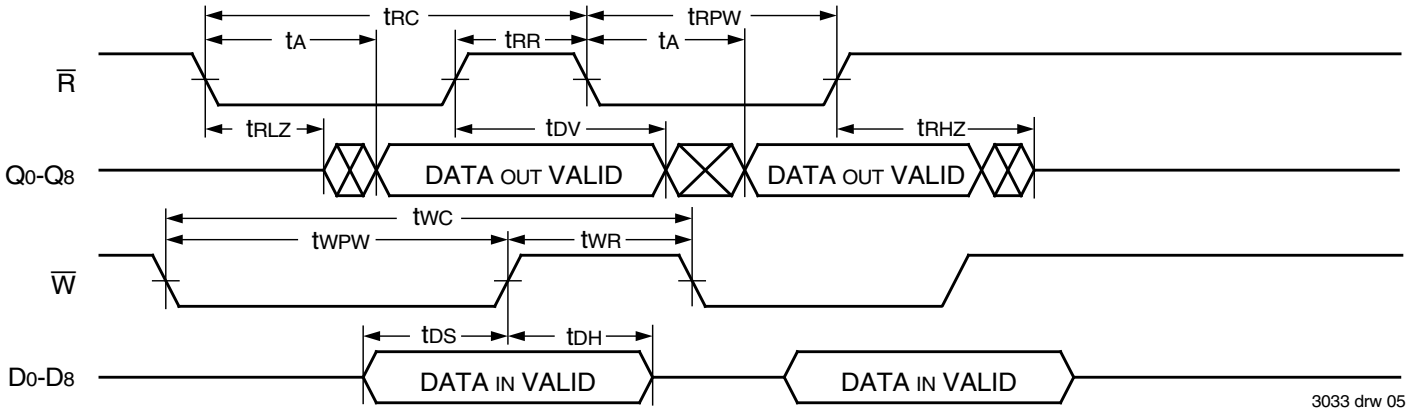


Figure 3. Asynchronous Write and Read Operation

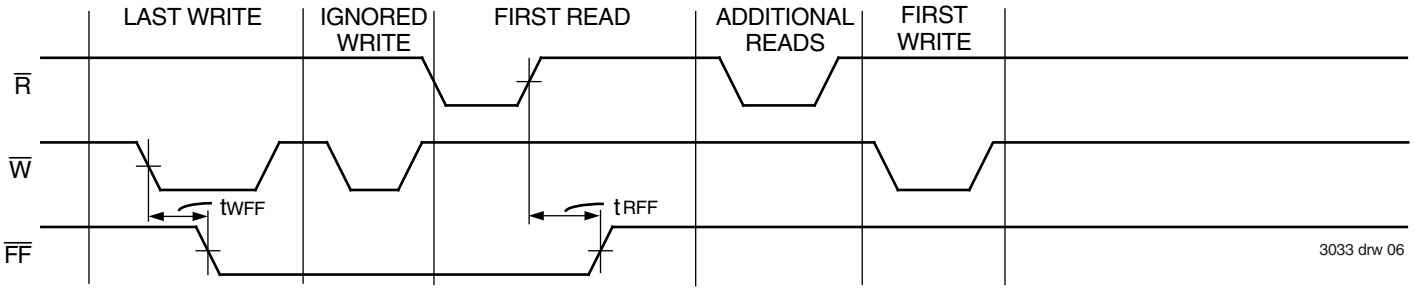


Figure 4. Full Flag From Last Write to First Read

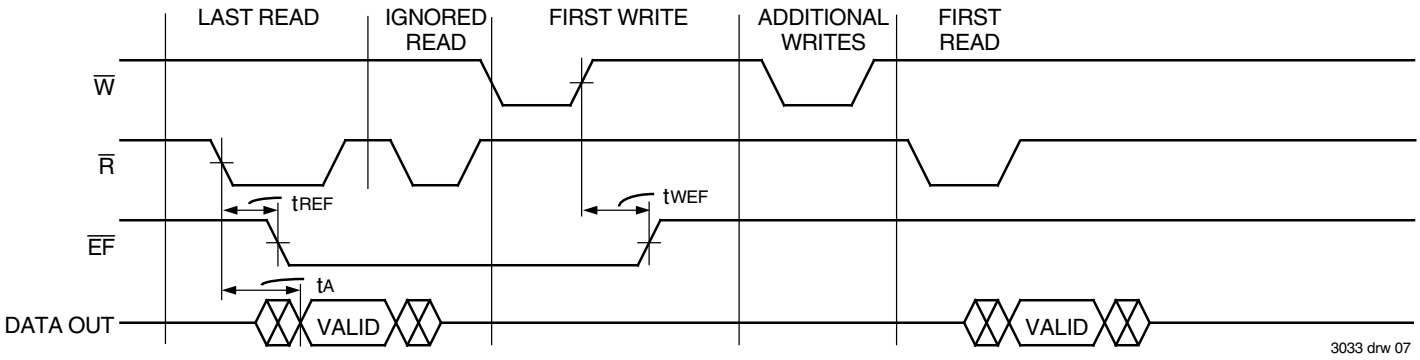


Figure 5. Empty Flag From Last Read to First Write

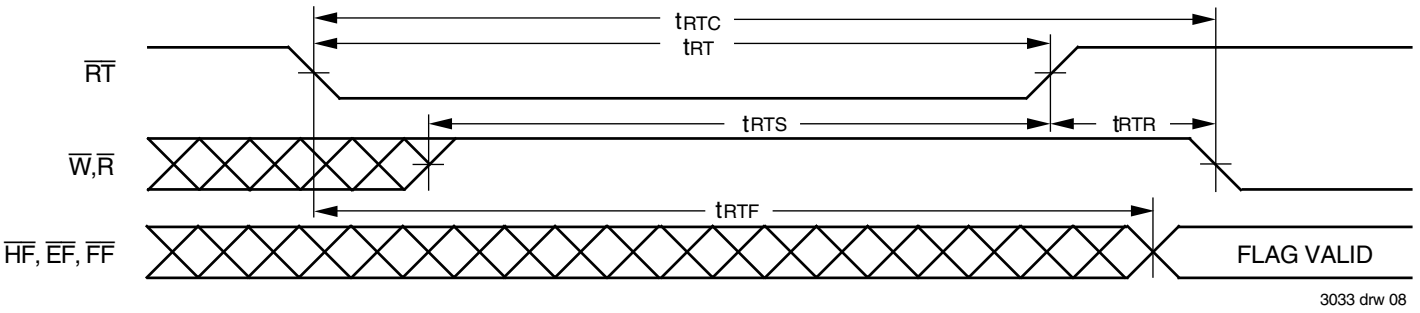


Figure 6. Retransmit

Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

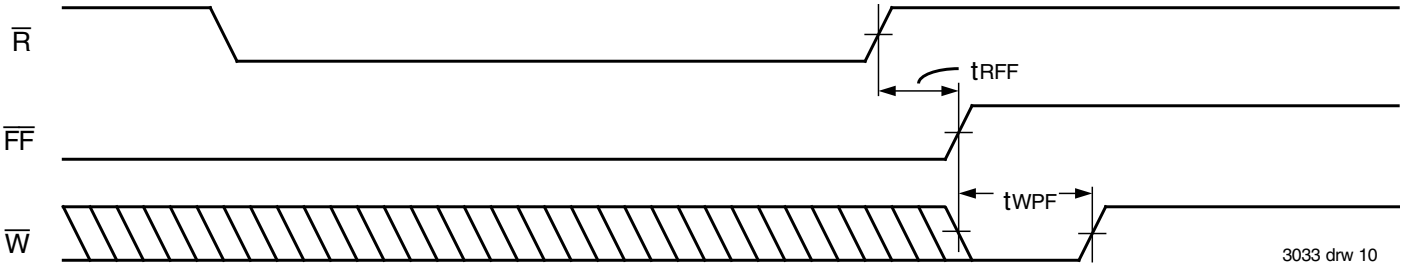


Figure 8. Minimum Timing for a Full Flag Coincident Write Pulse

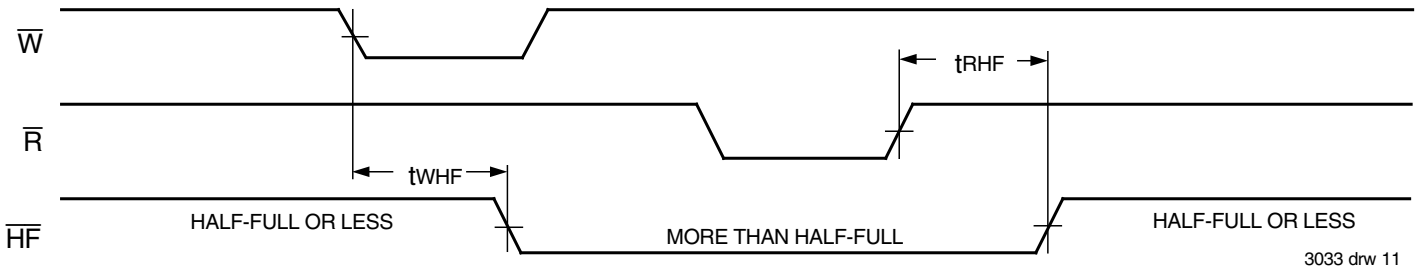


Figure 9. Half-Full Flag Timing

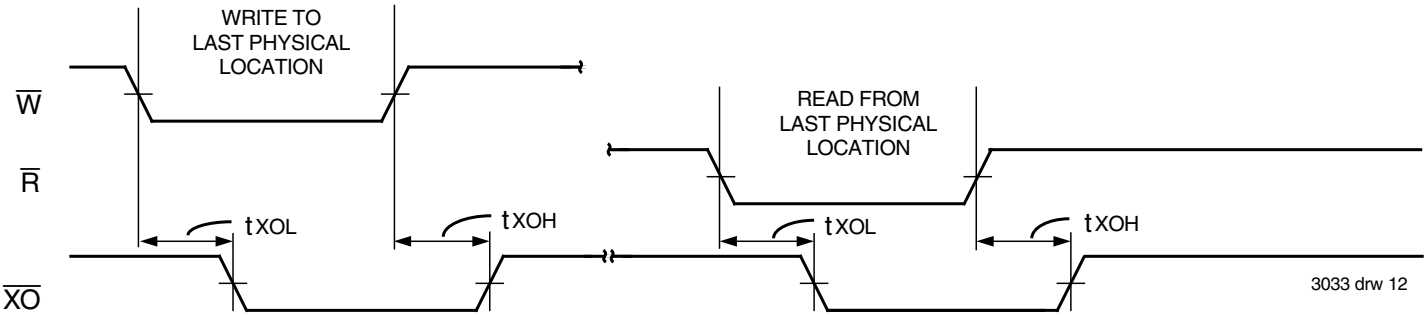


Figure 10. Expansion Out

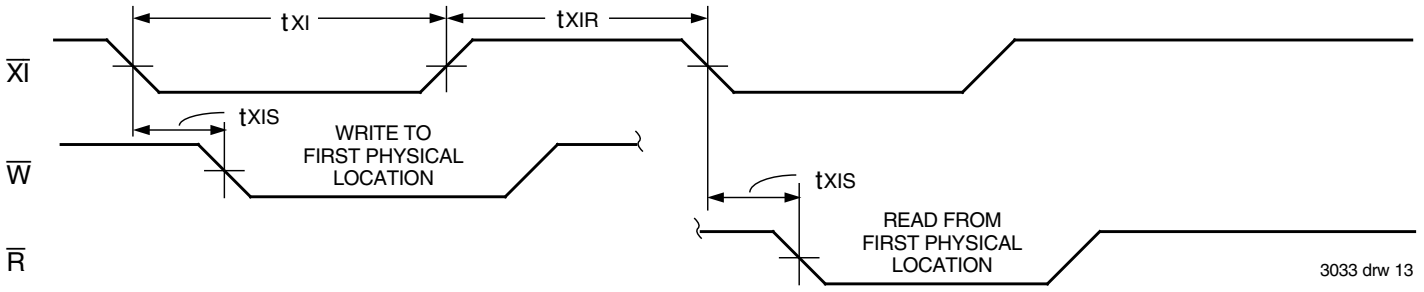


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

SINGLE DEVICE MODE

A single IDT72V01/72V02/72V03/72V04/72V05/72V06 may be used when the application requirements are for 512/1,024/2,048/4,096/8,192/16,384 words or less. These devices are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

These FIFOs can easily be adapted to applications when the requirements are for greater than 512/1,024/2,048/4,096/8,192/16,384 words. Figure 14 demonstrates Depth Expansion using three IDT72V01/72V02/72V03/72V04/72V05/72V06s. Any depth can be attained by adding additional IDT72V01/72V02/72V03/72V04/72V05/72V06s. These devices operate in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT72V01/72V02/72V03/72V04/72V05/72V06s. Any word width can be attained by adding additional IDT72V01/72V02/72V03/72V04/72V05/72V06s (Figure 13).

BIDIRECTIONAL OPERATION

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72V01/72V02/72V03/72V04/72V05/72V06s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

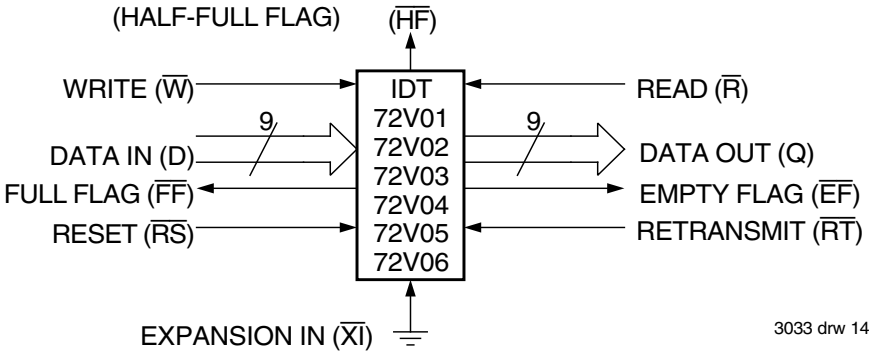


Figure 12. Block Diagram of Single 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9, 8,192 x 9 and 16,384 x 9 FIFO

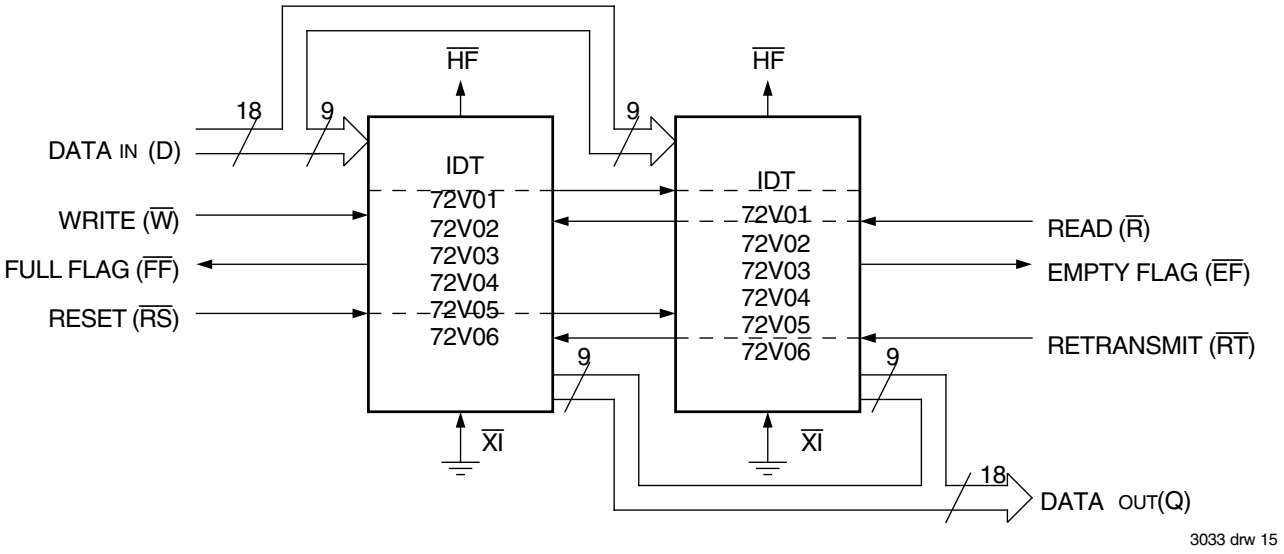


Figure 13. Block Diagram of 512 x 18, 1,024 x 18, 2,048 x 18, 4,096 x 18, 8,192 x 18 and 16,384 x 18 FIFO Memory Used in Width Expansion Mode

TABLE 1 — RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if flag is HIGH

TABLE 2 — RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

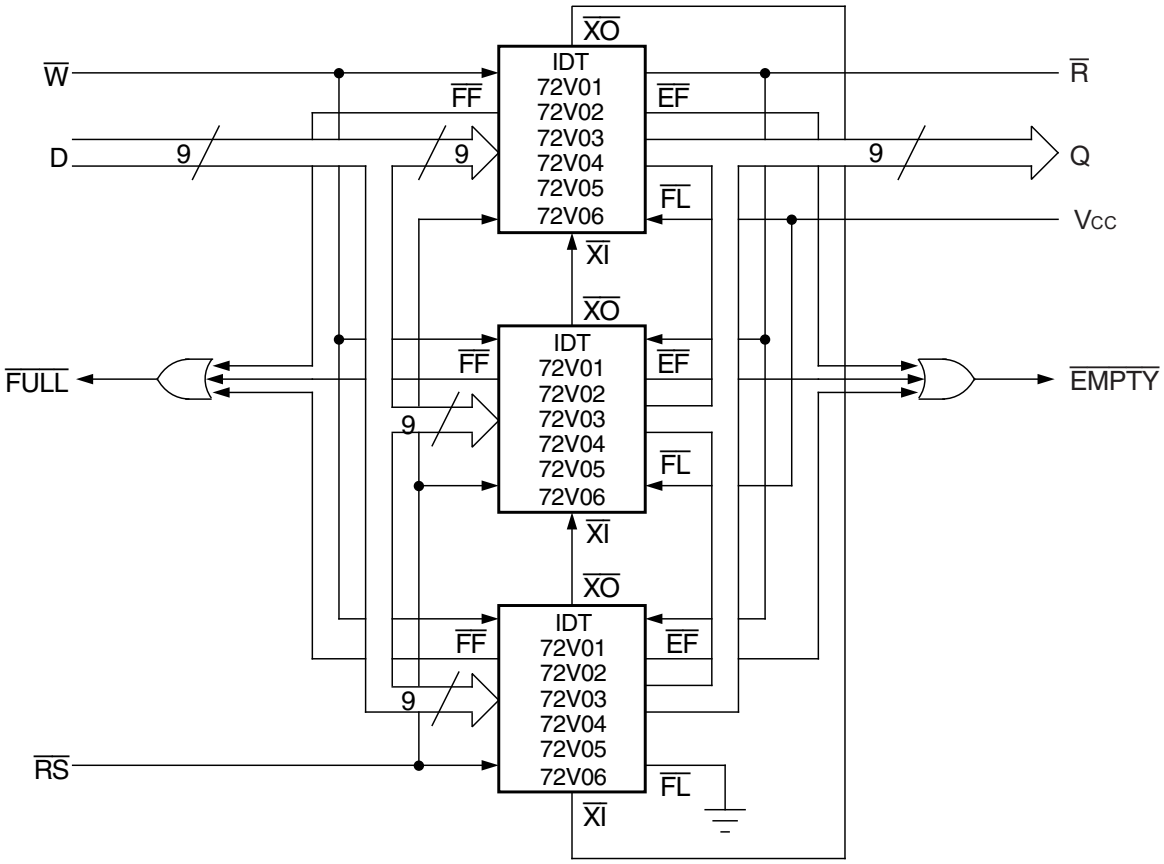
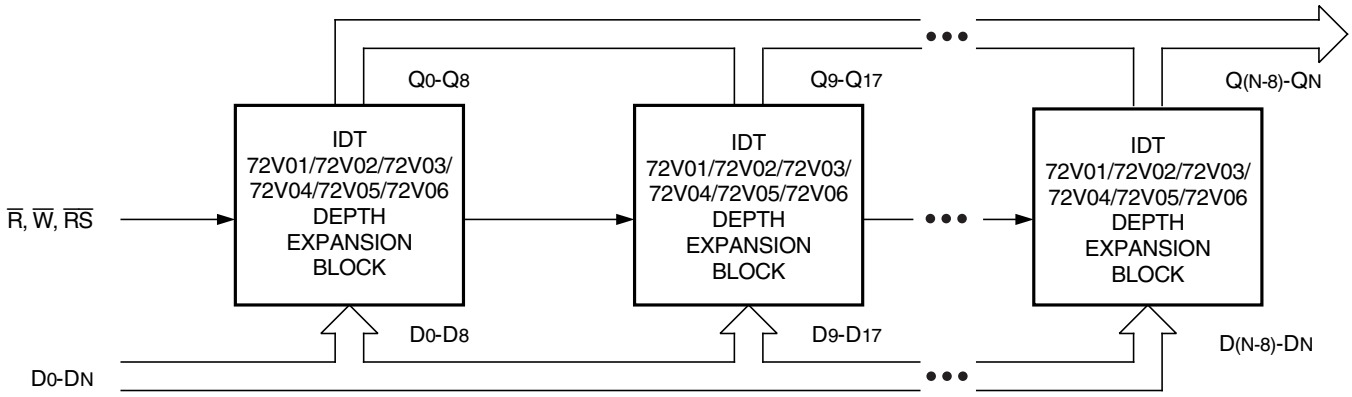


Figure 14. Block Diagram of 1,536 x 9, 3,072 x 9, 6,144 x 9, 12,288 x 9, 24,576 x 9 and 49,152 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

3033 drw 17

Figure 15. Compound FIFO Expansion

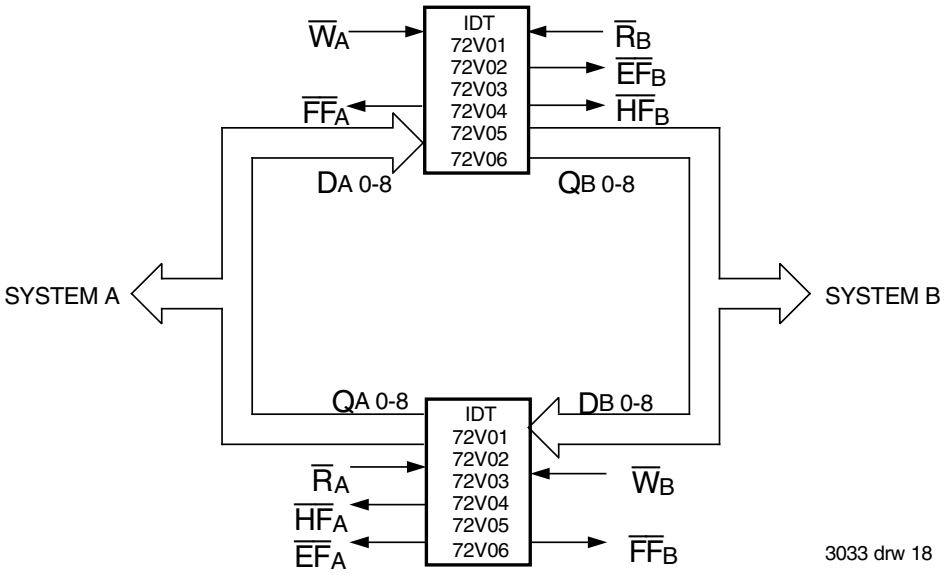


Figure 16. Bidirectional FIFO Mode

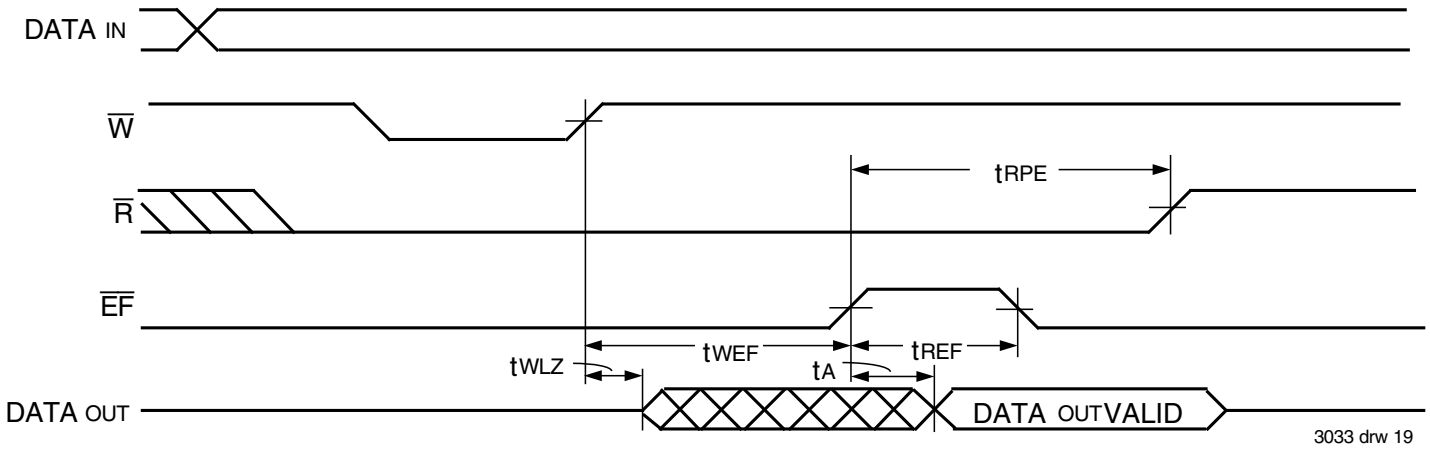


Figure 17. Read Data Flow-Through Mode

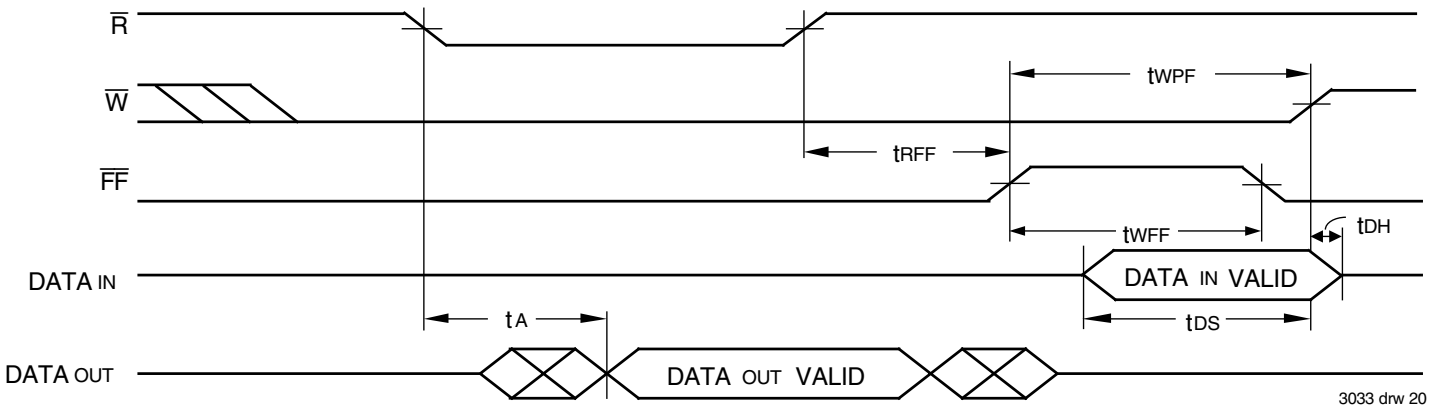
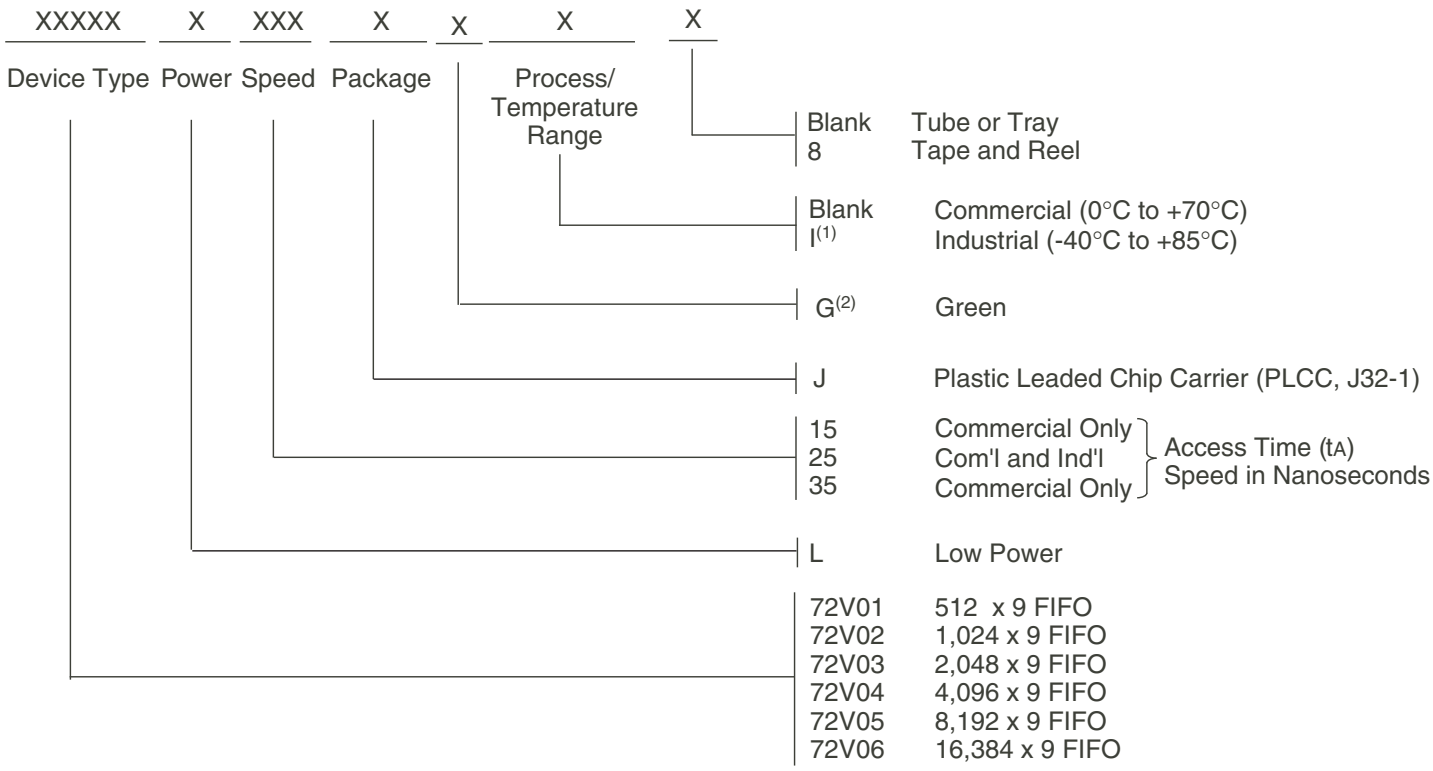


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



3033 drw 21

NOTES:

1. Industrial temperature range product for the 25ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages contact your local sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

DATASHEET DOCUMENT HISTORY

08/29/2001	pg. 3.
04/08/2003	pg. 2.
05/05/2003	pg. 2.
03/09/2006	pgs. 1 and 12.
10/22/2008	pgs. 12.
06/29/2012	pgs. 1 and 12.
11/27/2017	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
408-360-1753
email: FIFOhelp@idt.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

IDT (Integrated Device Technology):

72V02L25J 72V05L15JG 72V02L15J 72V01L25JI 72V06L25J 72V02L35J 72V06L15J 72V06L35J 72V03L25J8 72V06L25JI 72V04L25J 72V02L35J8 72V04L35J8 72V01L15J8 72V04L15J 72V04L35J 72V03L25JGI8 72V05L25JGI8 72V02L25JGI8 72V06L25JGI8 72V05L25J8 72V01L35J8 72V05L35J 72V05L25J 72V04L25JI 72V05L15J 72V04L15J8 72V03L25J 72V03L15J 72V03L35J 72V03L25JI 72V02L15JG 72V02L25J8 72V03L15JG 72V06L15JG 72V01L35J 72V01L25J 72V06L25JGI 72V02L25JGI 72V04L25JGI 72V05L25JGI 72V02L15JG8 72V03L15JG8 72V01L15JG8 72V04L15JG8 72V06L15JG8 72V05L15JG8 72V03L25JGI 72V05L15J8 72V04L25J8 72V02L25JI 72V01L15J 72V01L15JG 72V05L25JI8 72V03L25JI8 72V02L25JI8 72V06L25JI8 72V04L25JI8 72V01L25JI8 72V02L15J8 72V05L35J8 72V06L35J8 72V03L15J8 72V06L25J8 72V04L25JGI8 72V05L25JI 72V04L15JG 72V01L25J8 72V06L15J8 72V03L35J8 72V01L25JGI8 72V01L25JGI