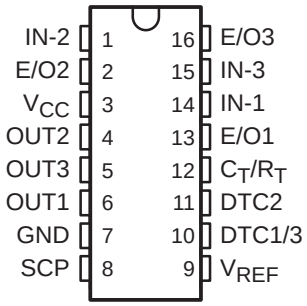
- **Low Voltage Operation . . . 2.5 V to 7 V**
- **Low Power . . . 3. 5 mA (f = 500 kHz, Duty = 50%)**
- **Internal Undervoltage Lockout Protection**
- **Internal Short Circuit Protection**
- **Wide Operating Frequency . . . 50 kHz to 1 MHz**
- **Internal Precision Reference . . . 1.25 V ±1% (25°C)**
- **On/Off Switch for CH1/3 Pair and Ch2 (see Function Table)**
- **0 to 100% Dead Time Control**
- **Totem Pole Output Stage**
- **Smal l Package . . . 16 Pin TSSOP**

PW PACKAGE
(TOP VIEW)



description

The TPS5100 is a triple PWM control circuit, primarily designed to compose the power supply for LCD display. Each PWM channel has own error amplifier, PWM comparator, dead-time control and output driver. The trimmed voltage reference, oscillator, undervoltage lockout and short circuit protection are common for all channels.

This device includes two boost exclusive circuits (ch1,3) and a buck-boost exclusive circuit (ch2). The operating frequency is set with external resister and capacitor, and dead time is continuously adjustable form 0% to 100% duty cycle with resistive divider network. Soft start function can be implemented by adding a capacitor to dead time divider network. Two dead time control inputs are assigned for ch1,3 pair and ch2 individually and each dead time control input can be used to control on/off operation. TPS5100 can operate from 2.5 V supply voltage and ch1,3 pair and ch2 operate with reverse phase switching each other to achieve efficient operation in low power and battery powered system.

The TPS5100 is characterized for operation from –20°C to 85°C.

FUNCTION TABLE

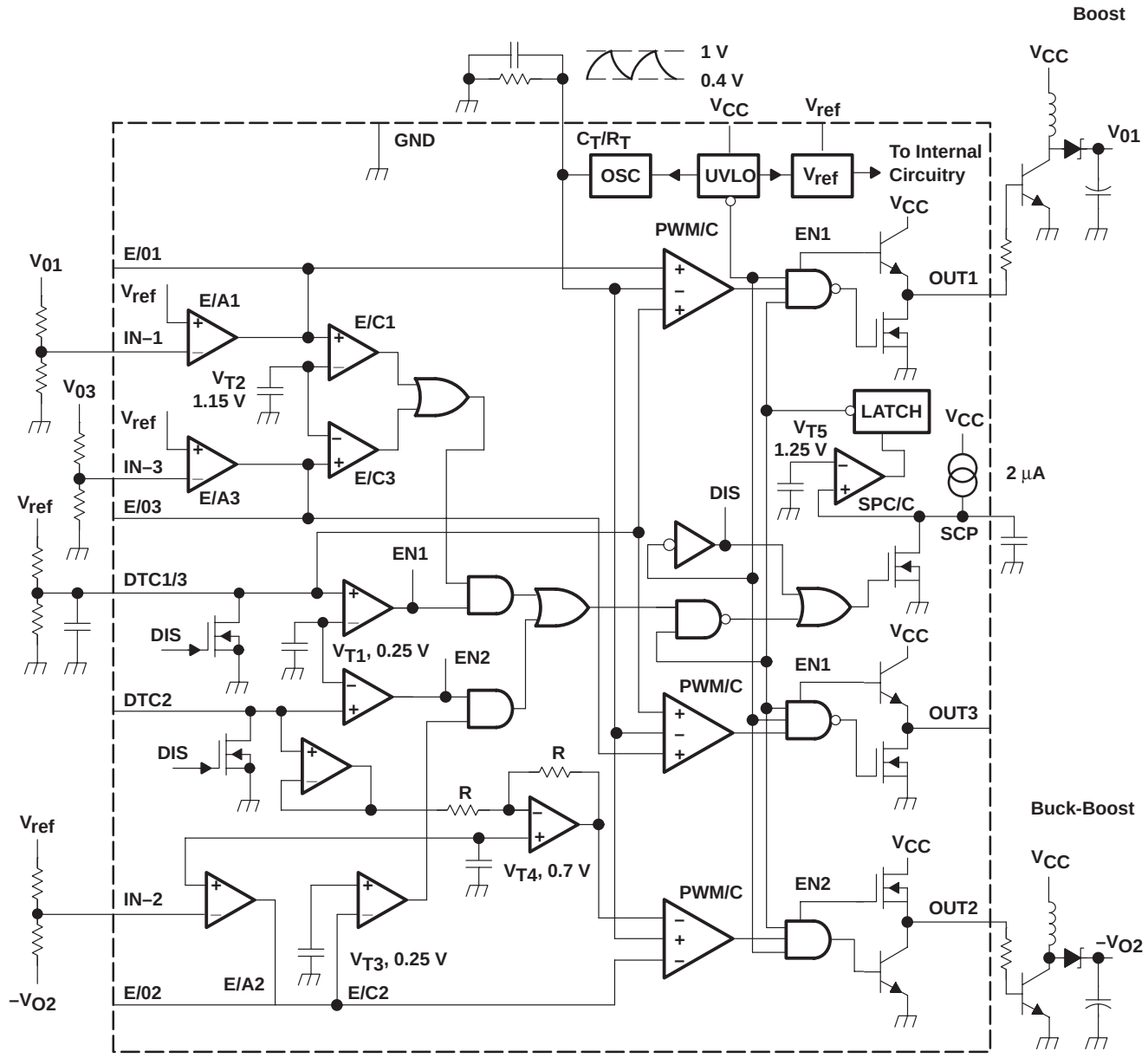
CONDITION	OUTPUT		
	CH-1	CH-2	CH-3
DTC1/3 >. 0.3 V, DTC2 > 0.3 V	ON H	ON L	ON H
DTC1/3 > 0.3 V, DTC2 <. 0.2 V	ON H	OFF H	ON H
DTC1/3 < 0.2 V, DTC2 > 0.3 V	OFF L	ON L	OFF L
DTC1/3 < 0.2 V, DTC2 < 0.2 V	OFF L	OFF H	OFF L

AVAILABLE OPTIONS

T_A	PACKAGE
	TSSOP (PW)
–20°C to 85°C	TPS5100PW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



NOTE A: All voltages and currents listed are nominal.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V (unless otherwise noted) (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	I_{REF} = –1 mA,	T_A = 25°C	1.237	1.250	1.263	V
$V_{REF(dev)}$	Reference voltage change with T_A	I_{REF} = –1 mA,	See Note 2		15	25	mV
R_{EGIN}	Input regulation	I_{REF} = –1 mA,	V_{CC} = 2.5 V to 7 V		2	5	mV
R_{EGL}	Output regulation	I_{REF} = –0.1 mA to –1 mA			1	5	mV
I_{OS}	Short-circuit output current	V_{REF} = 0		–2	–10	–30	mA

NOTES: 1. Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.
2. The deviation parameter $V_{REF(dev)}$ is defined as the difference between the maximum and minimum values obtained over the recommended free-air temperature range (–20°C to 85°C).

undervoltage lockout section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH}	Upper threshold voltage	T_A = 25°C	2.2	2.3	2.4	V
V_{TL}	Lower threshold voltage	T_A = 25°C	2	2.1	2.2	V
V_{hys}	Hysteresis ($V_{TH} – V_{TL}$)	T_A = 25°C	0.1	0.2	0.3	V

NOTE 1: Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.

protection control section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SCP}	Input terminal source current		–1.4	–2	–2.6	µA
V_{T2}	Input threshold voltage	CH-1, 3	1.10	1.15	1.20	V
V_{T3}		CH-2	0.20	0.25	0.30	
V_R	Latch reset threshold voltage	T_A = 25°C	0.8	1.5		V
V_{T5}	Threshold voltage		1.20	1.25	1.30	V

NOTE 1: Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.

oscillator section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{OSC}	Frequency	C_T = 130 pF,	R_T = 7 kΩ	400	500	600	kHz
f_{dV}	Frequency change with V_{CC}	V_{CC} = 2.5 V, C_T = 130 pF,	T_A = 25°C, R_T = 7 kΩ		1%	2%	
f_{dT}	Frequency change with T_A	C_T = 130 pF,	R_T = 7 kΩ		5%	10%	
$I_{CT/RT}$	Output source current			–180	–200	–220	µA
V_{OSCH}	H level output voltage			0.95	1	1.05	V
V_{OSCL}	L level output voltage			0.35	0.40	0.45	V

NOTE 1: Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.

dead time control section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{BDT1/3}$	Input bias current	$V_{DTC1/3}$ = 0.35 V to 1.05 V				200	nA
I_{BDT2}		V_{DTC2} = 0.35 V to 1.05 V			±2	±20	
V_{T1}	Comparator threshold voltage			0.2	0.25	0.3	V
$V_{T0(DTC1/3)}$	Input threshold voltage (DTC1/3) (see Note 3)	Duty = 0%	f_{OSC} = 500 kHz	0.3	0.4	0.5	V
$V_{T100(DTC1/3)}$		Duty = 100%		0.9	1	1.1	
$V_{T0(DTC2)}$	Input threshold voltage (DTC2) (see NOte 3)	Duty = 0%	f_{OSC} = 500 kHz	0.3	0.4	0.5	V
$V_{T100(DTC2)}$		Duty = 100%		0.9	1	1.1	

NOTES: 1: Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.
3. These specifications are not production tested. They are specified as ensured values on circuit design.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V (unless otherwise noted) (see Note 1) (continued)

error amplifier section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	CH1, 3,	A_V = 1			15	mV
I_{IB}	Input bias current	CH1, 3,	V_I = –.95 V to 1.55 V		±10	±20	nA
		CH2,	V_I = 0.4 V to 1 V		±10	±20	
V_{IR}	Input voltage range	CH1, 3,		0.95		1.55	V
		CH2		0.4		1	
A_{VD}	Open-loop voltage amplification	R_{FB} = 200 kΩ			60		dB
B_1	Unity-gain bandwidth				1		MHz
V_{OM+}	Output voltage swing	V_{ID} = 0.1 V	I_O = 60 µA	1.2			V
$V_{OM–}$			I_O = 0.2 mA			0.2	
I_{OM+}	Output sink current	V_{ID} = 0.1 V,	V_O = 0.2 V	0.2	1		mA
$I_{OM–}$	Output source current	V_{ID} = 0.1 V,	V_O = 1.2 V	–60	–100		µA
V_{T4}	Input bias voltage	CH2,	A_V = 1, T_A = 25°C	678	700	722	mV
		CH2,	A_V = 1	665	700	735	

NOTE 1: Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.

output section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_O = 20 mA (CH2)	2.9	3.05		V
		I_O = –40 mA (CH1, 3)	1.9	2.2	2.6	
V_{OL}	Low-level output voltage	I_O = 20 mA (CH1, 3)		0.2	0.4	V
		I_O = 40 mA (CH2)	0.2	0.3	0.6	
t_r	Rise time	CL = 1000 pF		130		ns
t_f	Fall time	I_O = 1000 pF		50		ns

NOTE 1: Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	Output OFF state		2.5	4	mA
I_{CCA}	Average supply current	F_{OSC} = 500 kHz, Duty = 50%, No load		3.5	5	mA

NOTE 1: Typical values of all parameters except for $V_{REF(dev)}$ and f_{dT} are specified at T_A = 25°C.

TYPICAL CHARACTERISTICS

REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

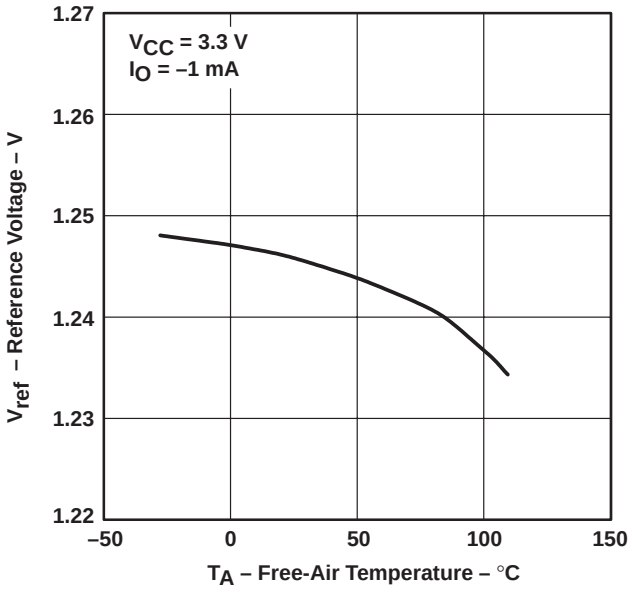


Figure 1

INPUT THRESHOLD VOLTAGE (UVLO) vs FREE-AIR TEMPERATURE

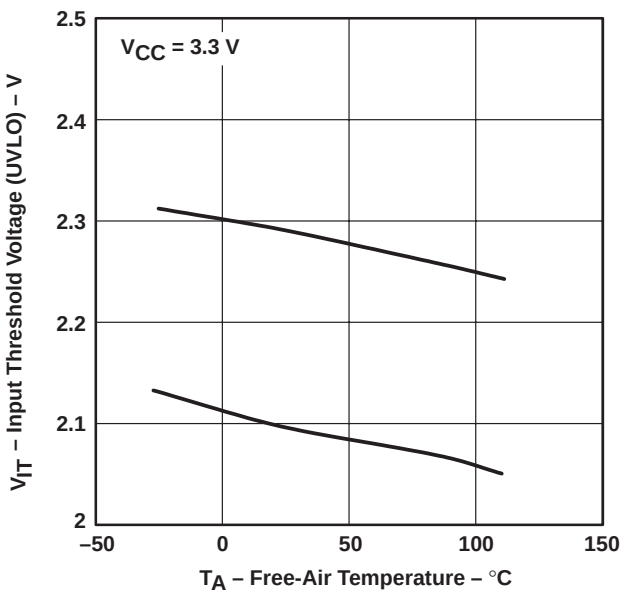


Figure 2

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

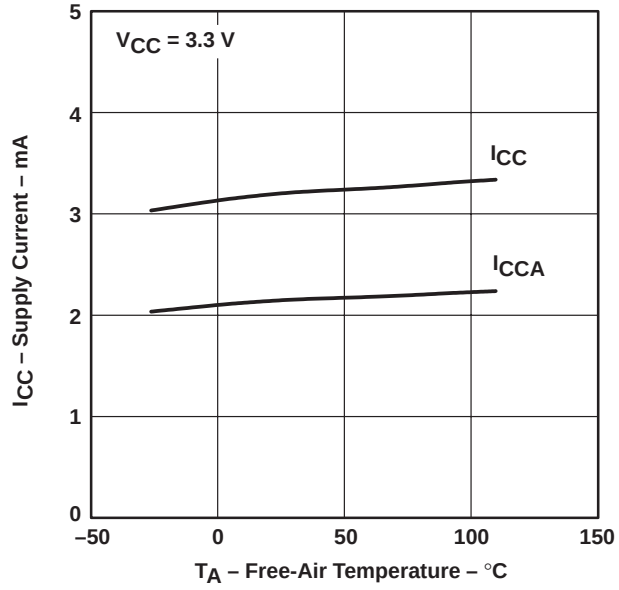


Figure 3

SOURCE CURRENT vs FREE-AIR TEMPERATURE

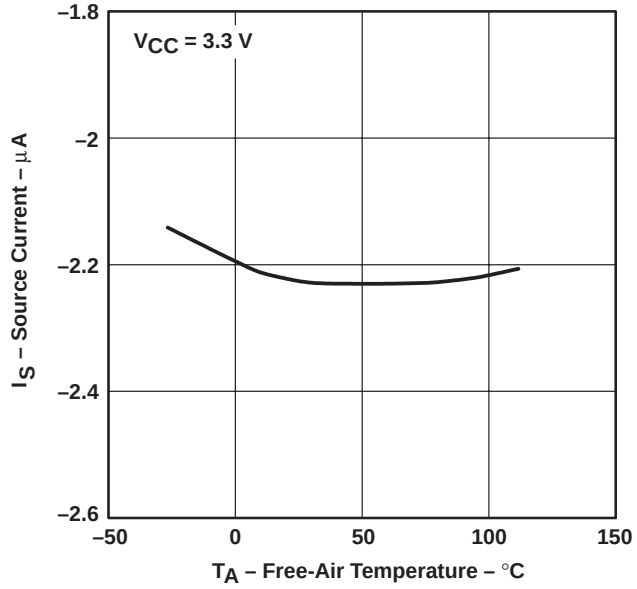


Figure 4

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs TIMING CAPACITOR

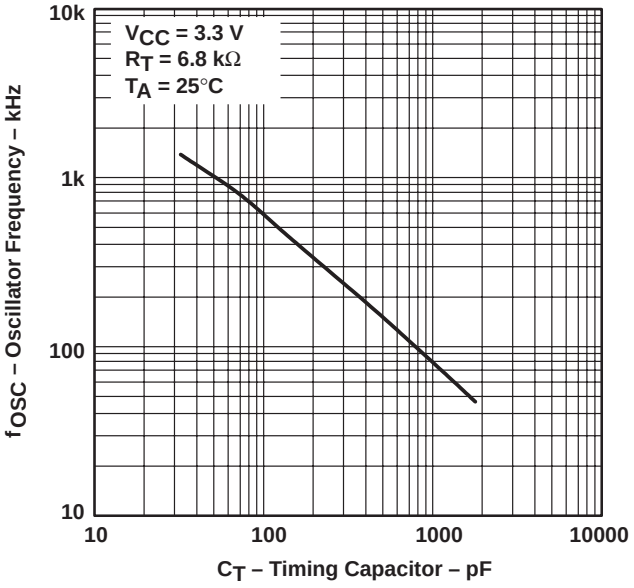


Figure 5

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

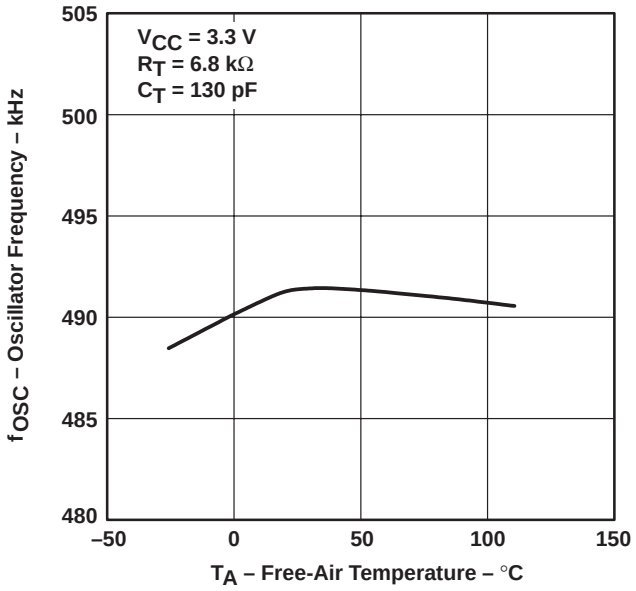


Figure 6

SOURCE CURRENT vs FREE-AIR TEMPERATURE

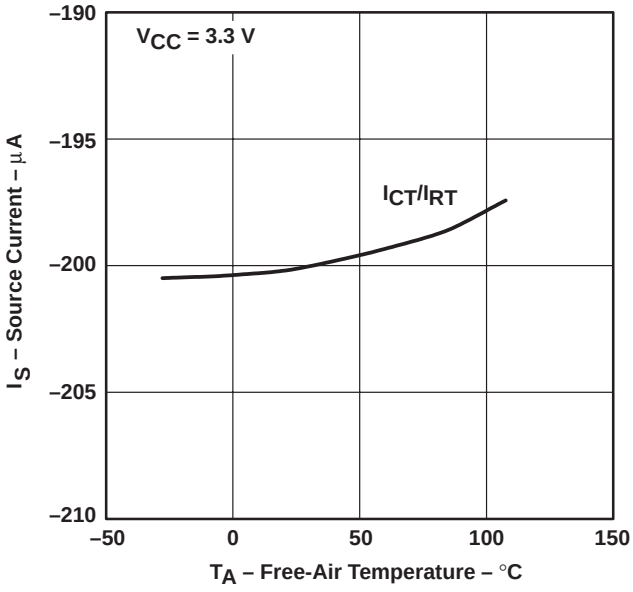


Figure 7

TYPICAL CHARACTERISTICS

INPUT THRESHOLD VOLTAGE (DTC)
vs
TIMING CAPACITOR

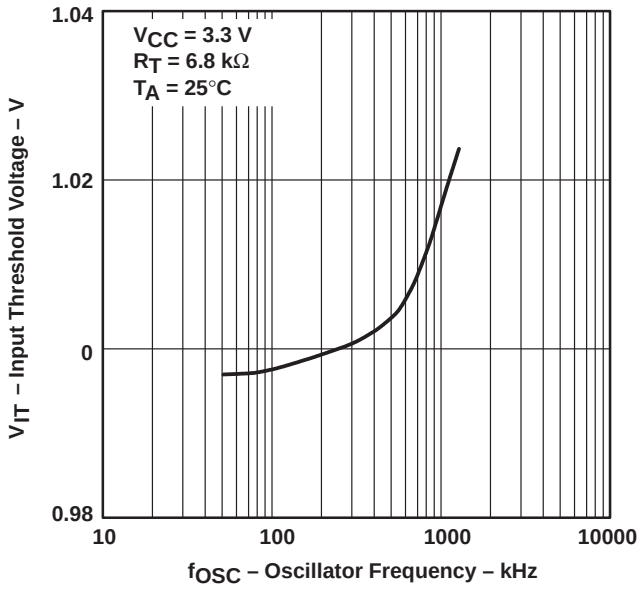


Figure 8

INPUT THRESHOLD VOLTAGE (DTC)
vs
TIMING CAPACITOR

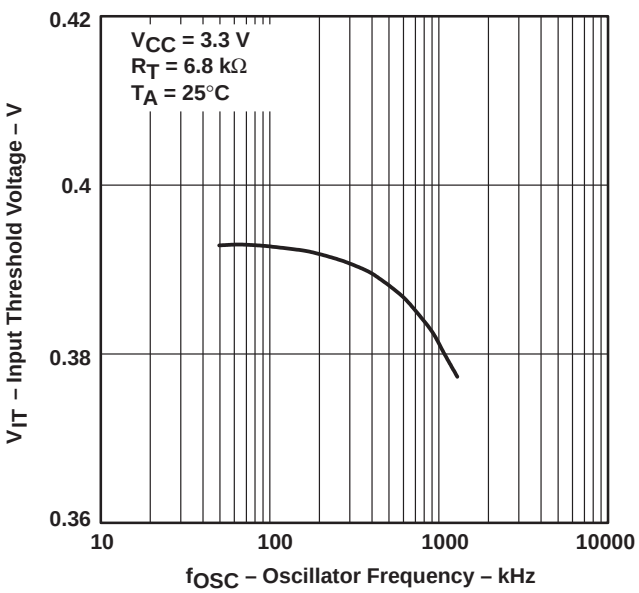


Figure 9

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

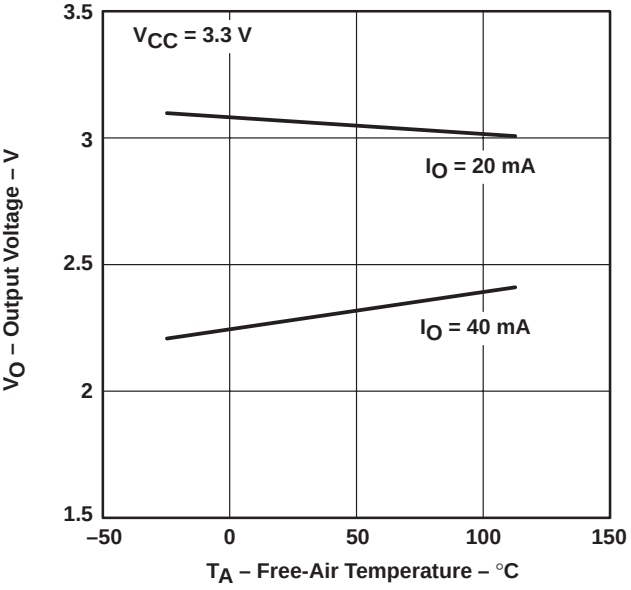


Figure 10

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

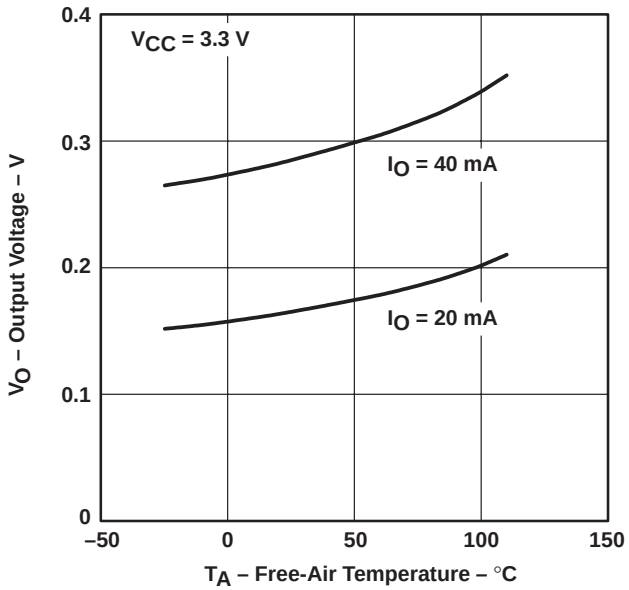


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT SOURCE CURRENT

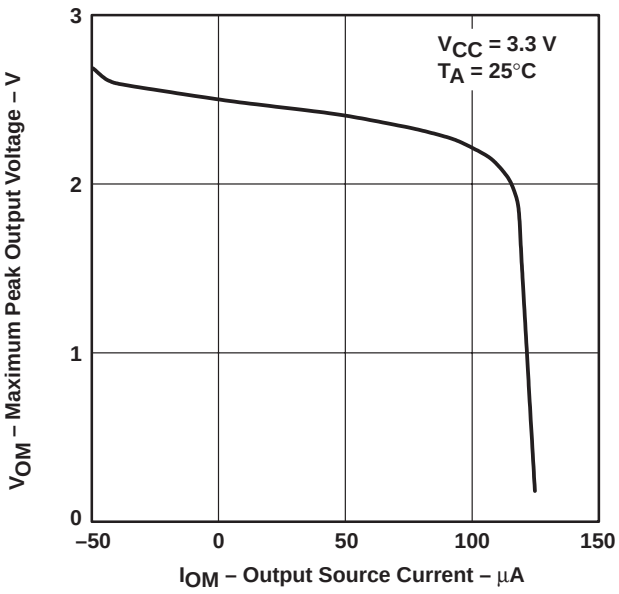


Figure 12

OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

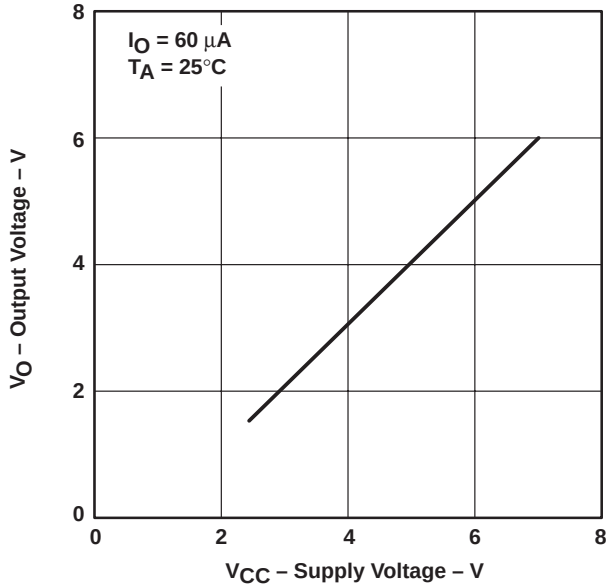


Figure 13

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

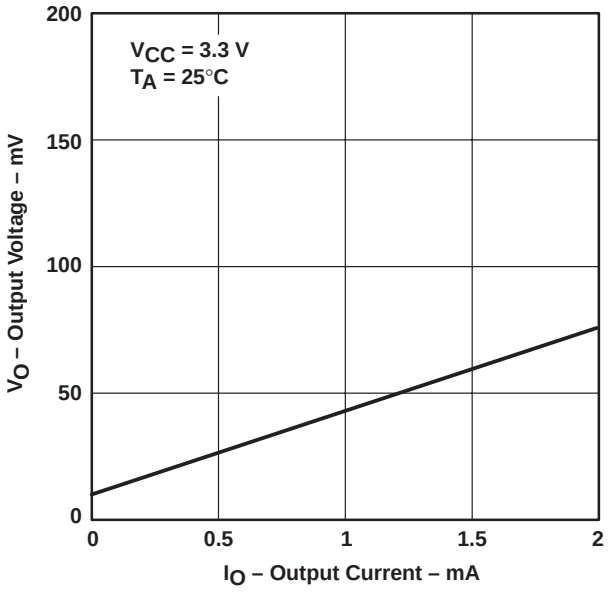


Figure 14

REFERENCE VOLTAGE
vs
SUPPLY VOLTAGE

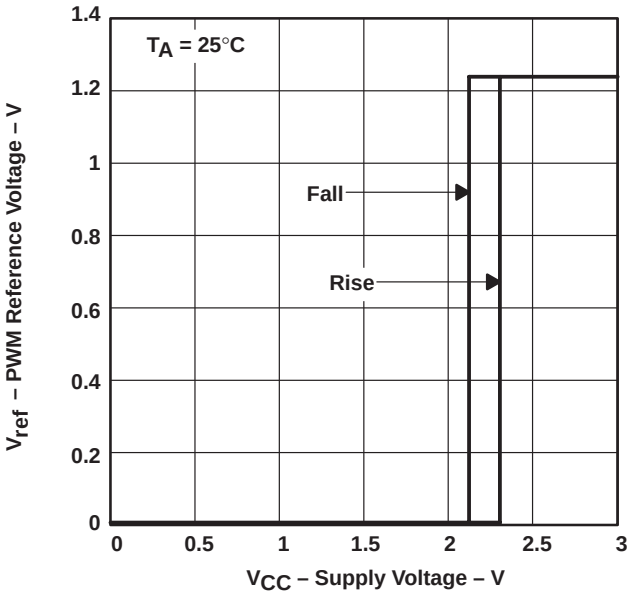


Figure 15

TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN
vs
FREQUENCY**

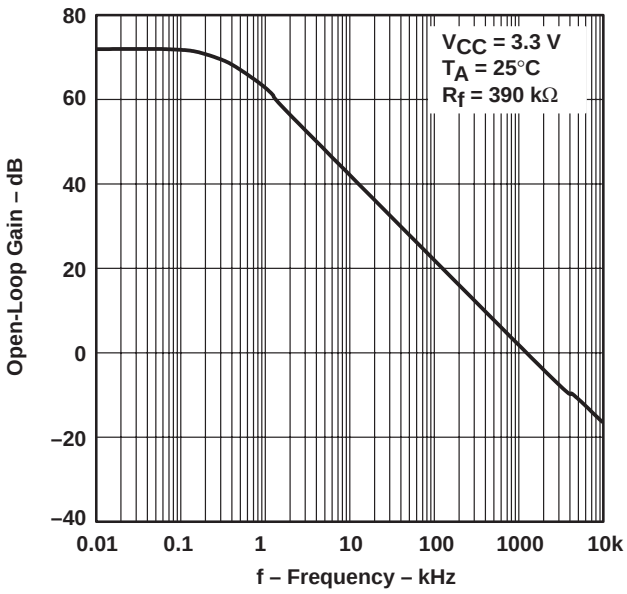


Figure 16

**PHASE SHIFT
vs
FREQUENCY**

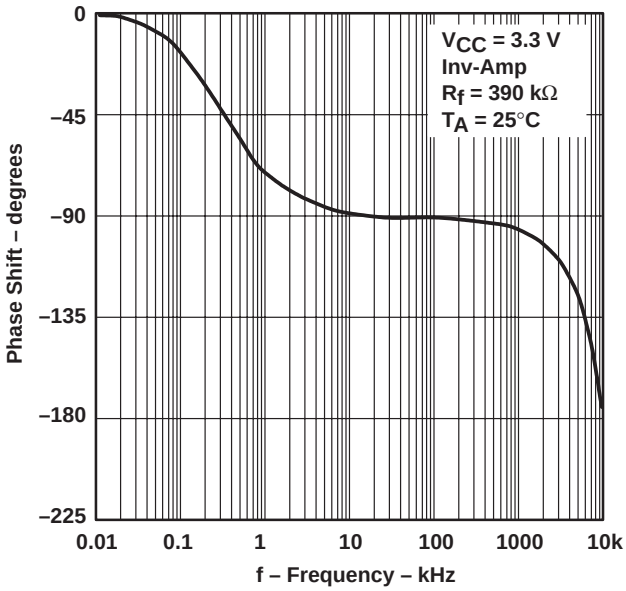


Figure 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5100IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PU5100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

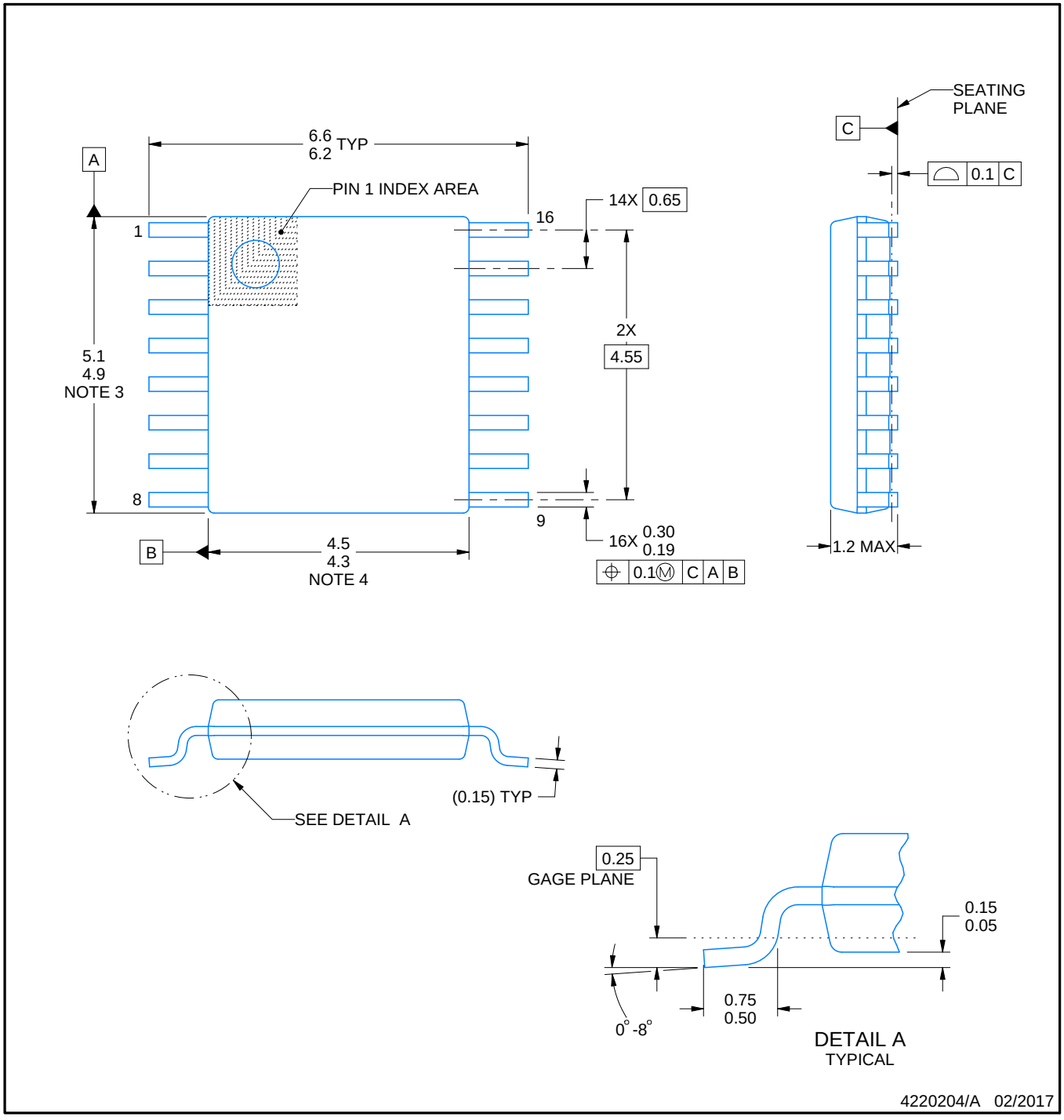
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PW0016A

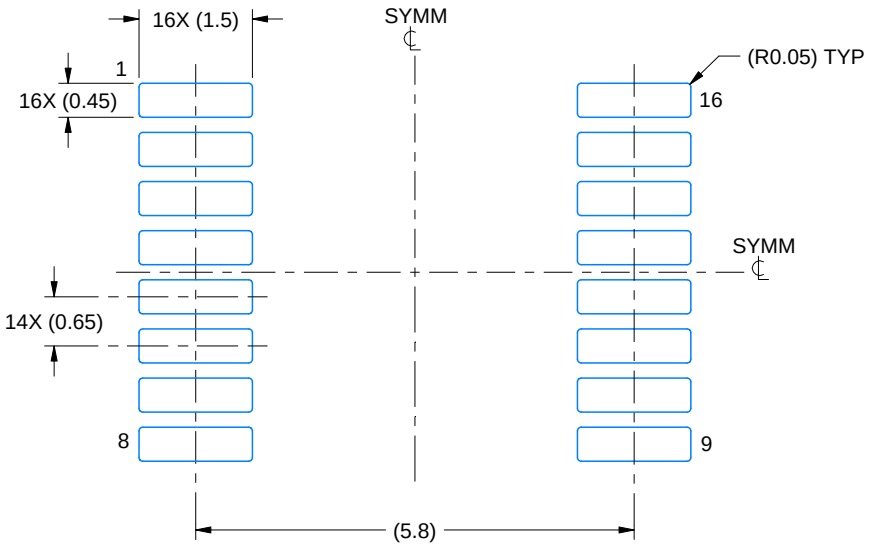
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

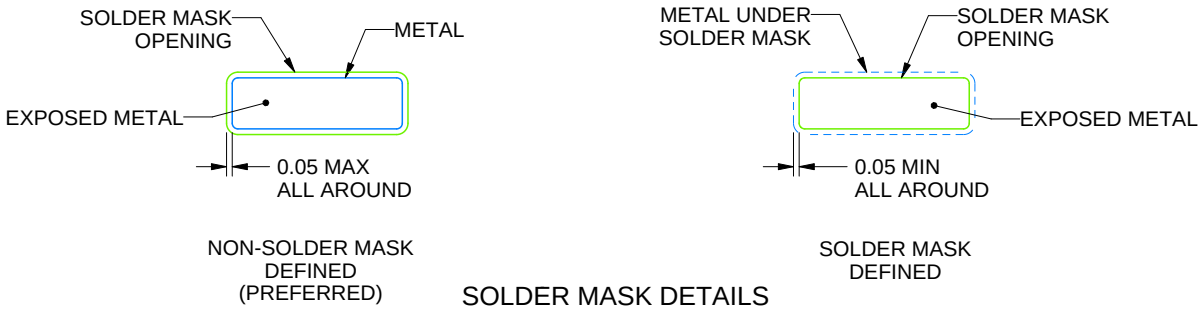


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

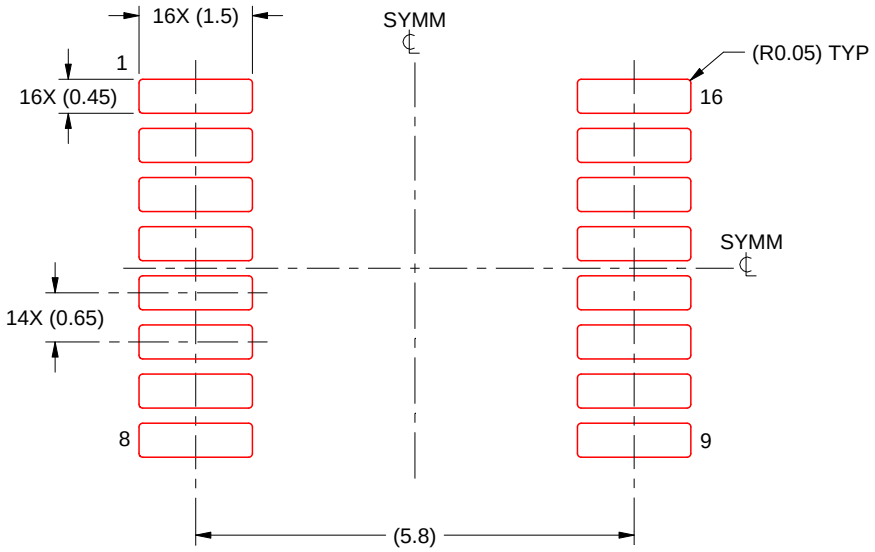


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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