25 MHz Direct Digital Synthesizer, Waveform Generator

Known Good Die

AD9832-KGD

FEATURES

25 MHz speed
On-chip SIN lookup table
On-chip, 10-bit DAC
Serial loading
Power-down option
Temperature range: −40°C to +85°C
200 mW power consumption
Known good die (KGD): these die are fully guaranteed to data sheet specifications

APPLICATIONS

Frequency stimulus/waveform generation
Frequency phase tuning and modulation
Low power RF/communications systems
Liquid and gas flow measurement
Sensory applications: proximity, motion, and defect detection
Test and medical equipment

GENERAL DESCRIPTION

The AD9832-KGD is a numerically controlled oscillator employing a phase accumulator, a sine look-up table, and a 10-bit digital-to-analog converter (DAC) integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation and frequency modulation.

Clock rates up to 25 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation is effected by loading registers through the serial interface.

A power-down bit lets the user power down the AD9832-KGD when it is not in use, the power consumption being reduced to 5 mW (5 V) or 3 mW (3 V).

Similar DDS products can be found at www.analog.com/DDS.

Additional application and technical information can be found in the AD9832 data sheet.

FUNCTIONAL BLOCK DIAGRAM

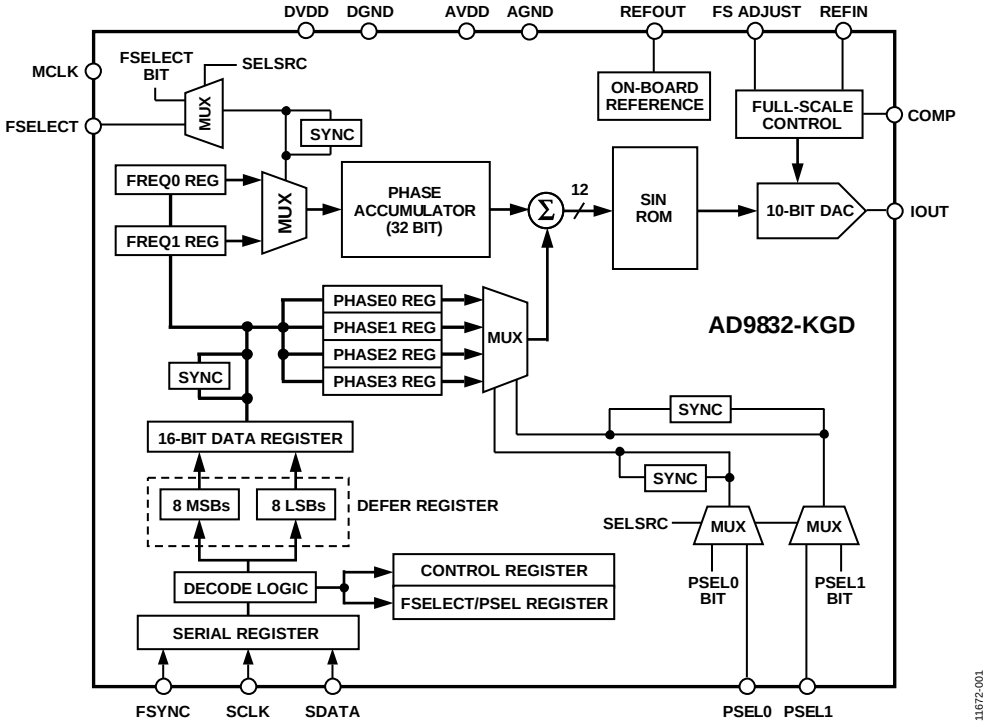

Figure 1.

Rev. A Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

7/13—Rev. 0 to Rev. A

Changes to Ordering Guide 8

6/13—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = +5 V ± 5%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}; REFIN = REFOUT; R_{SET} = 3.9 kΩ; R_{LOAD} = 300 Ω for IOUT, unless otherwise noted. Also, see Figure 2.

Table 1.

Parameter[1]	AD9832-KGD	Unit	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Update Rate (f_{MAX})	25	MSPS nom	
IOUT Full Scale	4	mA nom	
	4.5	mA max	
Output Compliance	1.35	V max	3 V power supply
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±0.5	LSB typ	
DDS SPECIFICATIONS[2]			
Dynamic Specifications			
Signal-to-Noise Ratio	50	dB min	f_{MCLK} = 25 MHz, f_{OUT} = 1 MHz
Total Harmonic Distortion	−53	dBc max	f_{MCLK} = 25 MHz, f_{OUT} = 1 MHz
Spurious-Free Dynamic Range (SFDR)[3]			f_{MCLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Narrow Band (±50 kHz)	−72	dBc min	5 V power supply
	−70	dBc min	3 V power supply
Wideband (±2 MHz)	−50	dBc min	
Clock Feedthrough	−60	dBc typ	
Wake-Up Time[4]	1	ms typ	
Power-Down Option	Yes		
VOLTAGE REFERENCE			
Internal Reference @ 25°C	1.21	V typ	
T_{MIN} to T_{MAX}	1.21 ± 7%	V min/V max	
REFIN Input Impedance	10	MΩ typ	
Reference Temperature Coefficient (TC)	100	ppm/°C typ	
REFOUT Output Impedance	300	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	V_{DD} − 0.9	V min	
Input Low Voltage, V_{INL}	0.9	V max	
Input Current, I_{INH}	10	μA max	
Input Capacitance, C_{IN}	10	pF max	
POWER SUPPLIES			
AVDD	2.97/5.5	V min/V max	
DVDD	2.97/5.5	V min/V max	
I_{AA}	5	mA max	5 V power supply
I_{DD}	2.5 + 0.4/MHz	mA typ	5 V power supply
I_{AA} + I_{DD}[5]	15	mA max	3 V power supply
	24	mA max	5 V power supply
Low Power Sleep Mode	350	μA max	

[1] Operating temperature range is −40°C to +85°C.
[2] 100% production tested.
[3] f_{MCLK} = 6.25 MHz, frequency word = 0x5671C71C, and f_{OUT} = 2.11 MHz.
[4] To reduce the wake-up time at low power supplies and low temperature, the use of an external reference is suggested.
[5] Measured with the digital inputs static and equal to 0 V or DVDD. The AD9832-KGD is tested with a capacitive load of 50 pF. The part can operate with higher capacitive loads, but the magnitude of the analog output will be attenuated. For example, a 5 MHz output signal is attenuated by 3 dB when the load capacitance equals 85 pF.

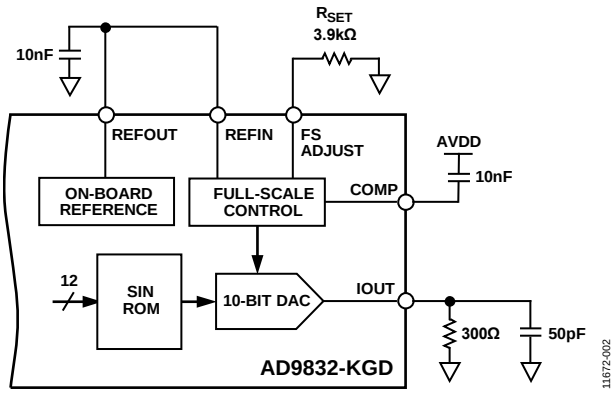

Figure 2. Test Circuit by Which Specifications Were Tested

TIMING CHARACTERISTICS

V_{DD} = +5 V ± 5%; AGND = DGND = 0 V, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	40	ns min	MCLK period
t_2	16	ns min	MCLK high duration
t_3	16	ns min	MCLK low duration
t_4	50	ns min	SCLK period
t_5	20	ns min	SCLK high duration
t_6	20	ns min	SCLK low duration
t_7	15	ns min	FSYNC to SCLK falling edge setup time
t_8	20	ns min	FSYNC to SCLK hold time
	SCLK − 5	ns max	
t_9	15	ns min	Data setup time
t_{10}	5	ns min	Data hold time
t_{11}	8	ns min	FSELECT, PSEL0, PSEL1 setup time before MCLK rising edge
t_{11A}[1]	8	ns min	FSELECT, PSEL0, PSEL1 setup time after MCLK rising edge

[1] See the Pad Configuration and Function Descriptions section.

Timing Diagrams

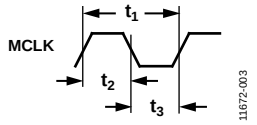

Figure 3. Master Clock

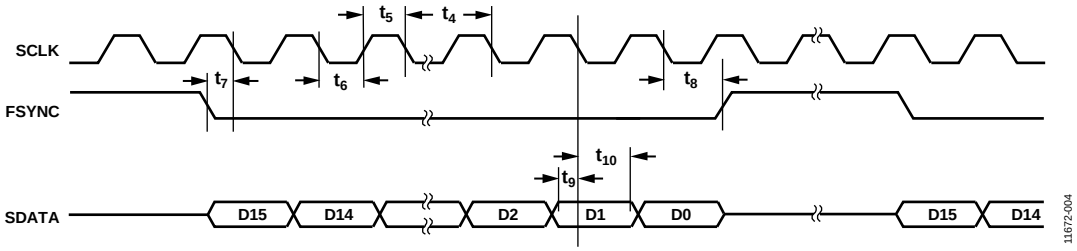

Figure 4. Serial Timing

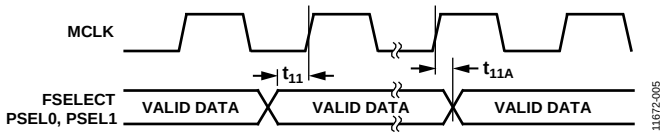

Figure 5. Control Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AGND	−0.3 V to +7 V
DVDD to DGND	−0.3 V to +7 V
AVDD to DVDD	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
Digital I/O Voltage to DGND	−0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to AVDD + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Rating	>4500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

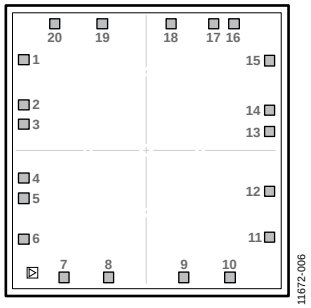

Figure 6. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	X-Axis(µm)	Y-Axis(µm)	Mnemonic	Pad Type	Description
1	−1130	+790.1	REFOUT	Single	Voltage Reference Output.
2	−1132.1	+402.9	DVDD	Single	Positive Power Supply for the Digital Section.
3	−1132.1	+232	DVDD	Single	Positive Power Supply for the Digital Section.
4	−1130	−240.4	DGND	Single	Digital Ground
5	−1130	−415	DGND	Single	Digital Ground
6	−1130	−767.9	MCLK	Single	Digital Clock Input
7	−763.2	−1105	SCLK	Single	Serial Clock, Logic Input
8	−351.7	−1105	SDATA	Single	Serial Data In, Logic Input
9	+343.9	−1105	FSYNC	Single	Data Synchronization Signal, Logic Input.
10	+771.8	−1105	FSELECT	Single	Frequency Select Input
11	+1130	−747.2	PSEL1	Single	Phase Select Input
12	+1130	−354	PSEL0	Single	Phase Select Input
13	+1130	+169	AGND	Single	Analog Ground
14	+1130	+346.9	AGND	Single	Analog Ground
15	+1130	+787.6	IOUT	Single	Current Output
16	+801	+1105	AVDD	Single	Positive Power Supply for the Analog Section
17	+618.2	+1105	AVDD	Single	Positive Power Supply for the Analog Section
18	+226.6	+1102.9	COMP	Single	Compensation Pin
19	−408.1	+1102.9	FS ADJUST	Single	Full-Scale Adjust Control.
20	−851.5	+1102.9	REFIN	Single	Voltage Reference Input.

OUTLINE DIMENSIONS

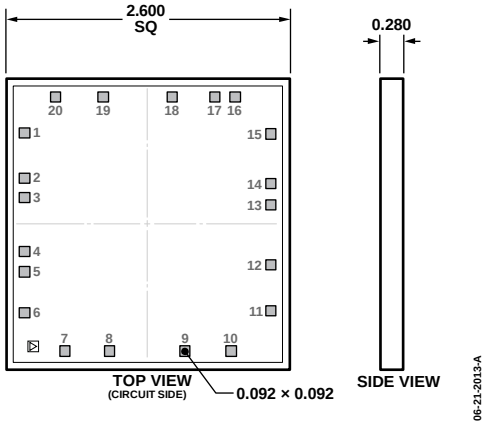

Figure 7. 20-Pad Bare Die [CHIP]
(C-20-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit[1]
Chip Size	2600 × 2600	µm
Scribe Line Width	100 × 150	µm
Die Size	2500 × 2450	mm (maximum)
Thickness	280	µm
Bond Pad	92 × 92	µm (minimum)
Bond Pad Composition	98.5% Al, 1% Si, 0.5% Cu	%
Backside	Bare	N/A
Passivation	Nitride	N/A

[1] N/A means not applicable.

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	No special requirements
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Pads 4 & 5 First

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9832-KGD-CHIPS	−40°C to +85°C	20-Pad Bare Die [CHIP]	C-20-1

D11672-0-7/13(A)

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