

MC100ELT23

5 V Dual Differential PECL to TTL Translator

Description

The MC100ELT23 is a dual differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The PECL inputs are differential; therefore, the MC100ELT23 can accept any standard differential PECL input referenced from a V_{CC} of 5.0 V.

Features

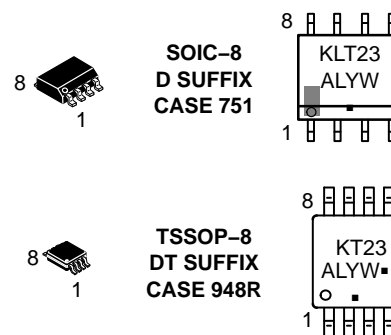
- 3.5 ns Typical Propagation Delay
- 24 mA TTL Outputs
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- Operating Range $V_{CC} = 4.75$ V to 5.25 V with $GND = 0$ V
- Internal Input 50 K Ω Pulldown Resistors
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC100ELT23

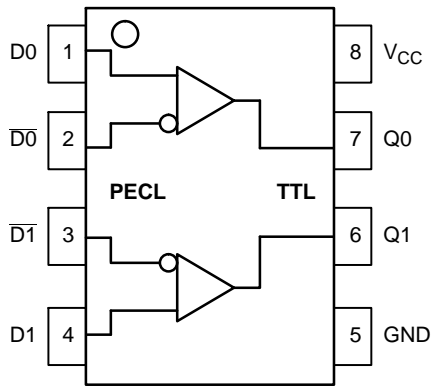


Table 1. PIN DESCRIPTION

| Pin | Function |
|-----------------|--------------------------|
| Qn | TTL Outputs |
| Dn, \bar{D}_n | PECL Differential Inputs |
| V _{CC} | Positive Supply |
| GND | Ground |

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 2. ATTRIBUTES

| Characteristics | Value |
|---|-----------------------------------|
| Internal Input Pulldown Resistor | 50 k Ω |
| Internal Input Pullup Resistor | N/A |
| ESD Protection | Human Body Model Machine Model |
| | > 2 kV > 400 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| | SOIC-8 TSSOP-8 |
| | Level 1 Level 3 |
| Flammability Rating | Oxygen Index: 28 to 34 |
| | UL 94 V-0 @ 0.125 in |
| Transistor Count | 91 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--------------------|----------------------------------|---------------|--------------|
| V _{CC} | Power Supply | GND = 0 V | | 7 | V |
| V _I | Input Voltage | GND = 0 V | V _I ≤ V _{CC} | 0 to 6 | V |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SOIC-8 SOIC-8 | 190 130 | °C/W °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-8 | 41 to 44 | °C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | TSSOP-8 TSSOP-8 | 185 140 | °C/W °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP-8 | 41 to 44 ± 5% | °C/W |
| T _{sol} | Wave Solder | Pb-Free | <2 to 3 sec @ 260°C | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MC100ELT23

Table 4. PECL INPUT DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $GND = 0.0\text{ V}$ (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-----|------|------|-----|------|------|-----|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{IH} | Input HIGH Voltage (Single-Ended) (Note 3) | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 4) | 2.2 | | 5.0 | 2.2 | | 5.0 | 2.2 | | 5.0 | V |
| I_{IH} | Input HIGH Current | | | 255 | | | 175 | | | 175 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- Input parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.25\text{ V}$.
- TTL output $R_L = 500\ \Omega$ to GND.
- V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}

Table 5. TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 4.75\text{ V}$ to 5.25 V ; $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Characteristic | Condition | Min | Typ | Max | Unit |
|-----------|------------------------------|---------------------------|------|-----|----------|------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -3.0\text{ mA}$ | 2.4 | | (Note 5) | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 24\text{ mA}$ | | | 0.5 | V |
| I_{CCH} | Power Supply Current | | | 23 | 33 | mA |
| I_{CCL} | Power Supply Current | | | 26 | 36 | mA |
| I_{OS} | Output Short Circuit Current | | -150 | | -60 | mA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- Max level is $V_{CC} - 0.7\text{ V}$ by design.

Table 6. AC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $GND = 0.0\text{ V}$ (Note 6 and Note 7)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------|--|-------|-----|------|------|------------|------|------|-----|------|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle Frequency | | | | | 100 | | | | | MHz |
| t_{JITTER} | Random Clock Jitter (RMS) | | | | | 35 | | | | | ps |
| t_{PLH} | Propagation Delay @ 1.5 V | 2.0 | | 5.5 | 2.0 | | 5.5 | 2.0 | | 5.5 | ns |
| t_{PHL} | Propagation Delay @ 1.5 V | 2.0 | | 5.5 | 2.0 | | 5.5 | 2.0 | | 5.5 | ns |
| V_{PP} | Input Swing (Note 8) | 200 | | 1000 | 200 | | 1000 | 200 | | 1000 | mV |
| t_r/t_f | Output Rise Time (10–90%) Output Fall Time (10–90%) | | | | | 1.6 1.1 | | | | | ns ns |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- V_{CC} can vary $\pm 0.25\text{ V}$.
- TTL output $R_L = 500\ \Omega$ to GND, and $C_L = 20\text{ pF}$ to GND. Refer to Figure 2.
- $V_{PP}(\text{min})$ is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .

MC100ELT23

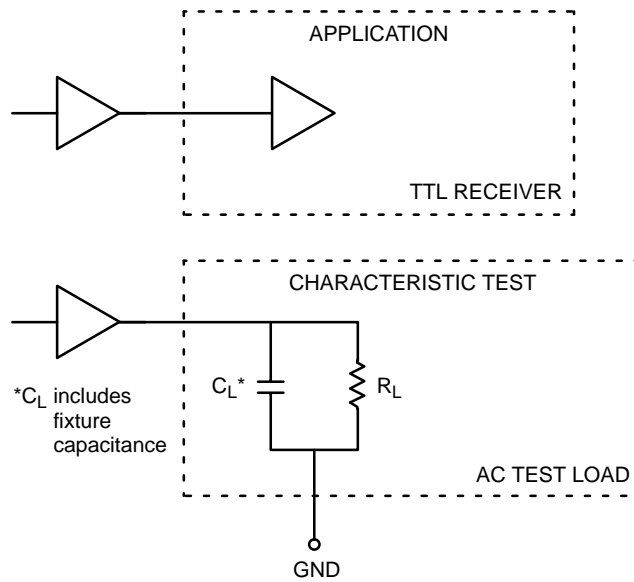


Figure 2. TTL Output Loading Used for Device Evaluation

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-----------------|----------------------|-----------------------|
| MC100ELT23DG | SOIC-8 (Pb-Free) | 98 Units / Rail |
| MC100ELT23DR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| MC100ELT23DTG | TSSOP-8 (Pb-Free) | 100 Units / Rail |
| MC100ELT23DTR2G | TSSOP-8 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

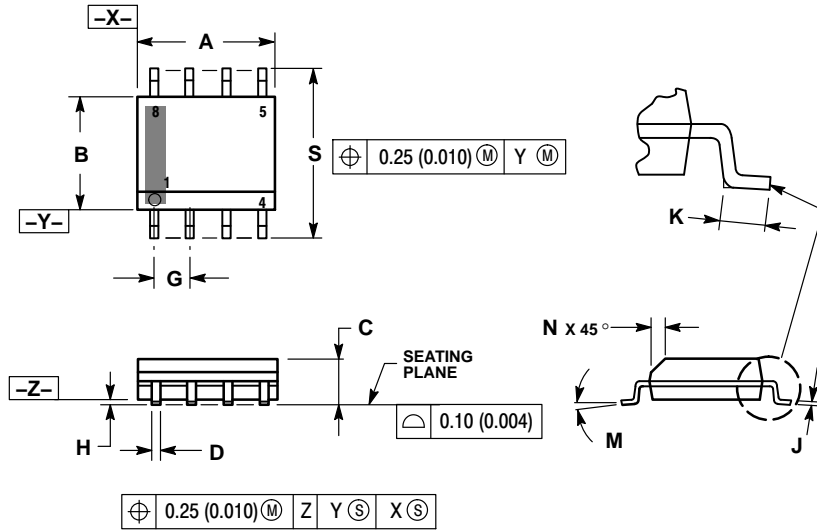
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC100ELT23

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

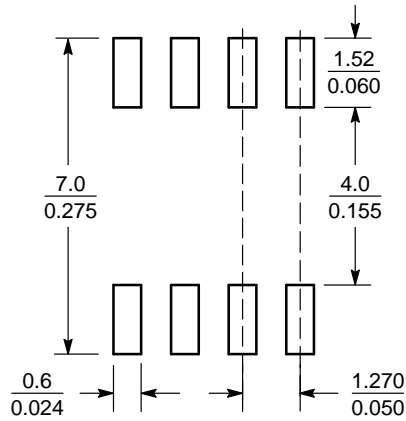


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



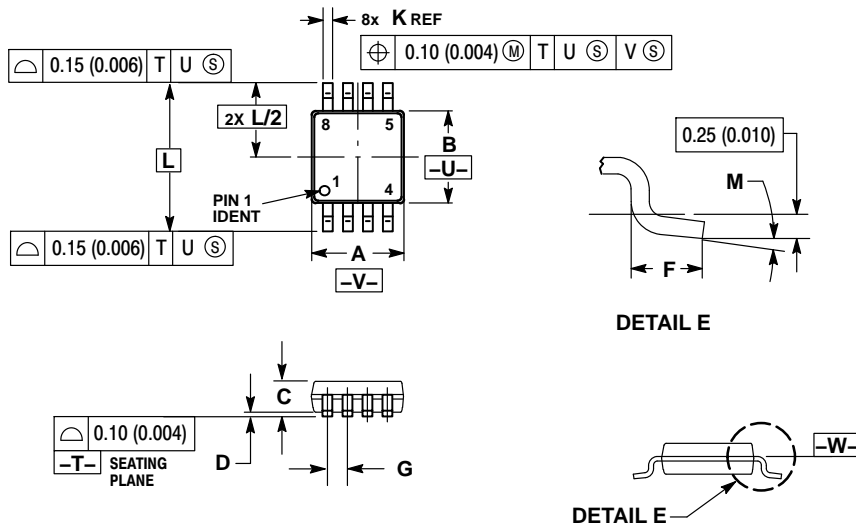
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC100ELT23

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
CASE 948R-02
ISSUE A




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

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