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FAIRCHILD SEMICONDUCTOR®

December 2010

NC7SZ00
TinyLogic® UHS Two-Input NAND Gate

Features

- Ultra-High Speed: t_{PD} 2.4ns (Typical) into 50pF at 5V V_{CC}
- High Output Drive: ±24mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Matches Performance of LCX Operated at 3.3V V_{CC}
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance inputs facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SOT23 and SC70 Packages

Description

The NC7SZ00 is a single two-input NAND gate from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V, independent of V_{CC} operating voltage.

Related Resources

- *MS-503 — Family Characteristics TinyLogic® HS/HST and UHS Series*

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ00M5X	7Z00	5-Lead SOT23, JEDEC MO-178 1.6mm	3000 Units on Tape & Reel
NC7SZ00P5X	Z00	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SZ00L6X	YY	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SZ00FHX	YY	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

Connection Diagrams

Figure 1. Logic Symbol

Pin Configurations

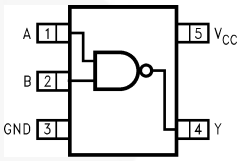


Figure 2. SC70 and SOT23 (Top View)

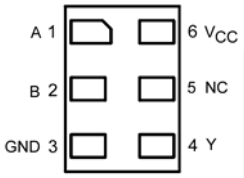


Figure 3. MicroPak™ (Top Through View)

Pin Definitions

Pin # SC70 / SOT23	Pin # MicroPak™	Name	Description
1	1	A	Input
2	2	B	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V_{CC}	Supply Voltage
	5	NC	No Connect

Function Table

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	6.0	V
V_{IN}	DC Input Voltage		-0.5	6.0	V
V_{OUT}	DC Output Voltage		-0.5	6.0	V
I_{IK}	DC Input Diode Current	V_{IN} < -0.5V		-50	mA
		V_{IN} > 6.0V		+20	
I_{OK}	DC Output Diode Current	V_{OUT} < -0.5V		-50	mA
		V_{OUT} > 6V, V_{CC}=GND		+20	
I_{OUT}	DC Output Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C	SOT-23		200	mW
		SC70-5		150	
		MicroPak™-6		130	
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8V, 2.5V ±0.2V	0	20	ns/V
		V_{CC} at 3.3V ± 0.3V	0	10	
		V_{CC} at 5.0V ± 0.5V	0	5	
θ_{JA}	Thermal Resistance	SOT-23		300	°C/W
		SC70-5		435	
		MicroPak™-6		500	
		MicroPak2™-6		560	

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95		$0.75V_{CC}$			$0.75V_{CC}$		V
		2.30 to 5.50		$0.70V_{CC}$			$0.70V_{CC}$		
V_{IL}	LOW Level Input Voltage	1.65 to 1.95				$0.25V_{CC}$		$0.25V_{CC}$	V
		2.30 to 5.50				$0.30V_{CC}$		$0.30V_{CC}$	
V_{OH}	HIGH Level Output Voltage	1.65	$V_{IN}=V_{IL}$ I_{OH}=-100µA	1.55	1.65		1.55		V
		1.80		1.70	1.80		1.70		
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I_{OH}=-4mA	1.29	1.52		1.29		
		1.80	I_{OH}=-8mA	1.90	2.15		1.90		
		2.30	I_{OH}=-16mA	2.40	2.80		2.40		
		3.00	I_{OH}=-24mA	2.30	2.68		2.30		
		4.50	I_{OH}=-32mA	3.80	4.20		3.80		
V_{OL}	LOW Level Output Voltage	1.65	$V_{IN}=V_{IH}$ I_{OL}=100µA		0.00	0.10		0.08	V
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I_{OL}=4mA		0.80	0.24		0.24	
		2.30	I_{OL}=8mA		0.10	0.30		0.30	
		3.00	I_{OL}=16mA		0.15	0.40		0.40	
		3.00	I_{OL}=24mA		0.22	0.55		0.55	
		4.50	I_{OL}=32mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0 to 5.5	V_{IN}=5.5V, GND			±1		±10	µA
I_{OFF}	Power Off	0	V_{IN} or V_{OUT}=5.5V			1		10	µA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN}=5.5V, GND			2		20	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay	1.65	C_L=15pF, R_L=1MΩ	2.0	5.4	11.4	2.0	12.0	ns	Figure 4 Figure 5
		1.80		2.0	4.5	9.5	2.0	10.0		
		2.50 ± 0.20		0.8	3.0	6.5	0.8	7.0		
		3.30 ± 0.30		0.5	2.4	4.5	0.5	4.7		
		5.00 ± 0.50		0.5	2.0	3.9	0.5	4.1		
		3.30 ± 0.30	C_L=50pF, R_L=500Ω	1.5	2.9	5.0	1.5	5.2		
		5.00 ± 0.50		0.8	2.4	4.3	0.8	4.5		
C_{IN}	Input Capacitance	0.00			4				pF	
C_{PD}	Power Dissipation Capacitance(2)	3.30			24				pF	Figure 6
		5.00			30					

Note:

2. C_{PD} is defined as the value of the internal equivalent capacitance derived from dynamic operating current consumption (I_{CCD}) at no output lading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)$.

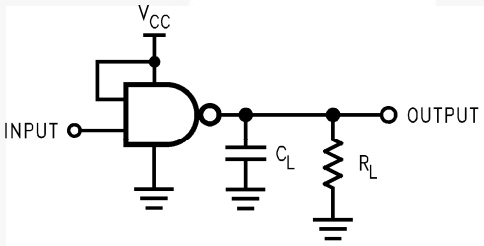


Figure 4. AC Test Circuit

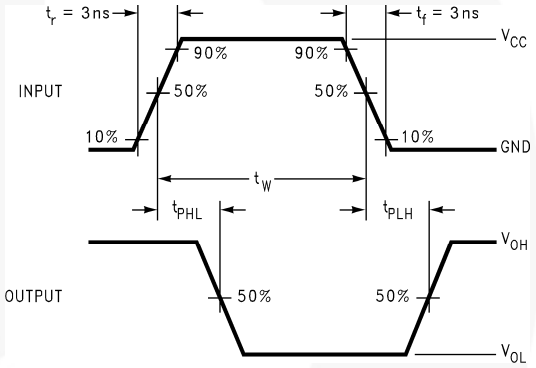
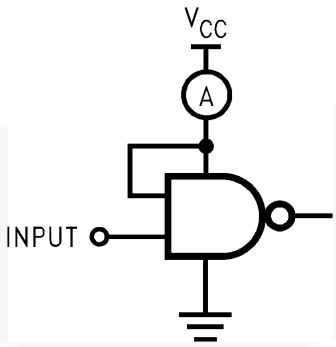


Figure 5. AC Waveforms



Note:

3. Input=AC Waveform; t_r=t_f=1.8ns; PRR=10MHz; Duty Cycle =50%.

Figure 6. I_{CCD} Test Circuit

Physical Dimensions

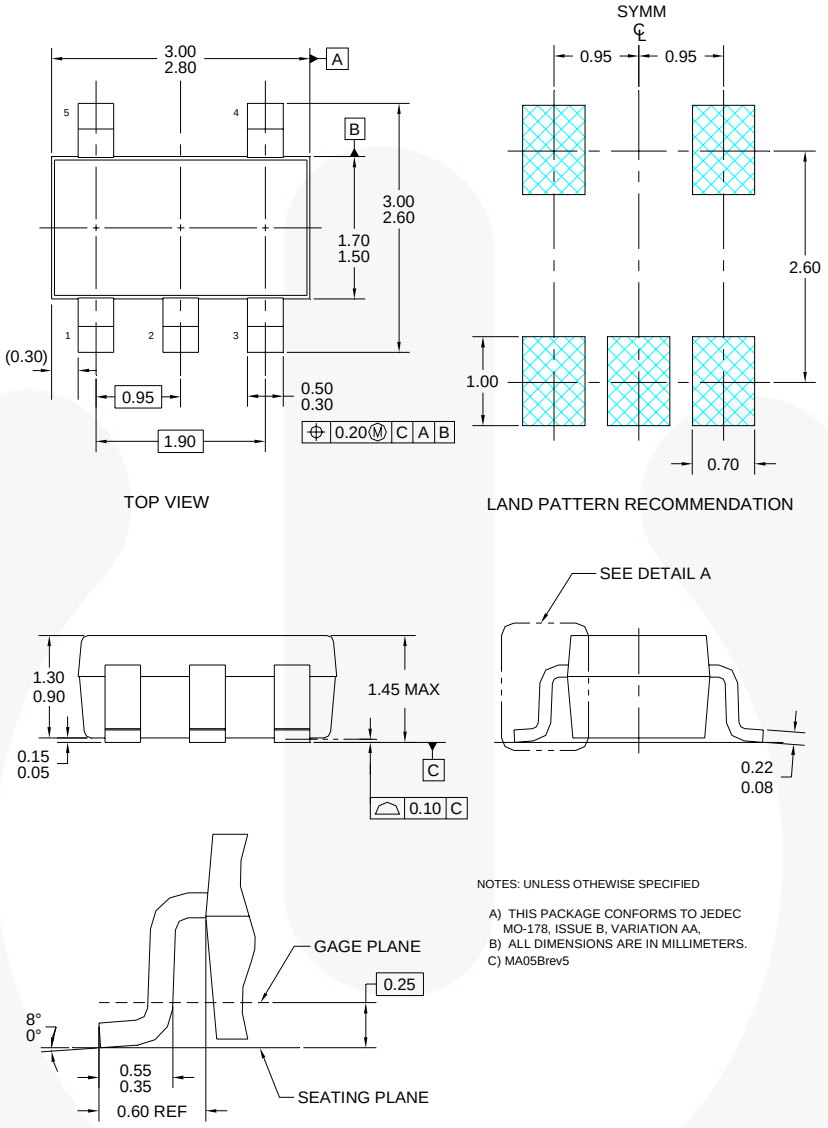


Figure 7. 5-Lead SOT23, JEDEC MO-178 1.6mm

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/SOT23-5L_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
M5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

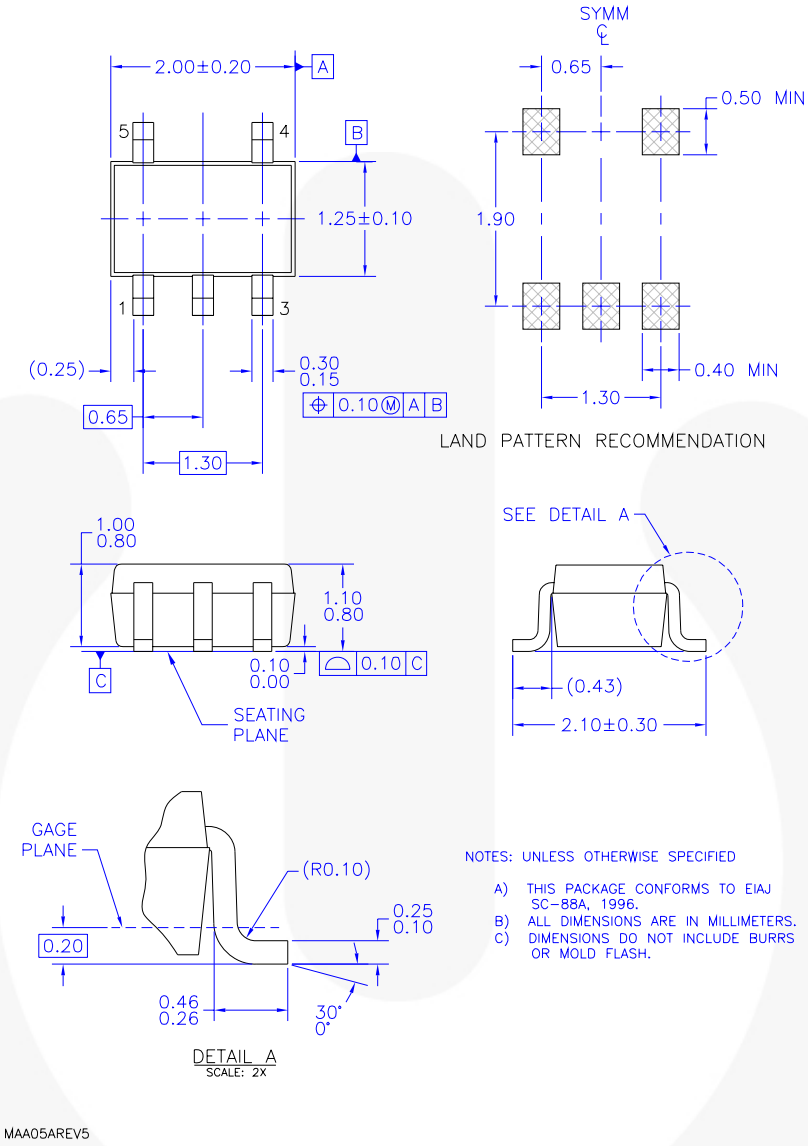

Figure 8. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

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Tape and Reel Specifications

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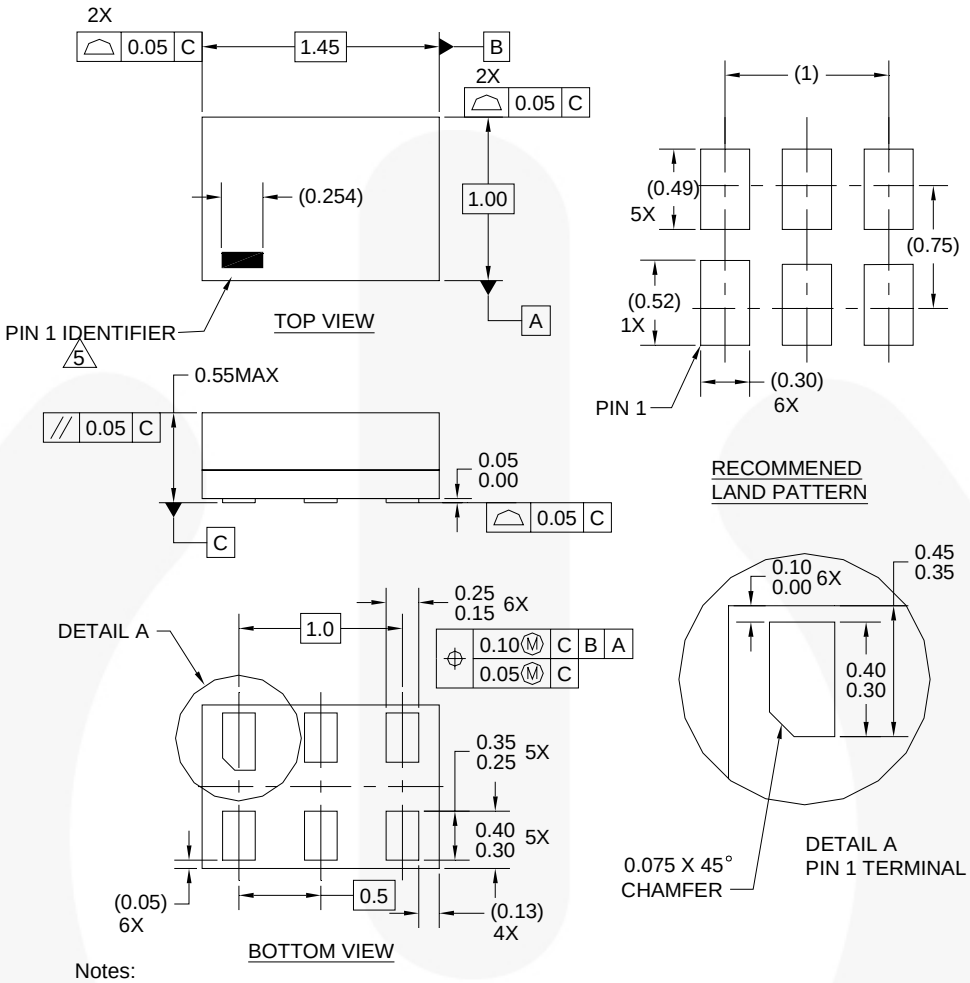
http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 9. 6-Lead, MicroPak™, 1.0mm Wide

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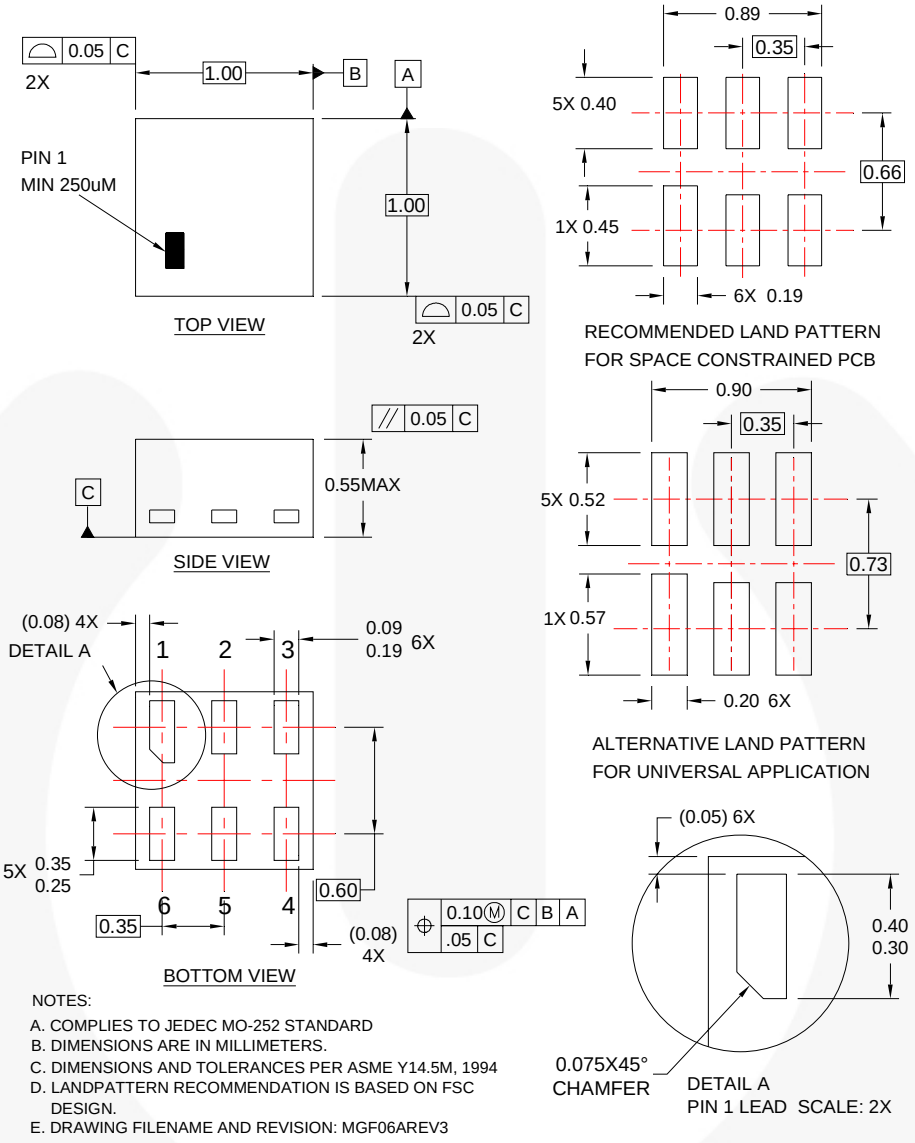
Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN.
E. DRAWING FILENAME AND REVISION: MGF06AREV3

Figure 10. 6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I52

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