XC61H Series

ETR0212-003a

Voltage Detector with Delay Circuit Built-In

■GENERAL DESCRIPTION

The XC61H series is a highly accurate, low power consumption CMOS voltage detector with a delay circuit. Detect voltage is accurate with minimal temperature drift. Output configurations are available in both CMOS and N-channel open drain.
Since the full delay circuit is built-in, an external delay-time capacitor is not necessary so that high density mounting is possible.

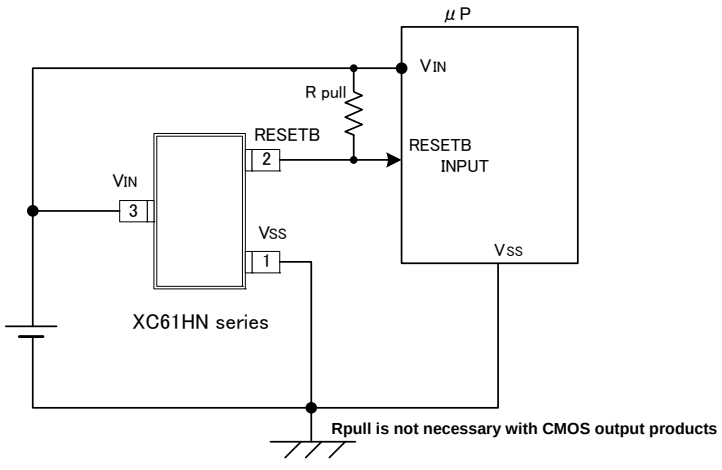
■APPLICATIONS

- ●Microprocessor reset circuitry
- ●System battery life and charge voltage monitors
- ●Memory battery back-up circuits
- ●Power-on reset circuits
- ●Power failure detection
- ●Delay circuitry

■FEATURES

Detect Voltage Accuracy : ± 2%
Low Power Consumption : 1.0μA(TYP.)[V_{IN}=2.0V]
Detect Voltage Range : 1.6V ~ 6.0V (0.1V increments)
Operating Voltage Range : 0.7V ~ 10.0V
Detect Voltage Temperature Characteristics
: ±100ppm/℃(TYP.)
Built-In Release Delay time: 1ms (MIN.)
50ms (MIN.)
80ms (MIN.)
Output Configuration : N-ch open drain or CMOS
Package : SOT-23
Environmentally Friendly : EU RoHS Compliant, Pb Free

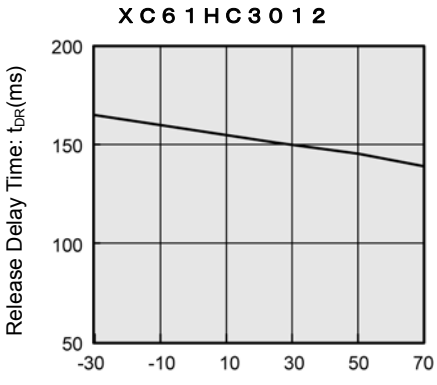
■TYPICAL APPLICATION CIRCUITS



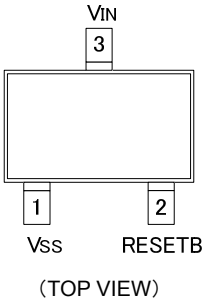
Rpull is not necessary with CMOS output products

■TYPICAL PERFORMANCE CHARACTERISTICS

●**Release Delay Time (t_{DR}) vs. Ambient Temperature**



■PIN CONFIGURATION



(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER SOT-23	PIN NAME	FUNCTION
1	V_{SS}	Ground
2	RESETB	Output
3	V_{IN}	Supply Voltage Input

■PRODUCT CLASSIFICATION

●Ordering Information

XC61H ①②③④⑤⑥⑦-⑧(*1)

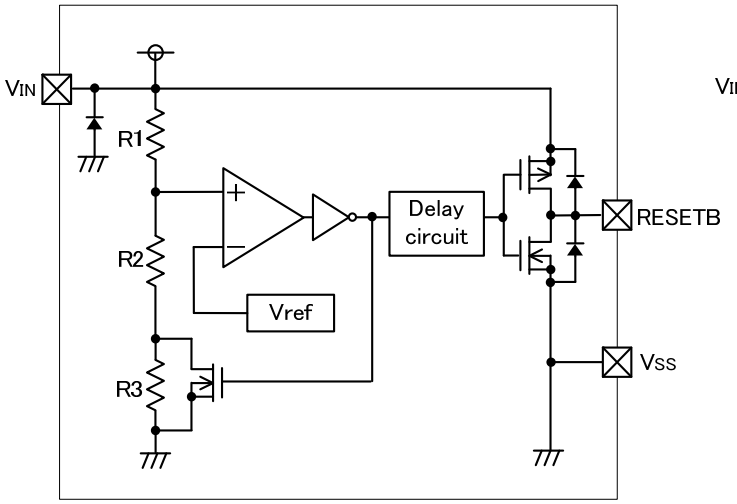
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
②③	Detect Voltage (V_{DF})	16 ~ 60	e.g. 2.5V → ②2 , ③5
④	Release Delay Time	1	50ms ~ 200ms
		4	80ms ~ 400ms
		5	1ms ~ 50ms
⑤	Detect Accuracy	2	± 2.0%(*2)
⑥⑦-⑧(*1)	Package (Oder Unit)	MR-G	SOT-23 (3000/Reel)

(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.

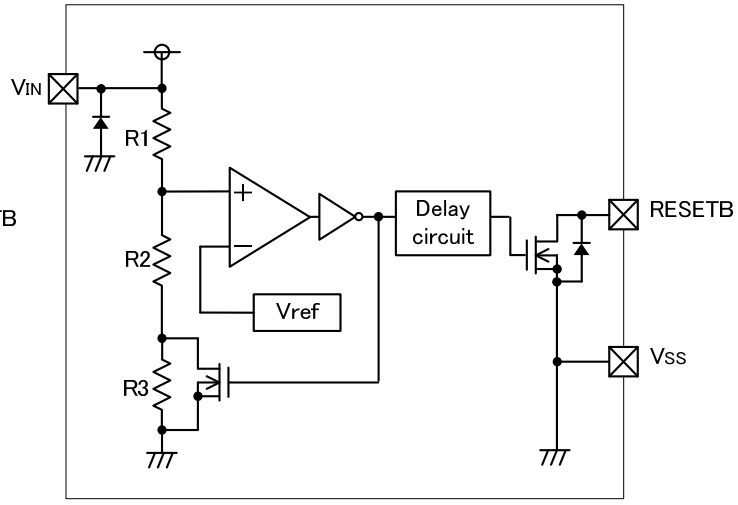
(*2) No parts are available with an accuracy of ± 1%

■BLOCK DIAGRAMS

(1)CMOS output



(2)N-ch open drain output



■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	12.0	V
Output Current		I_{OUT}	50	mA
Output Voltage	CMOS	RESTB	V_{SS}-0.3 ~V_{IN}+0.3	V
	N-ch open drain		V_{SS} -0.3 ~ 12	
Power Dissipation	SOT-23	Pd	250	mW
Operating Temperature Range		Topr	-30～+80	℃
Storage Temperature Range		Tstg	-40～+125	℃

■ELECTRICAL CHARACTERISTICS

Ta = 25℃

PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage		V_{DF}			$V_{DF(T)}$ x 0.98	$V_{DF(T)}$	$V_{DF(T)}$ x 1.02	V	①
Hysteresis Width		V_{HYS}			V_{DF} x 0.02	V_{DF} x 0.05	V_{DF} x 0.08	V	①
Supply Current (*1)		I_{SS}		V_{IN} = 1.5V	-	0.9	2.6	μA	②
				V_{IN} = 2.0V	-	1.0	3.0		
				V_{IN} = 3.0V	-	1.3	3.4		
				V_{IN} = 4.0V	-	1.6	3.8		
				V_{IN} = 5.0V	-	2.0	4.2		
Operating Voltage		V_{IN}	V_{DF}=1.6V～6.0V		0.7	-	10.0	V	①
Output Current		I_{OUT}	N-ch, V_{DS} = 0.5V	V_{IN} = 1.0V	1.0	2.2	-	mA	③
				V_{IN} = 2.0V	3.0	7.7	-		
				V_{IN} = 3.0V	5.0	10.1	-		
				V_{IN} = 4.0V	6.0	11.5	-		
				V_{IN} = 5.0V	7.0	13.0	-		
			P-ch, V_{DS}=2.1V (CMOS Output)	V_{IN} = 8.0V		-10.0	-2.0		④
Leakage Current	CMOS Output	I_{LEAK}	V_{IN}=10.0V, V_{OUT}=10.0V		-	0.01	-	μA	③
	Nch Open Drain				-	0.01	0.1		
Detect Voltage Temperature Characteristics		$\frac{\Delta V_{DF}}{\Delta Topr \cdot V_{DF}}$			-	±100	-	ppm/℃	-
Release Delay Time (V_{DR} → RESEB inversion)		t_{DR}	V_{IN} changes from 0.6V to 10V		50	-	200	ms	⑤
					80	-	400		
					1	-	50		

V_{DF} (T) is nominal detect voltage value
Release Voltage: V_{DR} = V_{DF} + V_{HYS}

(*1) The supply current during power-start until output being stable (during release operation) is 2μA greater with comparison to the period after the completion of release operation because of the shoot-through current in delay current.

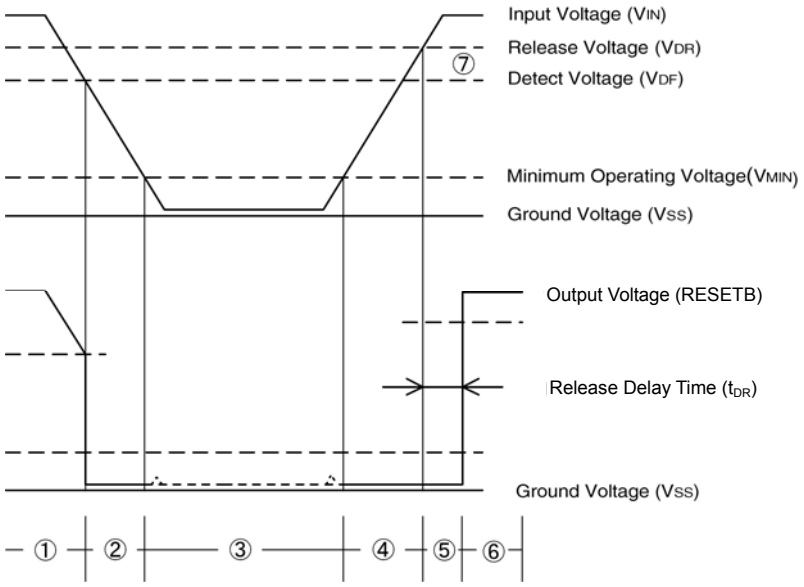
■OPERATIONAL EXPLANATION

●CMOS output

① An input voltage V_{IN} starts higher than the release voltage V_{DR}. Then, V_{IN} voltage will gradually fall. When V_{IN} voltage is higher than detect voltage V_{DF}, output voltage RESETB is equal to the V_{IN} voltage.
*Note that high impedance exists at RESETB with the N-channel open drain configuration. If the RESETB pin is pulled up, RESETB will be equal to the pull up voltage.
② When V_{IN} falls below V_{DF}, RESETB will be equal to ground voltage V_{SS} level (detect state).
* Note that this also applies to N-channel open drain configurations.
③ When VIN falls to a level below that of the minimum operating voltage V_{MIN}, output will become unstable.
*When the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.
④ When V_{IN} rises above the V_{SS} level (excepting levels lower than minimum operating voltage), RESETB will be equal to V_{SS} until V_{IN} reaches the V_{DR} level.
⑤ Although V_{IN} will rise to a level higher than V_{DR}, RESETB maintains ground voltage level via the delay circuit.
⑥ After taking a release delay time, V_{IN} voltage will be output at the RESETB pin.
*High impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

Notes:
1. The difference between V_{DR} and V_{DF} represents the hysteresis width.
2. Release delay time (t_{DR}) represents the time it takes until when V_{IN} voltage appears at RESETB pin once the input voltage has exceeded the V_{DR} level.

●Timing Chart



■NOTES ON USE

1. Please use this IC within the stated maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irregular oscillation may occur as a result of voltage drops at RIN if load current (IOUT) exists. It is therefore recommend that no resistor be added. (refer to Figure 1 below)
3. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of shoot-through current at the time of voltage release even if load current (IOUT) does not exist. (refer to Figure 1 below)
4. By connecting a resistor between the VIN pin and the input, detect and release voltages will rise as a result of the IC's supply current flowing through the VIN pin.
5. If a resistor (RIN) must be used, then please use with as small a level of input impedance as possible in order to control the occurrences of oscillation as described above.
   Further, please ensure that RIN is less than 10kΩ and that CIN is more than 0.1μF (Figure 1). In such cases, detect and release voltages will rise due to voltage drops at RIN brought about by the IC's supply current.
6. Depending on circuit's operation, release delay time of this IC can be widely changed due to upper limits or lower limits of operational ambient temperature.

●Irregular Oscillations

(1) Irregular oscillation as a result of output current with the CMOS output configuration:
When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow through RL. Because a voltage drop (RIN x IOUT) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin. When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.
Irregular oscillation may occur with this "release - detect - release" repetition.
Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Irregular oscillation as a result of shoot-through current:
Since the XC61H series are CMOS ICs, shoot-through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, irregular oscillation is liable to occur during release voltage operations as a result of output current which is influenced by this shoot-through current (Figure 3).
Since hysteresis exists during detect operations, irregular oscillation is unlikely to occur.

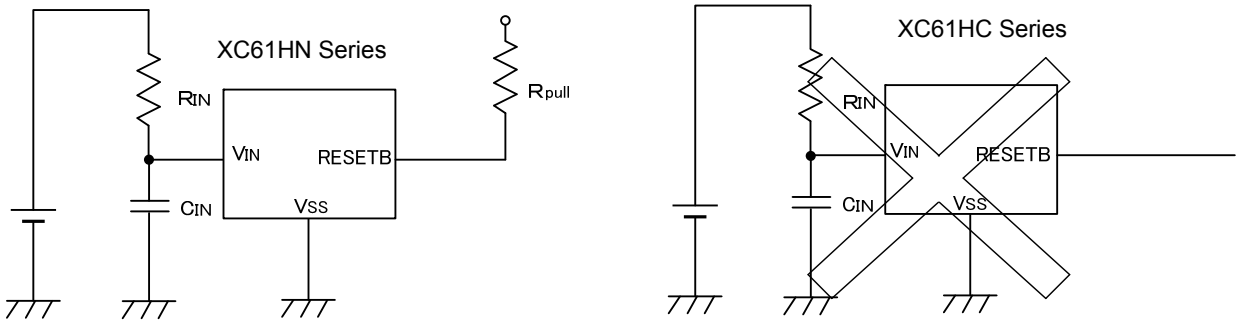


Figure 1 Use of input resistor R_{IN}

■NOTES ON USE

●Irregular Oscillations (Continued)

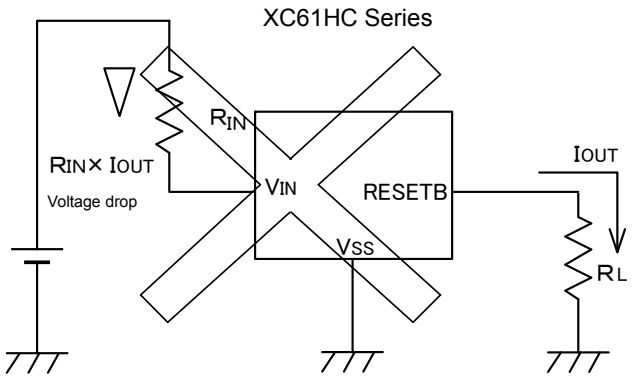


Figure 2 Irregular Oscillation by output current

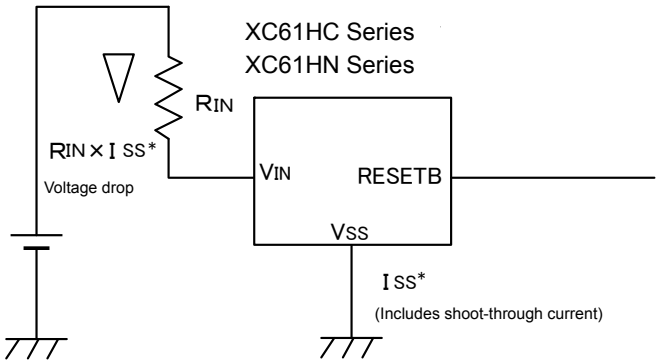
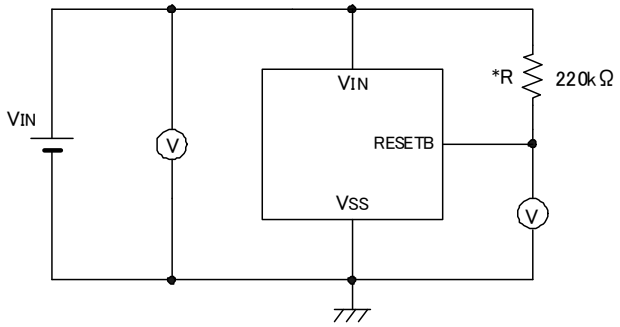


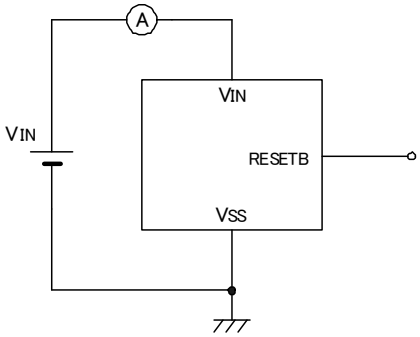
Figure 3 Irregular Oscillation by shoot-through current

■TEST CIRCUITS

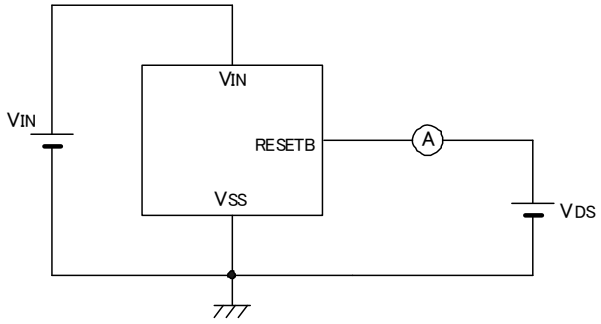
●Circuit ①



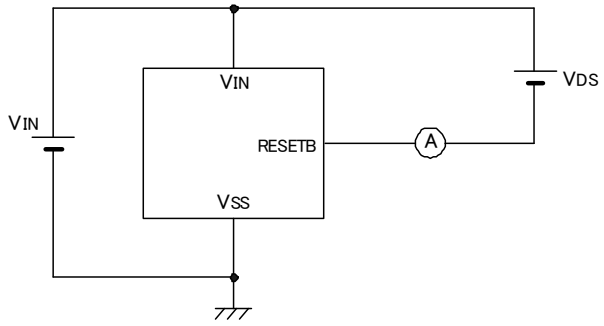
●Circuit ②



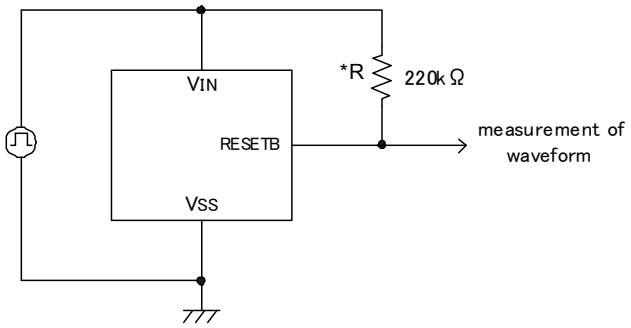
●Circuit ③



●Circuit ④



●Circuit ⑤

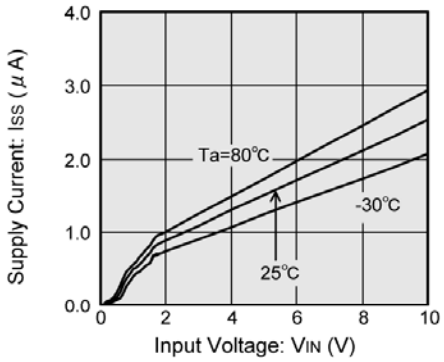


*R is not necessary with CMOS output products.

■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Supply Current vs. Input Voltage

XC61HN1612



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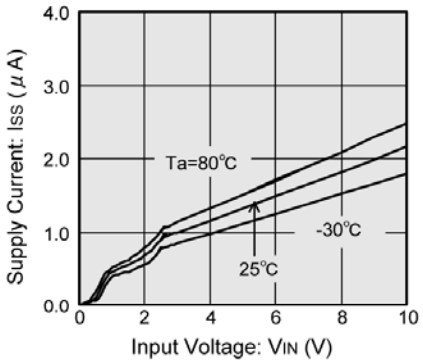

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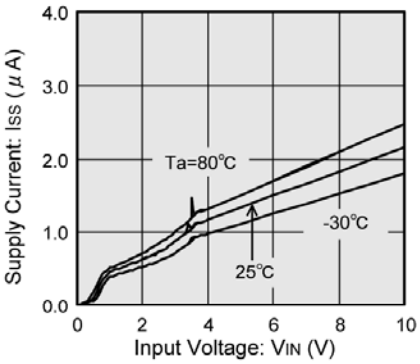
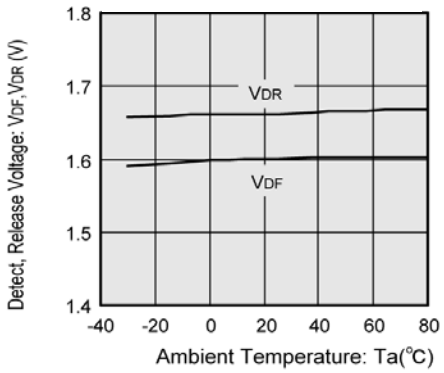


(2) Detect Voltage, Release Voltage vs. Ambient Temperature

XC61HN1612



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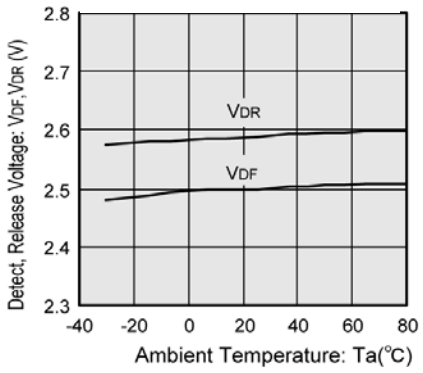

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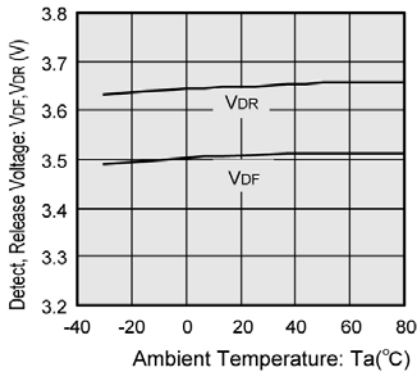
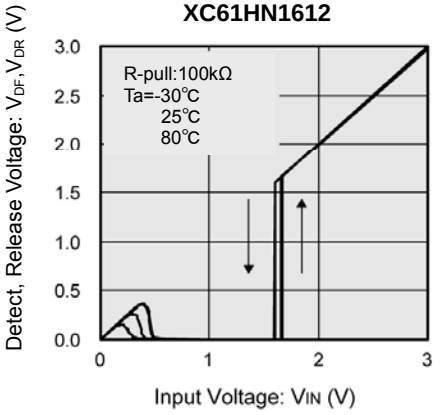


(3) Detect Voltage, Release Voltage vs. Input Voltage

XC61HN1612



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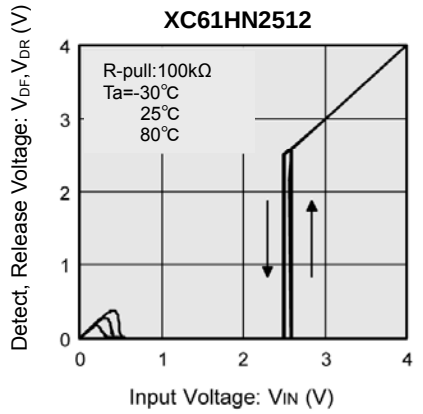

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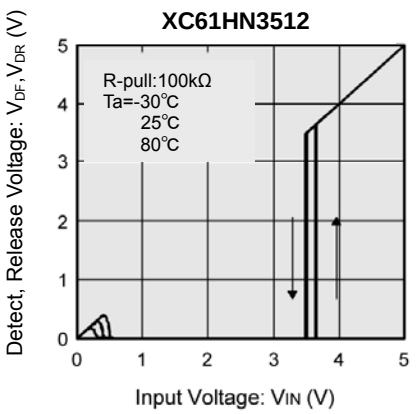
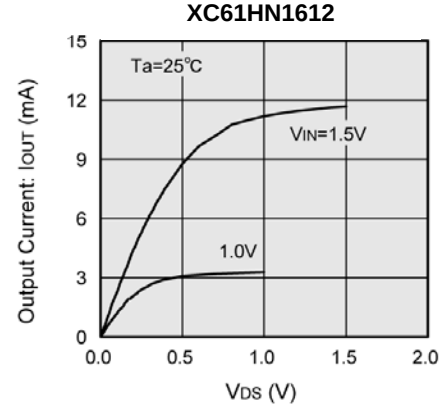


(4) N-Channel Driver Output Current vs. VDS

XC61HN1612



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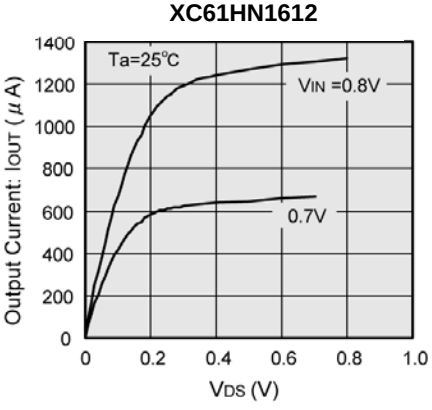

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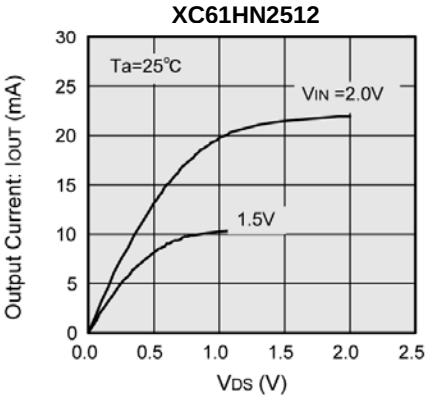
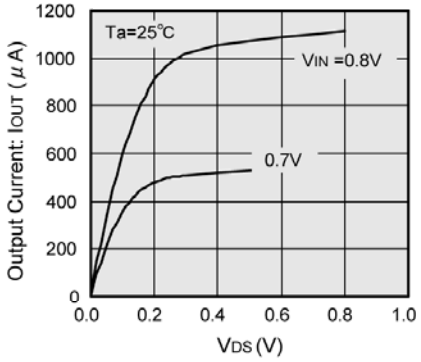


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) N-Channel Driver Output Current vs. VDS (Continued)

XC61HN2512



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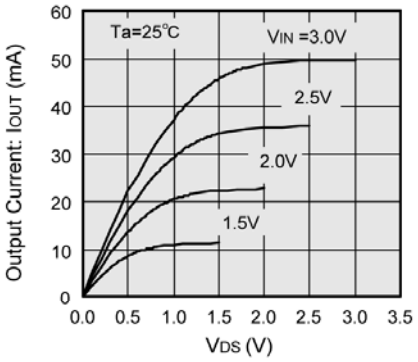

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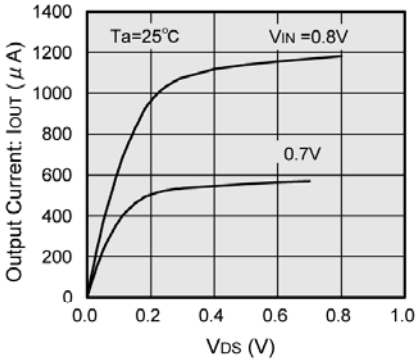
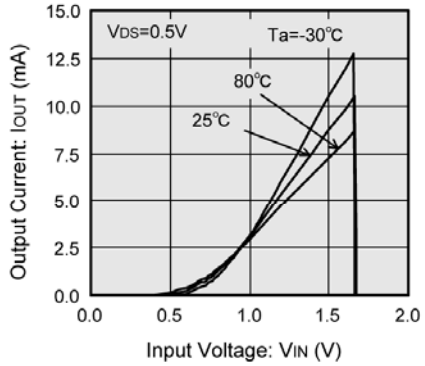


(5) N-Channel Driver Output Current vs. Input Voltage

XC61HN1612



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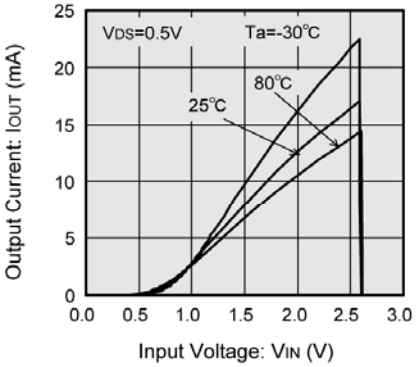

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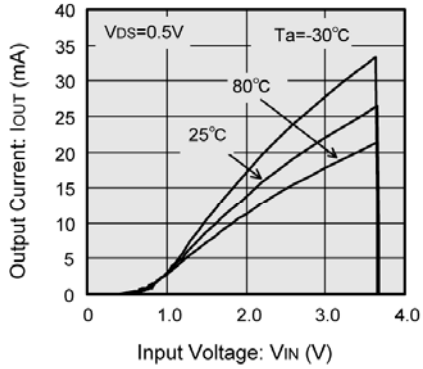
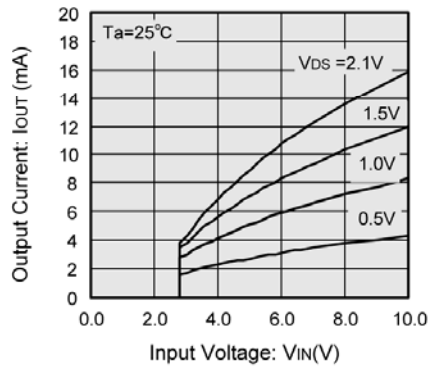


(6) P-Channel Driver Output Current vs. Input Voltage

XC61HC2712



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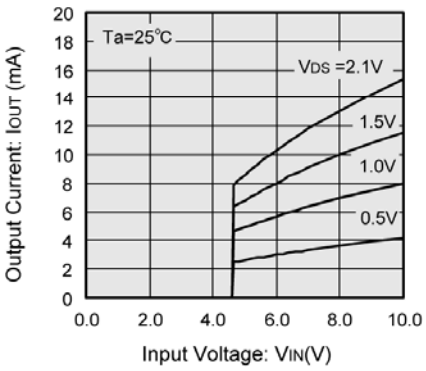
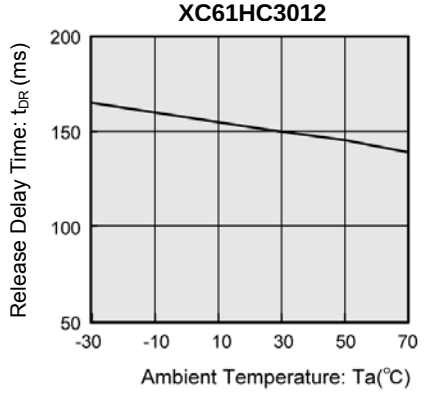


（7）Ambient Temperature vs. Release Delay Time (t_{DR})

XC61HC3012



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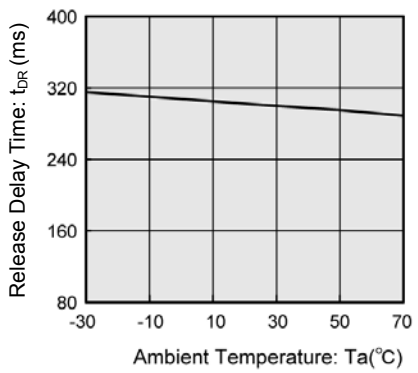

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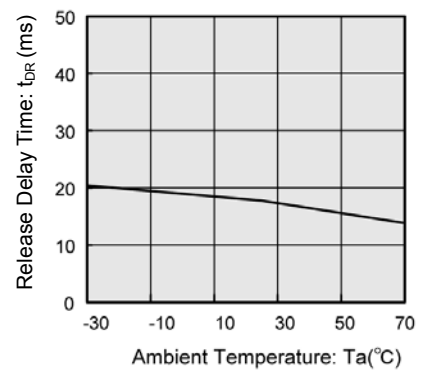
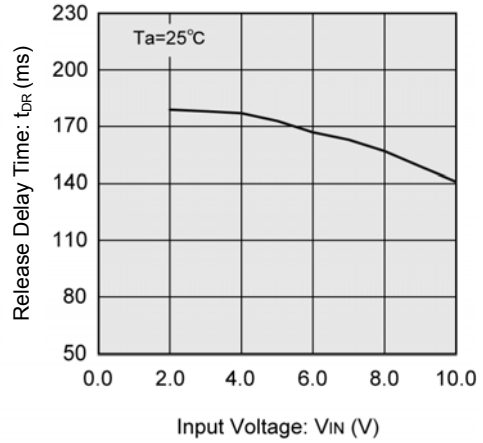


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

（8）Input Voltage vs. Release Delay Time (t_{DR})

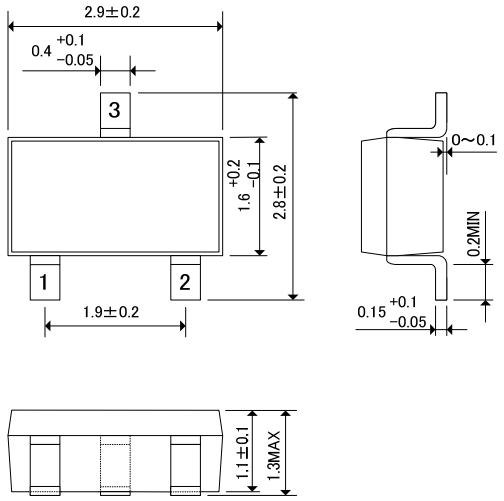
XC61HC2712



■PACKAGING INFORMATION

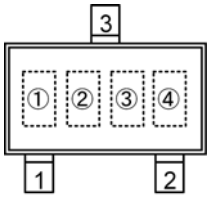
●SOT-23

(unit : mm)



■MARKING RULE

●SOT-23



SOT-23
(TOP VIEW)

① represents product series

MARK	PRODUCTS SERIES
8	XC61H*******-G

② standard：represents output configuration and integer number of detect voltage

CMOS output (XC61HC series)

MARK	VOLTAGE (V)
A	1. X
B	2. X
C	3. X
D	4. X
E	5. X
F	6. X

N-channel open drain (XC61HN series)

MARK	VOLTAGE (V)
P	1. X
R	2. X
S	3. X
T	4. X
U	5. X
V	6. X

③ represents decimal number of detect voltage and delay time.

DETECT VOLTAGE (V)	MARK		
	DELAY TIME 50ms～200ms (XC61H***1***-G)	DELAY TIME 80ms～400ms (XC61H***4***-G)	DELAY TIME 1ms～50ms (XC61H***5***-G)
X.0	0	A	N
X.1	1	B	P
X.2	2	C	R
X.3	3	D	S
X.4	4	E	T
X.5	5	F	U
X.6	6	H	V
X.7	7	K	X
X.8	8	L	Y
X.9	9	M	Z

④ represents production lot number
0 to 9, A to Z or inverted characters of 0 to 9, A to Z repeated.
(G, I, J, O, Q,W excluded)
*No character inversion used.

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