



# P-Channel 40-V (D-S) MOSFET

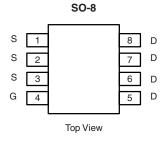
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
- 40	$0.014 \text{ at V}_{GS} = -10 \text{ V}$	- 10.5	40		
- 40	0.021 at V <sub>GS</sub> = - 4.5 V	- 8.7	40		

### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

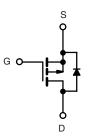






Ordering Information: Si4401BDY-T1-E3 (Lead (Pb)-free)

Si4401BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T <sub>A</sub> = 25 °C, unle	ss otherwise r	noted		
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	- 40		V
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current /T 150 °C\8	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 10.5	- 8.7	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		- 8.3	- 5.9	
Pulsed Drain Current		I <sub>DM</sub>	- 50		Α
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	- 2.6	- 1.36	
Avalanche Current	L = 1 mH	I <sub>AS</sub>	;	30	
Single Pulse Avalanche Energy	L=IIIII	E <sub>AS</sub>	45		mJ
Mariana Barra Birainatina	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.9	1.5	W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C		1.85	0.95	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manipulation to Applicate	t ≤ 10 s	R <sub>thJA</sub>	36	43	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	' 'thJA	70	84	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	16	21	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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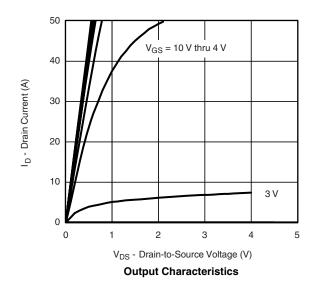
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	-					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1.0		- 3.0	V
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zana Cata Maltana Busin Comment	I <sub>DSS</sub>	V <sub>DS</sub> = - 40 V, V <sub>GS</sub> = 0 V		- 1		
Zero Gate Voltage Drain Current		$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			- 10	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 10 V	- 30			Α
5	D	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10.5 A		0.011	0.014	0
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 8.7 A		0.0165	0.021	Ω
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 10.5 A		26		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = - 2.7 A, V <sub>GS</sub> = 0 V		- 0.74	- 1.1	V
Dynamic <sup>b</sup>						
Total Gate Charge	$Q_g$			40	55	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15 \text{ V}, V_{GS} = -5 \text{ V}, I_{D} = -10.5 \text{ A}$		10		nC
Gate-Drain Charge	$Q_{gd}$			14		
Gate Resistance	$R_g$		1.4	2.8	4.2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			16	25	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 15 V, $R_L$ = 15 $\Omega$		15	25	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ - 1 A, $V_{GEN}=$ - 10 V, $R_g=$ 6 $\Omega$		97	150	ns
Fall Time	t <sub>f</sub>			47	75	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 2.1 A, dl/dt = 100 A/μs		35	55	

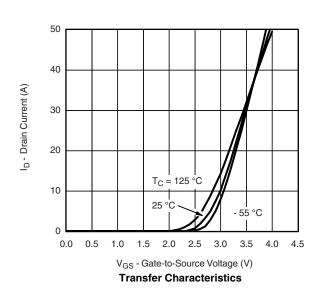
### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



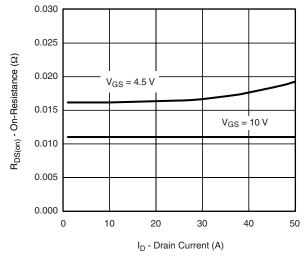




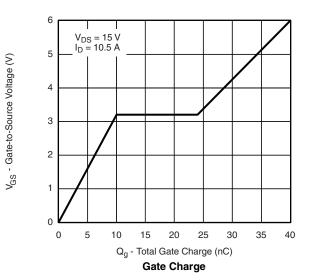


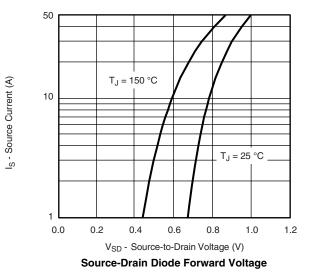


## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



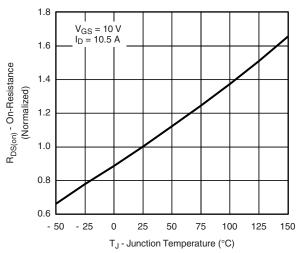
#### On-Resistance vs. Drain Current



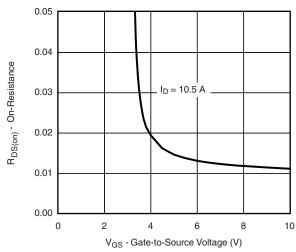


C - Capacitance (pF) Coss V<sub>DS</sub> - Drain-to-Source Voltage (V)

Capacitance



On-Resistance vs. Junction Temperature

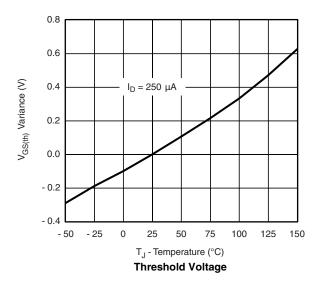


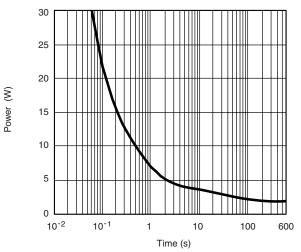
On-Resistance vs. Gate-to-Source Voltage

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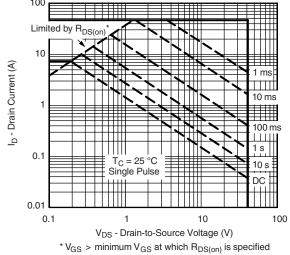
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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

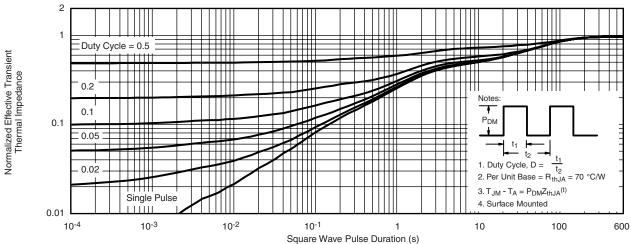




Single Pulse Power, Junction-to-Ambient



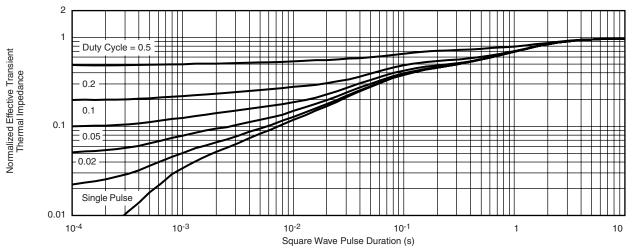
### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS INCHES			HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	0 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

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### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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