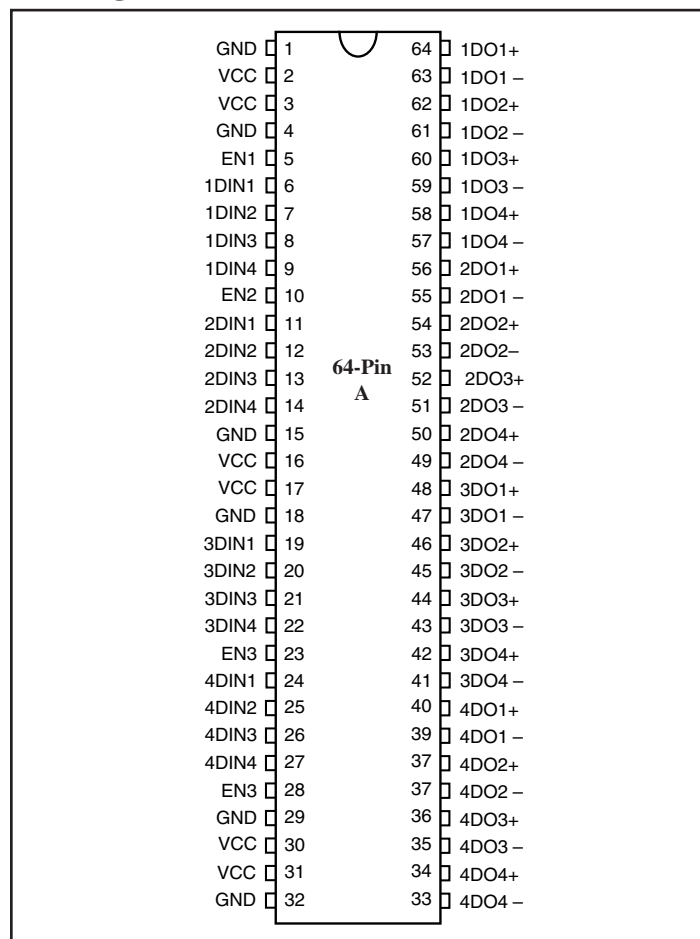


## High-Speed Differential Line Drivers

### Features

- Sixteen line drivers meet or exceed the requirements of the ANSI EIA/TIA-644 Standard
- Designed for signaling rates up to 500 Mbps with very low radiation (EMI)
- Low voltage differential signaling with typical output voltage of 350mV into :
  - 100Ω load (PI90LV387)
  - 50Ω load (PI90LVB387)
- Propagation delay times less than 2.6ns
- Output skew is less than 150ps
- Part-to-part skew is less than 1.5ns
- 35mW total power dissipation in each driver operating at 200 MHz
- Bus-pin ESD protection exceeds 10kV
- Low voltage TTL (LVTTTL) logic inputs are 5V tolerant
- Packaging (Pb-free & Green available):
  - 64-Pin TSSOP (A)

### Pin Diagram



### Description

PI90LV387/ PI90LVB387 consists of sixteen differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers output voltage levels to reduce power, increase switching speeds, and allow operation with a 3V supply rail.

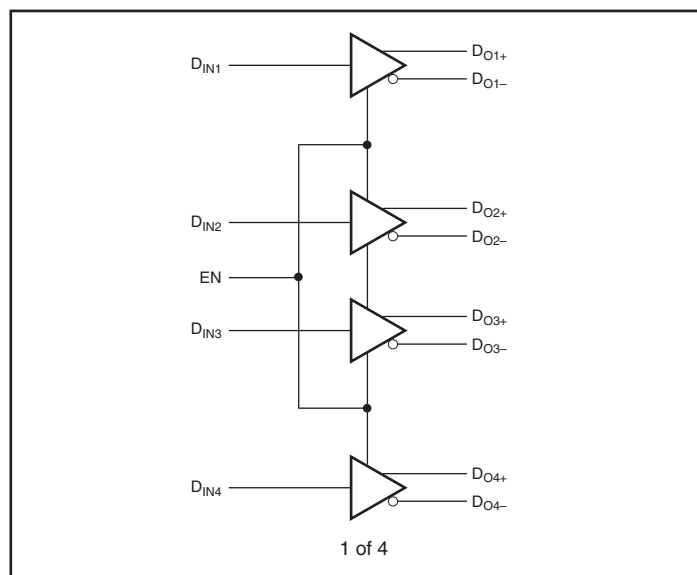
The intended application of this device and signaling technique is for point-to-point baseband (single termination) and multi-point (double termination) data transmission over a controlled impedance media of approximately 100Ω and 50Ω (LVB387). The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion 16-channel receivers, the PI90LV386 or PI90LVT386, over 400 million data transfers per second in single-edge clocked systems are possible with very little power.

(Note: The ultimate rate and distance of data transfer is dependent upon attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The drivers are enabled in groups of five. When disabled, driver outputs are at a high impedance. Each driver input ( $D_{IN}$ ) and enable (EN) have an internal pulldown that drives the input to a low level when open circuited.

The parts are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### Block Diagram



## Absolute Maximum Ratings

(Over Operating Free-Air Temperature, unless otherwise noted)<sup>(1)</sup>

Supply Voltage Range, $V_{CC}$ <sup>(2)</sup> .....	–0.5V to 4V
Voltage Range: Inputs .....	–0.5V to 6V
$D_{O+}$ or $D_{O-}$ .....	–0.5V to 4V
Electrostatic Discharge <sup>(3)</sup> :	
( $D_{O+}$ , $D_{O-}$ and GND).....	Class 3, A: 10kV, B:700V
(All Pins) .....	Class 3, A: 8kV, B:600V
Continuous Power Dissipation .....	(see dissipation rating table)
Storage Temperature Range .....	–65°C to 150°C
Lead Temperature 1.6mm (1/16 inch)	
from case for 10 seconds.....	260°C

### Notes:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.
2. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
3. Tested in accordance with MIL-STD-883C Method 3015.7

## Recommended Operating Conditions

	Min.	Nom.	Max.	Units
Supply Voltage, $V_{CC}$	3.0	3.3	3.6	V
High-level Input Voltage, $V_{IH}$	2.0			
Low-level Input Voltage, $V_{IL}$			0.8	
Operating free-air temperature, $T_A$	–40		85	°C

## Driver Function Table

Differential Input	Enables	Outputs	
$D_{IN}$	EN	$D_{OUT+}$	$D_{OUT-}$
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	L	H

### Notes:

1. H = high level,  
L = low level,  
X = irrelevant,  
Z = high impedance (off)

**Electrical Characteristics Over Recommended Operating Conditions** (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
$ V_{OH} $	Differential output voltage magnitude	$R_L = 50\Omega$ (LVB)		247	340	454	mV
$\Delta V_{OH} $	Change in differential output voltage magnitude between logic states	$R_L = 100\Omega$ (LV) See Figure 1 and 2		-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	LV	1.125		1.375	V
			LVB	1.000		1.375	
$\Delta V_{OC(SS)}$	Change in Steady-state common-mode output voltage between logic states	See Figure 3		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	
$I_{CC}$	Supply Current	$R_L = 50\Omega$ (LVB)	LV		60	78	mA
		$R_L = 100\Omega$ (LV) Enabled, $V_{IN} = GND$ or $V_{CC}$	LVB		122	190	
$I_{IH}$	High-Level input current	$V_{IH} = 2V$			3	20	$\mu A$
$I_{IL}$	Low-level input current	$V_{IL} = 0.8V$			2	10	
$I_{OS}$	Short-circuit output current	$V_{ODOUT+}$ or $V_{ODOUT-} = 0V$	LV			$\pm 24$	mA
			LVB			$\pm 48$	
		$V_{OD} = 0V$	LV			$\pm 12$	
			LVB			$\pm 24$	
$I_{OZ}$	High-impedance output current	$V_O = 0V$ or $V_{CC}$				$\pm 1$	$\mu A$
$I_{O(OFF)}$	Power-off output current	$V_{CC} = 0V$ , $V_O = 2.4V$				$\pm 1$	
$C_{IN}$	Input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5V$			6		pF
$C_O$	Output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5V$ , Disabled			9.4		

**Note:**

1. All typical values are at 25°C and with a 3.3V supply.

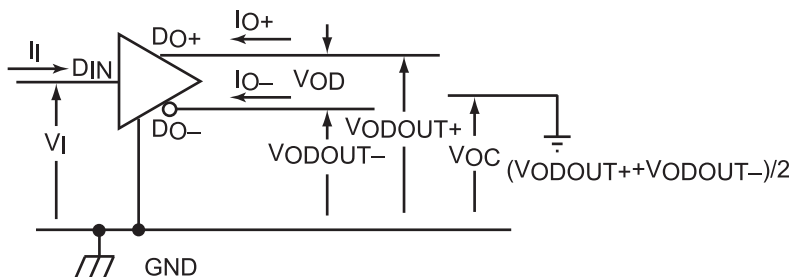
**Switching Characteristics** (Over Recommended Operating Conditions, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t <sub>PHL</sub>	Propagation delay time low-to-high level outputs	R <sub>L</sub> = 50Ω (LVB) R <sub>L</sub> = 100Ω (LV) C <sub>L</sub> = 10pF See Figure 4	0.9	1.8	2.6	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level outputs		0.9	1.8	2.6	
t <sub>r</sub>	Differential output sign rise time		0.4	0.8	1.3	
t <sub>f</sub>	Differential output signal fall time		0.4	0.8	1.3	
t <sub>sk(p)</sub>	Pulse skew (   t <sub>pHl</sub> - t <sub>pHl</sub>   )			150	500	ps
t <sub>sk(o)</sub>	Output skew <sup>(2)</sup>			80	150	
t <sub>sk(pp)</sub>	Part-to-part skew <sup>(3)</sup>				1.5	
t <sub>PZH</sub>	Propagation delay time, high impedance-to high-level output	See Figure 5		4.5	6.7	ns
t <sub>PZL</sub>	Propagation delay time, high impedance-to low-level output			3.5	5.1	
t <sub>PHZ</sub>	Propagation delay time, high-level-to-high-impedance output			3.1	4.6	
t <sub>PLZ</sub>	Propagation delay time, low-level-to-high-impedance output			3.1	4.6	
f <sub>MAX</sub>	Maximum operating frequency			250		MHz

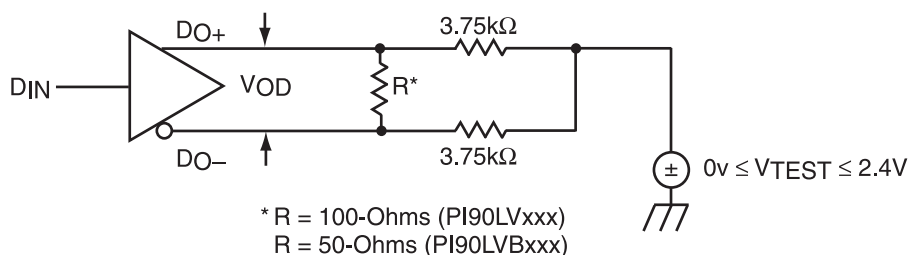
**Notes:**

1. All typical values are at 25°C and with a 3.3V supply
2. t<sub>sk(o)</sub> is the magnitude of the time difference between the t<sub>PLH</sub> or t<sub>PHL</sub> of all drivers of a single device with all of their inputs connected together.
3. t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits

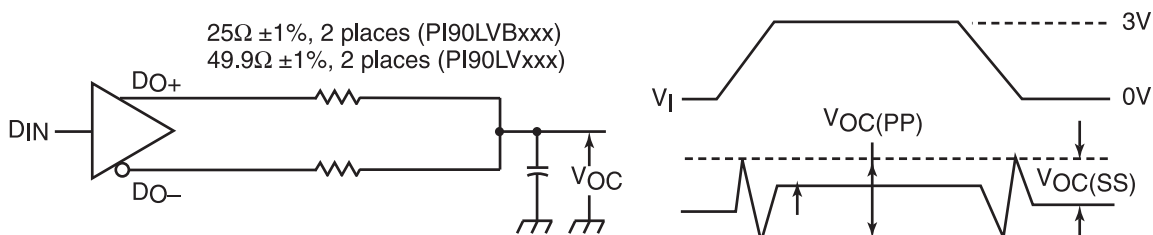
## Parameter Measurement Information



**Figure 1. Voltage and Current Definitions**



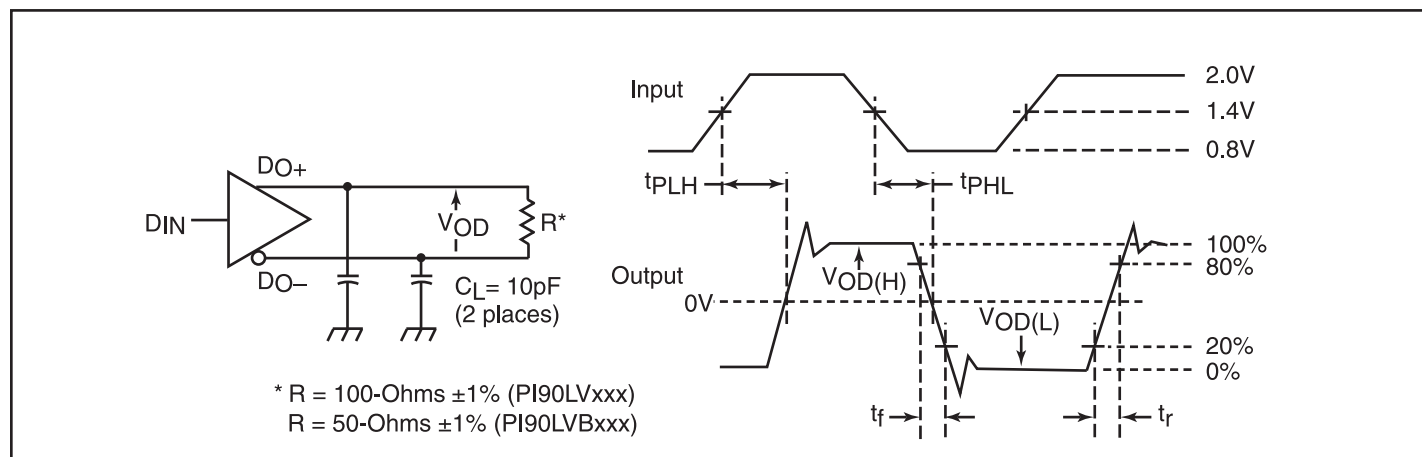
**Figure 2. VOD Test Circuit**



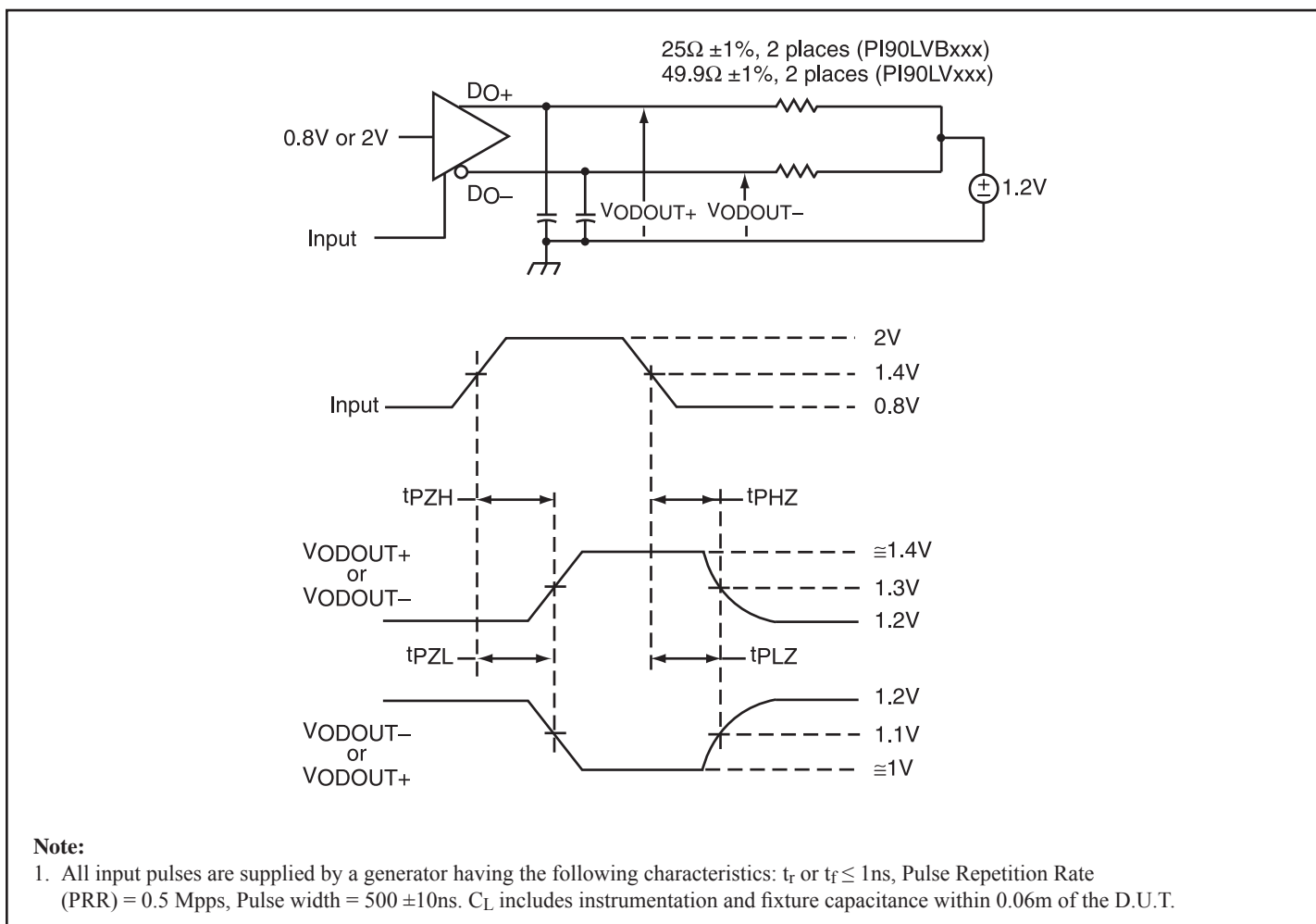
**Figure 3. Test Circuit & Definitions for the Driver Common-Mode Output Voltage**

### Note:

1. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1\text{ns}$ , Pulse Repetition Rate (PRR) = 50 Mpps, Pulse width =  $10 \pm 0.2\text{ns}$ .  $C_L$  includes instrumentation and fixture capacitance within 0.06m of the D.U.T. The measurement of  $VOC(PP)$  is made on test equipment with a -3dB bandwidth of at least 300MHz.

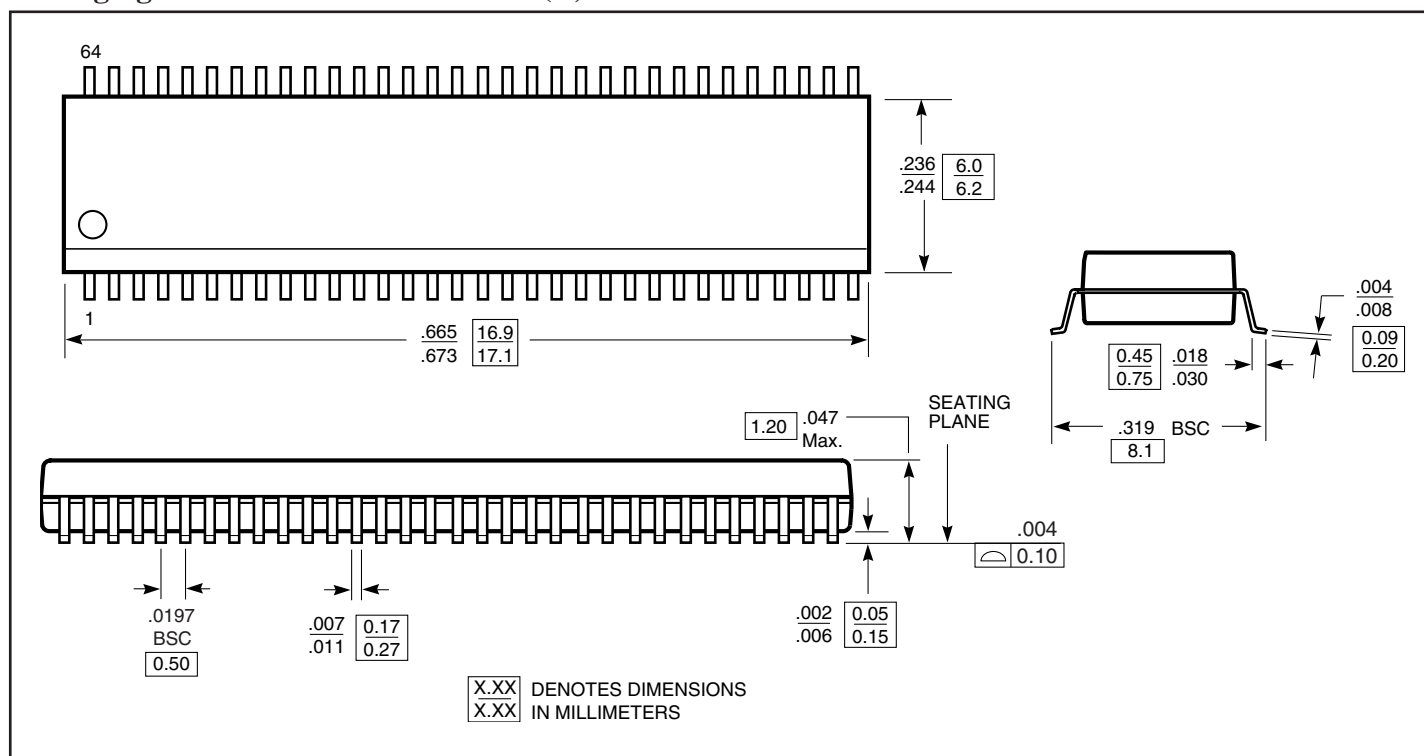
**Parameter Measurement Information (continued)**

**Figure 4. Test Circuit, Timing, & Voltage Definitions for the Differential Output Signal**
**Note:**

- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1\text{ns}$ , Pulse Repetition Rate (PRR) = 15 Mpps, Pulse width =  $10 \pm 0.2\text{ns}$ .  $C_L$  includes instrumentation and fixture capacitance within 0.06m of the D.U.T.


**Note:**

- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1\text{ns}$ , Pulse Repetition Rate (PRR) = 0.5 Mpps, Pulse width =  $500 \pm 10\text{ns}$ .  $C_L$  includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

**Figure 5. Enable & Disable Time Circuit & Definitions**

**Packaging Mechanical: 64-Pin TSSOP (A)**

**Ordering Information**

Ordering Code	Package Code	Package Type
PI90LV387AE	A	Pb-free & Green, 64-pin TSSOP
PI90LVB387A	A	64-pin TSSOP
PI90LVB387AE	A	Pb-free & Green, 64-pin TSSOP

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. Number of Transistors = TBD

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