AUDIO DIFFERENTIAL LINE RECEIVER 0dB (G = 1)

Check for Samples: INA2134-EP

FEATURES

- **Single and Dual Versions**
- **Low Distortion: 0.0005% at f = 1 kHz**
- **High Slew Rate: 14 V/ms**
- **Fast Settling Time: 3 ms to 0.01%**
- **Wide Supply Range: ±4 V to ±18 V**
- **Low Quiescent Current: 3.1 mA max**
- **High CMRR: 90 dB**
- **Fixed Gain = 0 dB (1V/V)**
- **Dual 14-Pin SOIC Package**

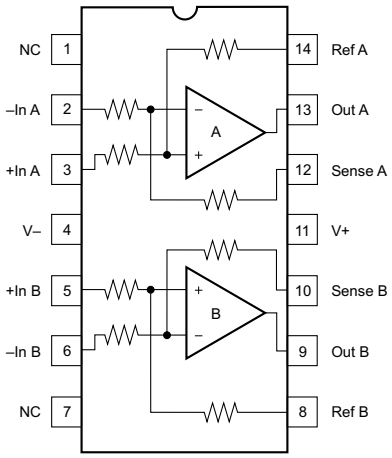
APPLICATIONS

- **Audio Differential Line Receiver**
- **Summing Amplifier**
- **Unity-Gain Inverting Amplifier**
- **Psuedoground Generator**
- **Instrumentation Building Block**
- **Current Shunt Monitor**
- **Voltage-Controlled Current Source**
- **Ground Loop Eliminator**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D PACKAGE
(TOP VIEW)



NC = No Connection

(1) Additional temperature ranges available - contact factory

DESCRIPTION

The INA2134 is a differential line receiver consisting of high performance op amps with onchip precision resistors. The device is fully specified for high performance audio applications and has excellent ac specifications, including low distortion (0.0005% at 1 kHz) and high slew rate (14 V/ms), assuring good dynamic response. In addition, wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. The dual version features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The INA2134 on-chip resistors are laser trimmed for accurate gain and optimum common-mode rejection. Furthermore, excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. Operation is guaranteed from ±4 V to ±18 V (8-V to 36-V total supply).

The INA2134 comes in a 14-pin SOIC surface-mount package and is specified for operation over the military temperature range, –55°C to 125°C.

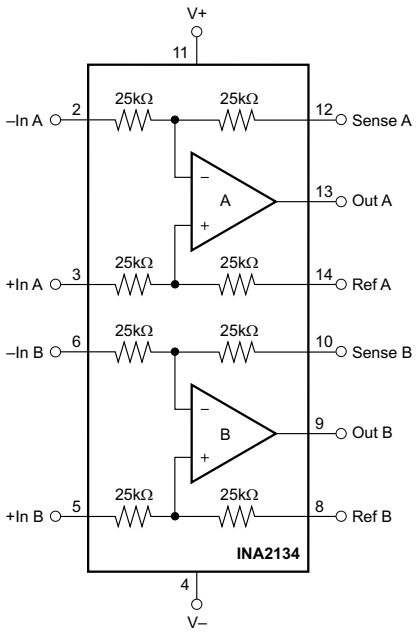
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	TOP-SIDE MARKING	ORDERABLE PART NUMBER	VID NUMBER	TRANSPORT MEDIA
–55°C to 125°C	SOIC-14 – D	INA2134M	INA2134MDREP	V62/12613-01XE	Tape and Reel, large
			INA2134MDEP	V62/12613-02XE	Tube

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage, V+ to V-		40	V
Input voltage range		±80	V
Output short-circuit (to ground)(2)		Continuous	
Operating temperature		-55 to 125	°C
Storage temperature		-65 to 150	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C
ESD Rating	Human Body Model (HBM)	500	V
	Machine Model (MM)	100	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) One channel per package.

THERMAL INFORMATION

THERMAL METRIC[1]		INA2134 D 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	73.1	°C/W
θ_{JC}	Junction-to-case thermal resistance	31.1	
θ_{JB}	Junction-to-board thermal resistance[3]	27.6	
ψ_{JT}	Junction-to-top characterization parameter[4]	3.2	
ψ_{JB}	Junction-to-board characterization parameter[5]	27.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

ELECTRICAL CHARACTERISTICS

At T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ, and Ref pin connected to Ground (unless otherwise noted).

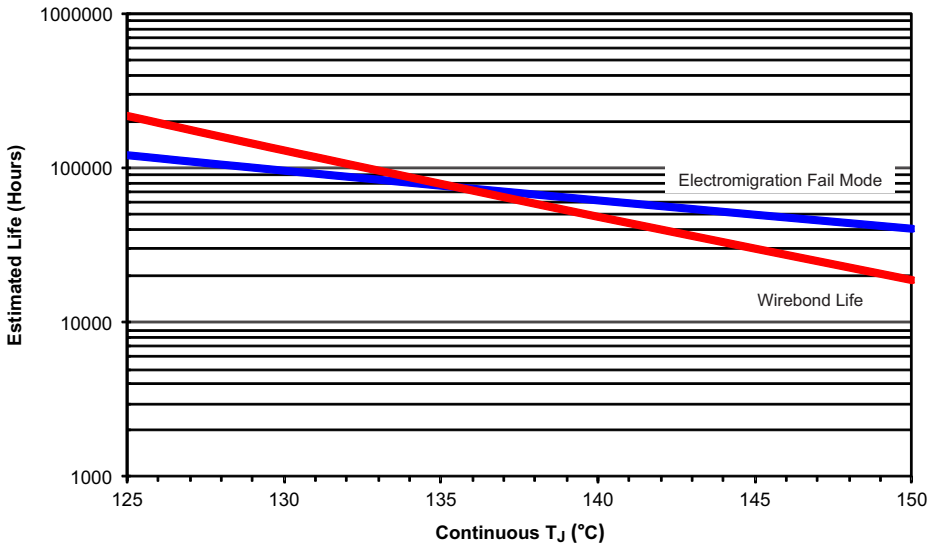
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
Total harmonic distortion + noise, f = 1 kHz		V_{IN} = 10 Vrms		0.0005		%
Noise floor[1]		20 kHz BW		-100		dBu
Headroom[1]		THD+N < 1%		23		dBu
FREQUENCY RESPONSE						
Small-signal bandwidth				3.1		MHz
Slew rate				14		V/µs
Settling time:	0.1%	10-V step, C_L = 100 pF		2		µs
	0.01%	10-V step, C_L = 100 pF		3		µs
Overload recovery time		50% overdrive		3		µs
Channel separation (dual), f = 1 kHz				117		dB
OUTPUT NOISE VOLTAGE[2]						
f = 20 Hz to 20 kHz				7		µVrms
f = 1 kHz				52		nV/√Hz
OFFSET VOLTAGE[3]						
Input offset voltage		V_{CM} = 0 V		±100	±1000	µV
	vs Temperature	-55°C to 125°C		±2		µV/°C
	vs Power supply	V_S = ±4 V to ±18 V, -55°C to 125°C		±5	±60	µV/V
INPUT						
Common-mode voltage range:	Positive	V_O = 0 V	2(V+) – 5	2(V+) – 4		V
	Negative	V_O = 0 V	2(V-) + 5	2(V-) + 2		V
Differential voltage range			See Typical Curve			
Common-mode rejection		V_{CM} = ±31 V, R_S = 0 Ω	74	90		dB
		V_{CM} = ±31 V, R_S = 0 Ω, -55°C to 125°C	72	85		dB
Impedance:[4]	Differential			50		kΩ
	Common-mode			50		kΩ

(1) dBu = 20log (Vrms/0.7746).
(2) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.
(3) Includes effects of amplifier's input bias and offset currents.
(4) 25-kΩ resistors are ratio matched, but have ±25% absolute value.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ, and Ref pin connected to Ground (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAIN						
Initial				1		V/V
Error		V_O = –16 V to 16 V		±0.02	±0.1	%
	vs Temperature	V_O = –16 V to 16 V, -55°C to 125°C		±2	±3.5	%
	Nonlinearity	V_O = –16 V to 16 V		0.0001		%
OUTPUT						
Voltage output:	Positive		(V+) – 2	(V+) – 1.8		V
	Negative		(V-) + 2	(V-) + 1.6		V
	Positive	Specified temperature range	(V+) – 2.45	(V+) – 2.1		V
	Negative	Specified temperature range	(V-) + 2.45	(V-) + 1.8		V
Current limit, continuous to common				±60		mA
Capacitive load (stable operation)				500		pF
POWER SUPPLY						
Rated voltage				±18		V
Voltage range			±4		±18	V
Quiescent current (per amplifier)		I_O = 0 A		±2.4	±2.9	mA
		I_O = 0 A, -55°C to 125°C		±2.7	±3.1	mA
TEMPERATURE RANGE						
Specified temperature range			–55		125	°C
Operating temperature range			–55		125	°C
Storage temperature range			–65		150	°C



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

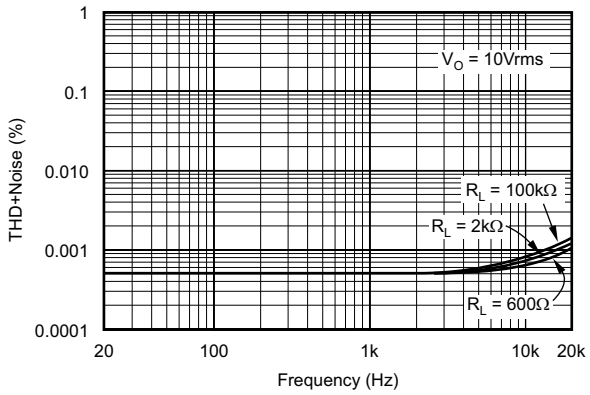
C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characterisitics.

Figure 1. INA2134 Electromigration Fail Mode/Wirebond Life Derating Chart

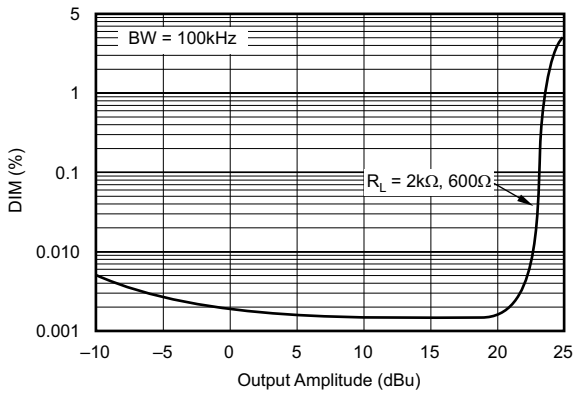
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = ±18 V (unless otherwise noted).

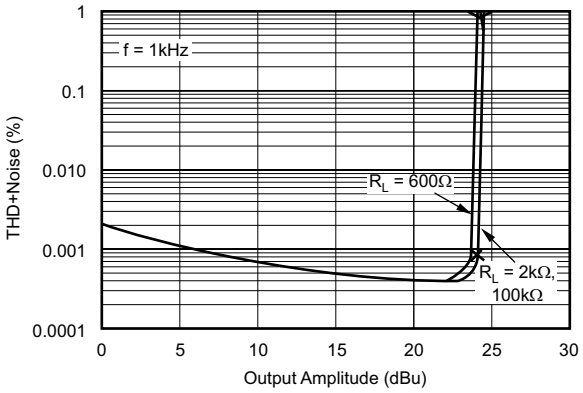
TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



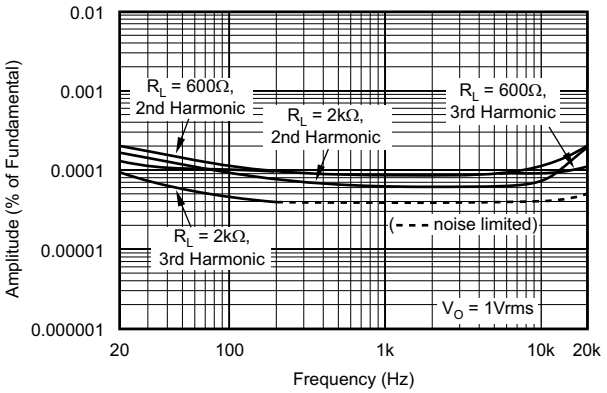
DIM INTERMODULATION DISTORTION vs OUTPUT AMPLITUDE



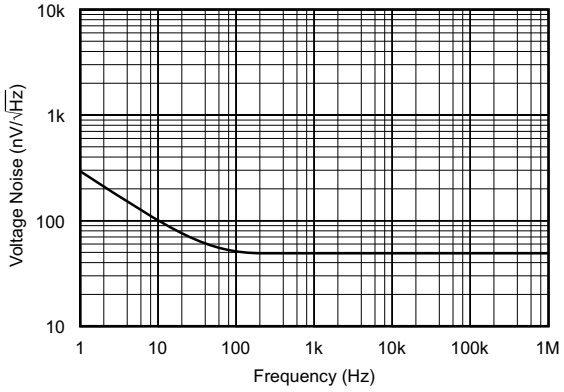
HEADROOM - TOTAL HARMONIC DISTORTION+NOISE vs OUTPUT AMPLITUDE



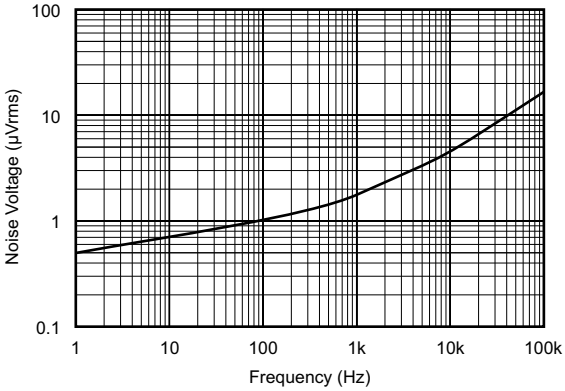
HARMONIC DISTORTION PRODUCTS vs FREQUENCY



OUTPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



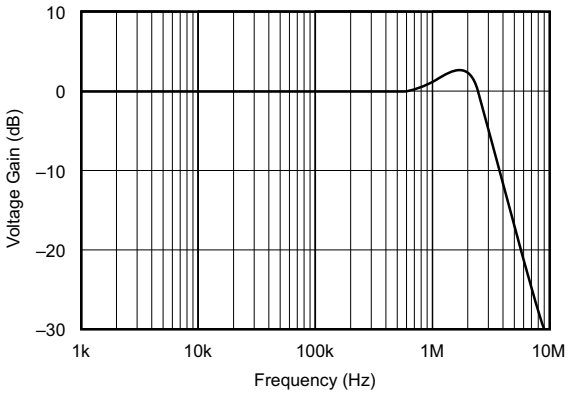
OUTPUT NOISE VOLTAGE vs NOISE BANDWIDTH



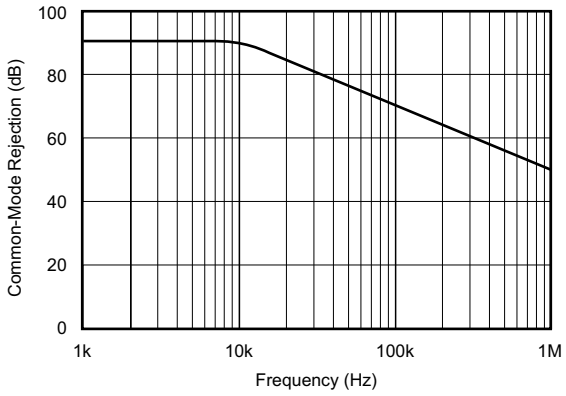
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V (unless otherwise noted).

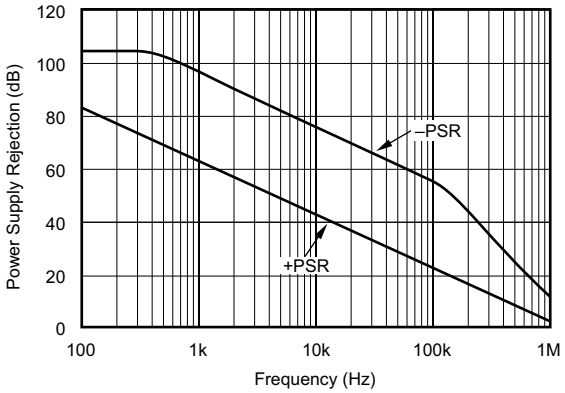
GAIN vs FREQUENCY



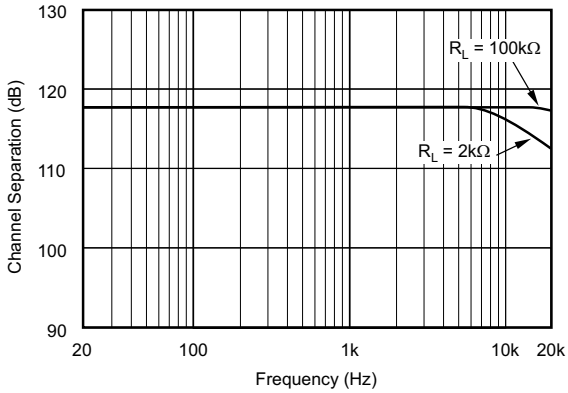
COMMON-MODE REJECTION vs FREQUENCY



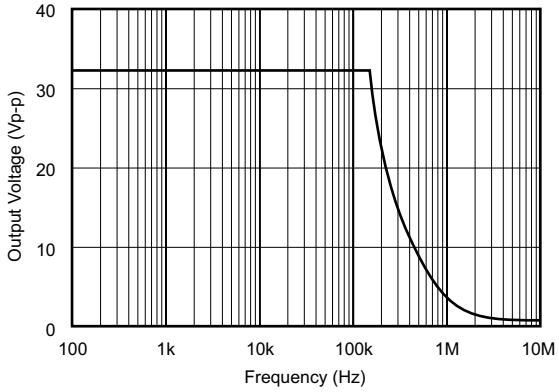
POWER SUPPLY REJECTION vs FREQUENCY



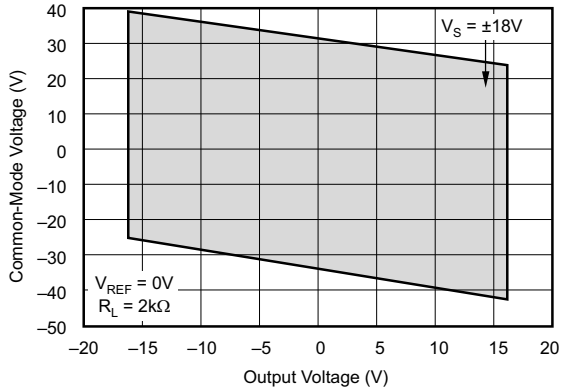
CHANNEL SEPARATION vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



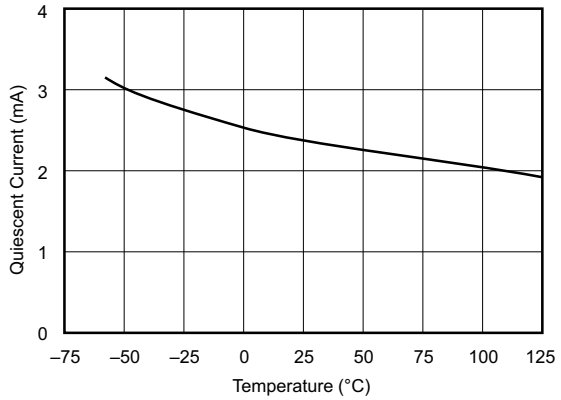
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



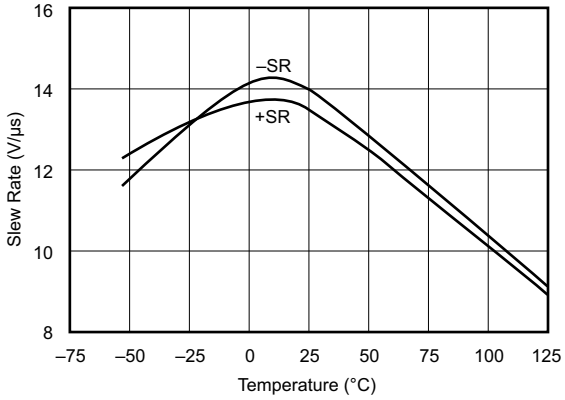
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V (unless otherwise noted).

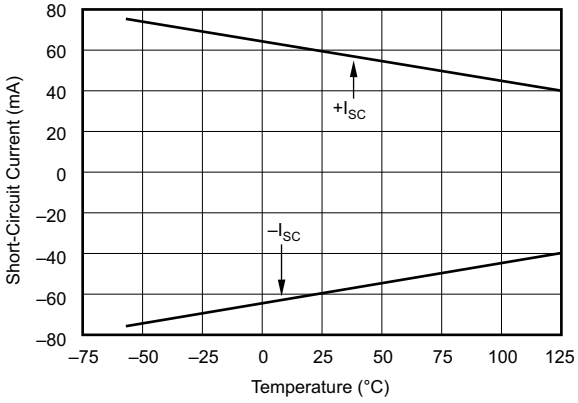
QUIESCENT CURRENT vs TEMPERATURE



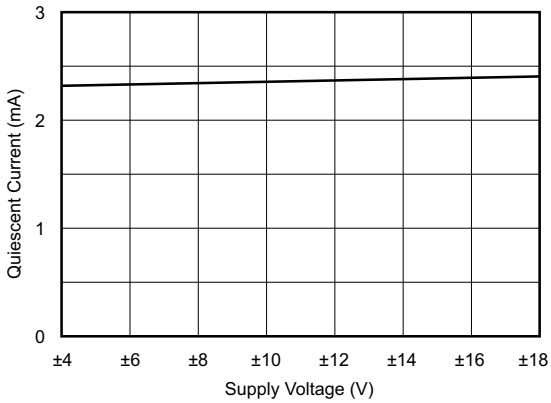
SLEW RATE vs TEMPERATURE



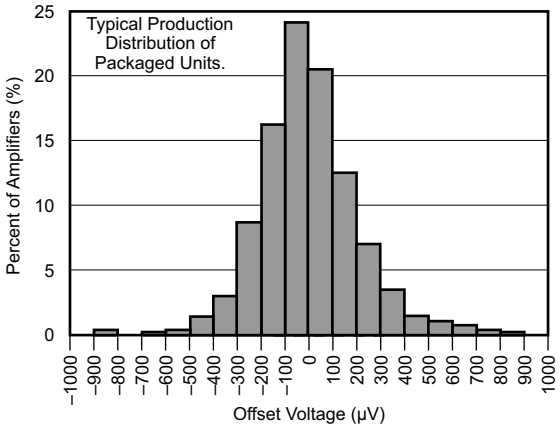
SHORT-CIRCUIT CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs SUPPLY VOLTAGE



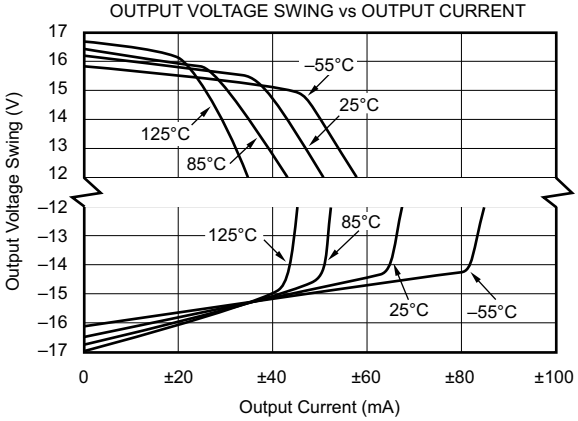
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



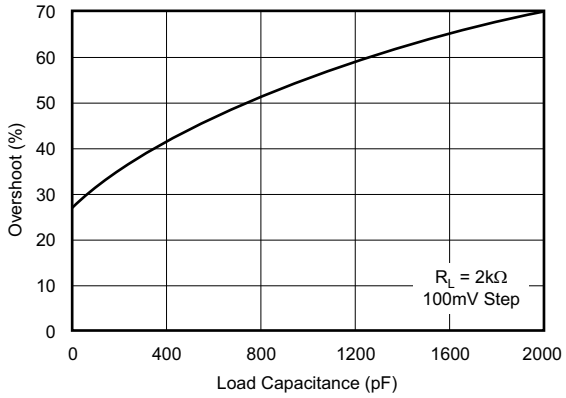
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V (unless otherwise noted).

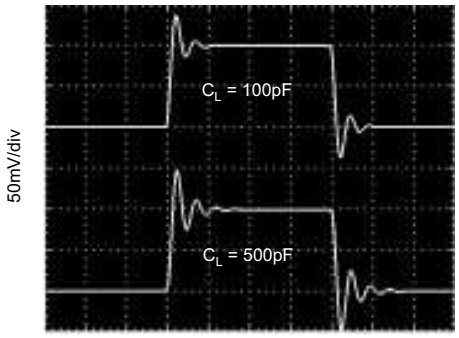
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



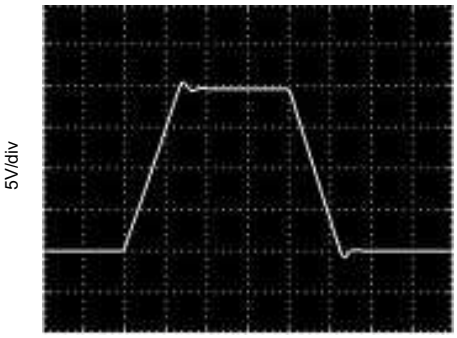
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



SMALL-SIGNAL STEP RESPONSE



LARGE-SIGNAL STEP RESPONSE
C_L = 500pF



APPLICATION INFORMATION

Basic Connection

Figure 2 shows the basic connections required for operation of the INA2134. Decoupling capacitors are strongly recommended in applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 2. All circuitry is completely independent in the dual version assuring lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 2, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to assure good common mode rejection. A 10-Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 74 dB. If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.

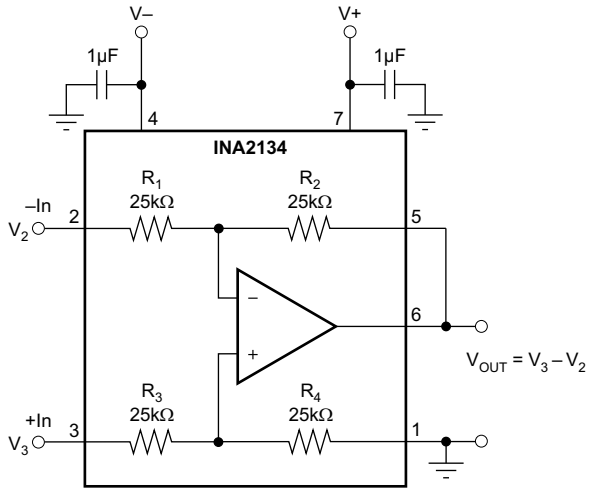


Figure 2. Precision Difference Amplifier (Basic Power Supply and Signal Connections)

Audio Performance

The INA2134 was designed for enhanced ac performance. Very low distortion, low noise, and wide bandwidth provide superior performance in high quality audio applications. Laser-trimmed matched resistors provide optimum common-mode rejection (typically 90 dB), especially when compared to circuits implemented with an operational amplifier and discrete precision resistors. In addition, high slew rate (14 V/µs) and fast settling time (3 ms to 0.01%) ensure good dynamic performance.

The INA2134 has excellent distortion characteristics. THD+Noise is below 0.002% throughout the audio frequency range. Up to approximately 10-kHz distortion is below the measurement limit of commonly used test equipment. Furthermore, distortion remains relatively flat over its wide output voltage swing range (approximately 1.7 V from either supply).

Offset Voltage Trim

The INA2134 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 3 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 3. The source impedance of a signal applied to the Ref terminal should be less than 10 Ω to maintain good common-mode rejection.

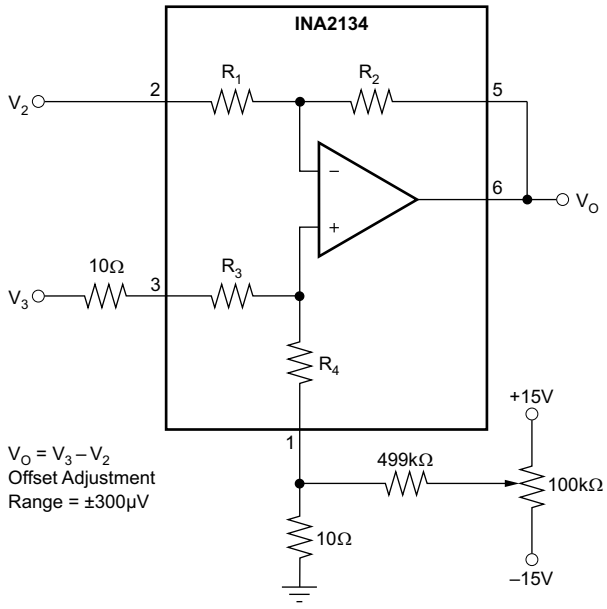


Figure 3. Offset Adjustment

Other Applications

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet (SBOS145) for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- ±10-V Precision Voltage Reference
- ±5- Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision G = 2 Amplifier
- Precision Summing Amplifier
- Precision G = 1/2 Amplifier
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator
- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low I_{OUT}
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of ±1 Amplifier

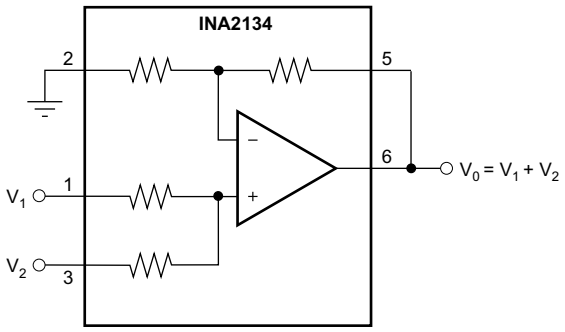


Figure 4. Precision Summing Amplifier

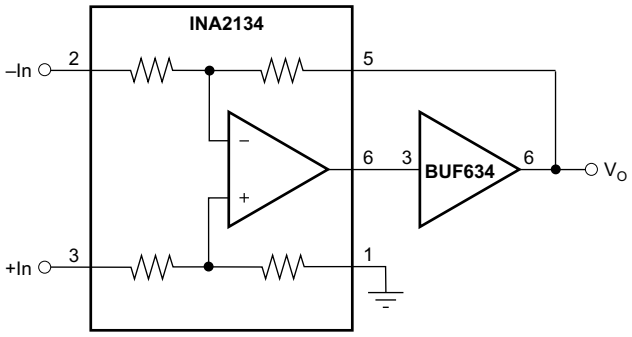
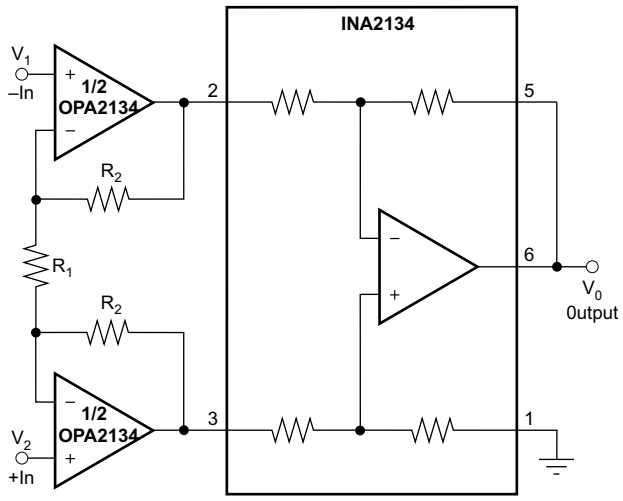


Figure 5. Boosting Output Current



$V_O = (1 + 2R_2/R_1)(V_2 - V_1)$

Figure 6. High Input Impedance Instrumentation Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA2134MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA2134M	Samples
V62/12613-01XE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA2134M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA2134-EP :

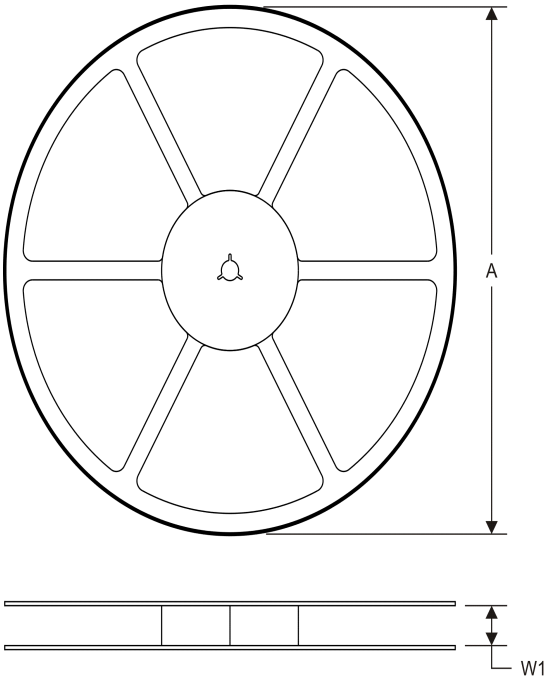
- Catalog: INA2134

NOTE: Qualified Version Definitions:

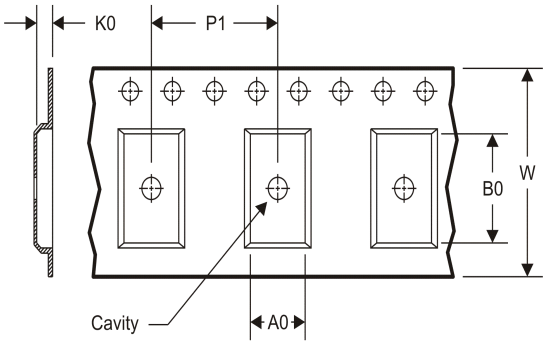
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



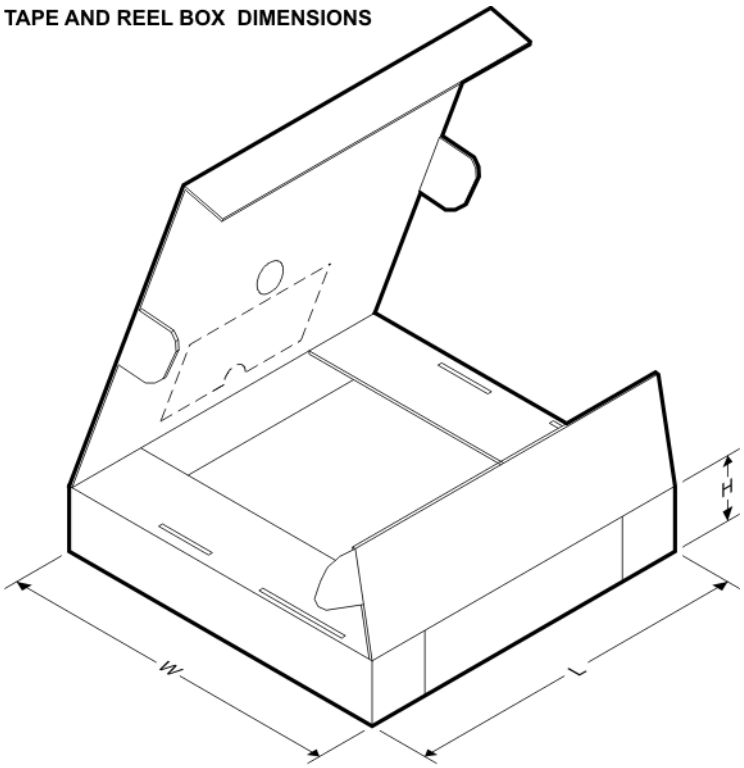
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2134MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

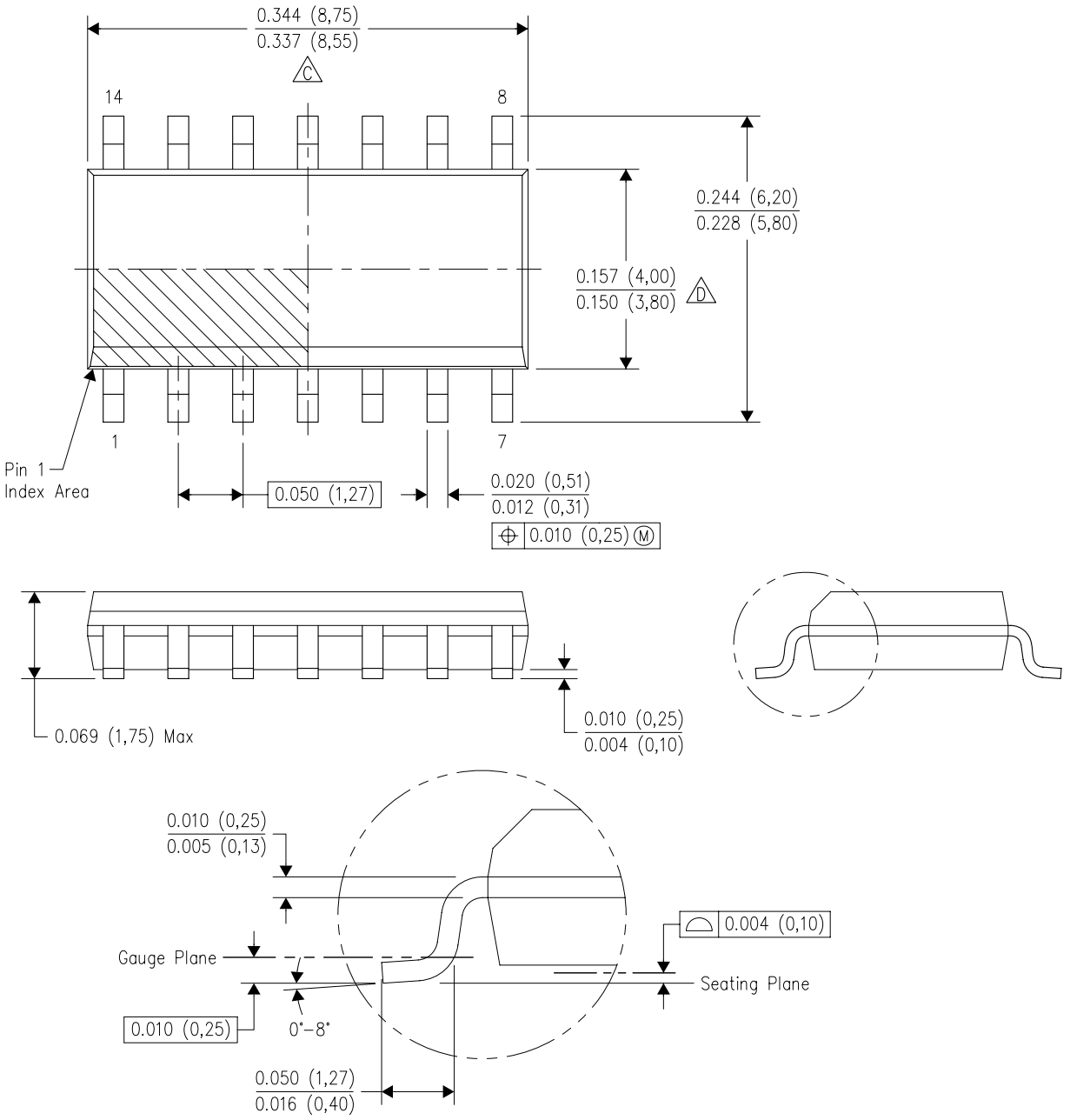
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2134MDREP	SOIC	D	14	2500	367.0	367.0	38.0

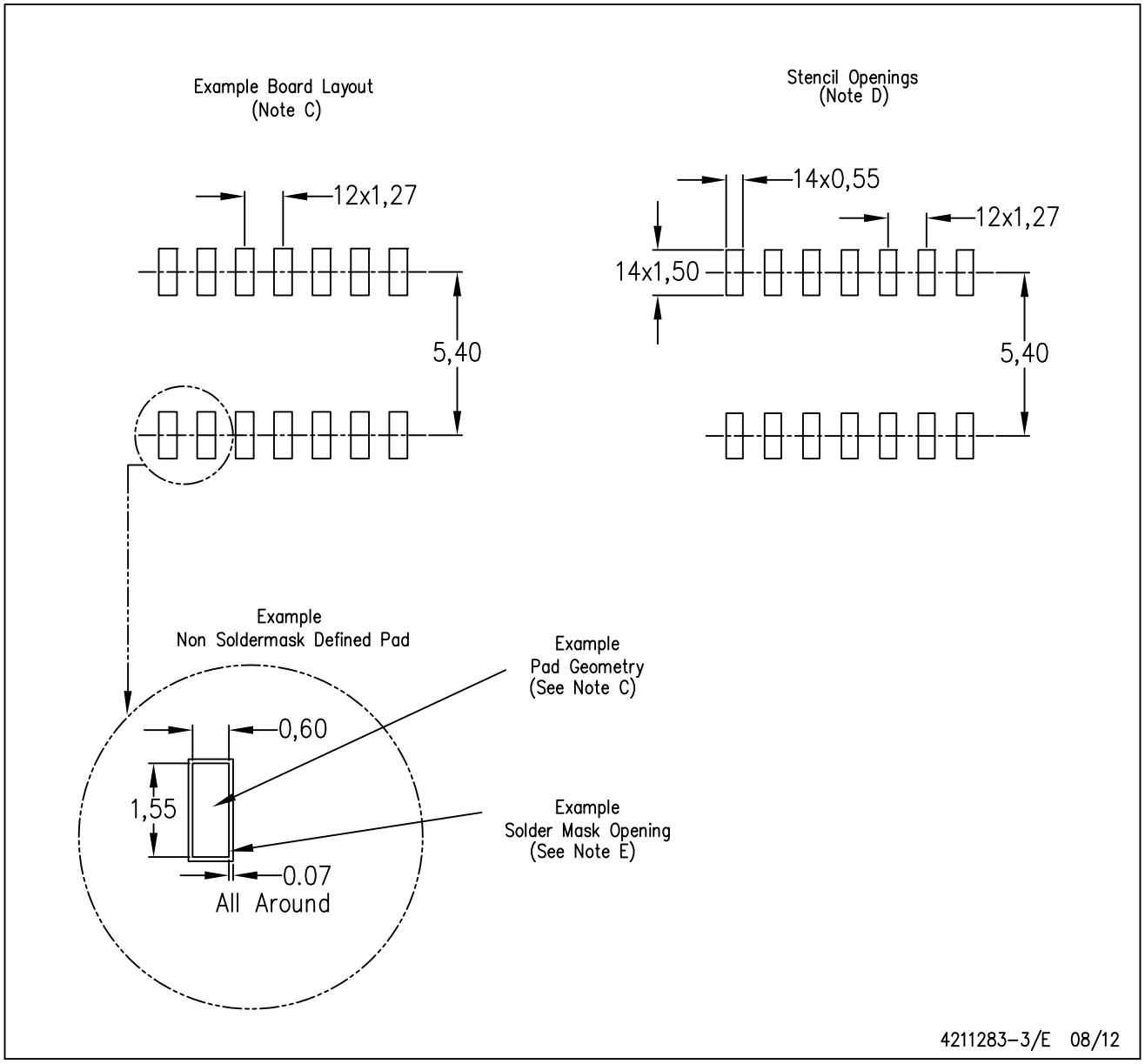
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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