

## High-Speed CMOS Logic 8-Bit Universal Shift Register; Three-State

### Features

- Buffered Inputs
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- Can be Cascaded for N-Bit Word Lengths
- I/O<sub>0</sub> - I/O<sub>7</sub> Bus Drive Capability and Three-State for Bus Oriented Applications
- Typical f<sub>MAX</sub> = 50MHz at V<sub>CC</sub> = 5V, C<sub>L</sub> = 15pF, T<sub>A</sub> = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N<sub>IL</sub> = 30%, N<sub>IH</sub> = 30% of V<sub>CC</sub> at V<sub>CC</sub> = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V<sub>IL</sub> = 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility, I<sub>I</sub> ≤ 1μA at V<sub>OL</sub>, V<sub>OH</sub>

### Description

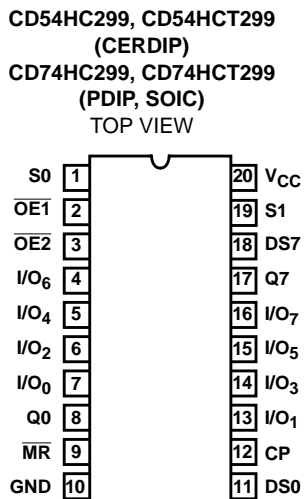
The 'HC259 and 'HCT299 are 8-bit shift/storage registers with three-state bus interface capability. The register has four synchronous-operating modes controlled by the two select inputs as shown in the mode select (S0, S1) table. The mode select, the serial data (DS0, DS7) and the parallel data (I/O<sub>0</sub> - I/O<sub>7</sub>) respond only to the low-to-high transition of the clock (CP) pulse. S0, S1 and data inputs must be stable one set-up time prior to the clock positive transition.

The Master Reset ( $\overline{MR}$ ) is an asynchronous active low input. When  $\overline{MR}$  output is low, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The three-state input/output I/O port has three modes of operation:

1. Both output enable ( $\overline{OE1}$  and  $\overline{OE2}$ ) inputs are low and S0 or S1 or both are low, the data in the register is presented at the eight outputs.
2. When both S0 and S1 are high, I/O terminals are in the high impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of  $\overline{OE1}$  and  $\overline{OE2}$ .
3. Either one of the two output enable inputs being high will force I/O terminals to be in the off-state. It is noted that each I/O terminal is a three-state output and a CMOS buffer input.

### Pinout

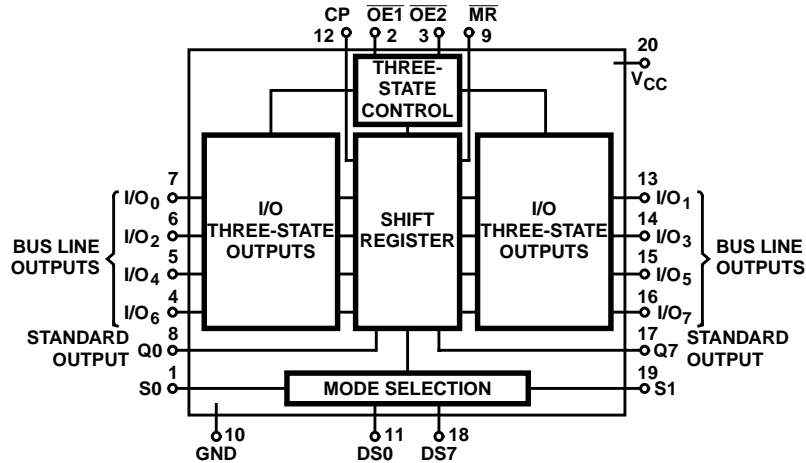


### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC299F3A	-55 to 125	20 Ld CERDIP
CD54HCT299F3A	-55 to 125	20 Ld CERDIP
CD74HC299E	-55 to 125	20 Ld PDIP
CD74HC299M	-55 to 125	20 Ld SOIC
CD74HC299M96	-55 to 125	20 Ld SOIC
CD74HCT299E	-55 to 125	20 Ld PDIP
CD74HCT299M	-55 to 125	20 Ld SOIC
CD74HCT299M96	-55 to 125	20 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

**Functional Diagram**



**MODE SELECT FUNCTION TABLE THREE-STATE I/O PORT OPERATING MODE**

FUNCTION	INPUTS				INPUTS/OUTPUTS	
	OE1	OE2	S0	S1	Qn (REGISTER)	I/O0 --- I/O7
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Qn = I/On	I/On = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

**TRUTH TABLE**

FUNCTION	INPUTS							REGISTER OUTPUTS				
	MR	CP	S0	S1	DS0	DS7	I/On	Q0	Q1	---	Q6	Q7
<b>RESET (CLEAR)</b>	L	X	X	X	X	X	X	L	L	---	L	L
Shift Right	H	↑	h	l	l	X	X	L	q0	---	q5	q6
	H	↑	h	l	h	X	X	H	q0	---	q5	Q6
Shift Left	H	↑	l	h	X	l	X	q1	q2	---	q7	L
	H	↑	l	h	X	h	X	q1	q2	---	q7	H
Hold (Do Nothing)	H	↑	l	l	X	X	X	q0	q1	---	q6	q7
Parallel Load	H	↑	h	h	X	X	l	L	L	---	L	L
	H	↑	h	h	X	X	h	H	H	---	H	H

H = Input Voltage High Level, h = Input voltage high one set-up timer prior clock transition; L = Input Voltage Low Level; l = Input voltage low one set-up time prior to clock transition; qn = Lower case letter indicates the state of the reference output one set-up time prior to clock transition; X - Voltage level on logic status don't care; Z = Output in high impedance state, ↑ = Low to High Clock Transition.

## CD54HC299, CD74HC299, CD54HCT299, CD74HCT299

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$ , For $-0.5V < V_O < V_{CC} + 0.5V$	
For Q Outputs .....	$\pm 25mA$
For I/O Outputs .....	$\pm 35mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
E (PDIP) Package .....	69
M (SOIC) Package .....	58
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C
(SOIC - Lead Tips Only)	

### Operating Conditions

Temperature Range, $T_A$ .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	.4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS		
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
<b>HC TYPES</b>														
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
				4.5	4.4	-	-	4.4	-	4.4	-	V		
				6	5.9	-	-	5.9	-	5.9	-	V		
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	Qn	I/On	-	-	-	-	-	-	V		
				-4	-6	4.5	3.98	-	-	3.84	-	3.7	-	V
				-5.2	-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
				4.5	-	-	0.1	-	0.1	-	0.1	V		
				6	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	Qn	I/On	-	-	-	-	-	-	V		
				4	6	4.5	-	-	0.26	-	0.33	-	0.4	V
				5.2	7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$		

**CD54HC299, CD74HC299, CD54HCT299, CD74HCT299**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
Three- State Leakage Current	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	-	6	-	-	±0.5	-	±5	-	±10	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Three- State Leakage Current	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	-	6	-	-	±0.5	-	±5	-	±10	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
S1, MR	0.25
I/O <sub>0</sub> - I/O <sub>7</sub>	0.25
DS0, DS7	0.25
S0, CP	0.6
OE1, OE2	0.3

NOTE: Unit Load is ΔI<sub>CC</sub> limit specific in Static Specifications Table, e.g., 360μA max. at 25°C.

**CD54HC299, CD74HC299, CD54HCT299, CD74HCT299**

**Prerequisite for Switching Specifications**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>HC TYPES</b>												
Maximum Clock Frequency	f <sub>MAX</sub>	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
MR Pulse Width	t <sub>W</sub>	2	50	-	-	65	-	-	75	-	-	ns
		4.5	10	-	-	13	-	-	15	-	-	ns
		6	9	-	-	11	-	-	13	-	-	ns
Clock Pulse Width	t <sub>W</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Setup Time DS0, DS7, I/On to Clock	t <sub>SU</sub>	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns
Hold Time DS0, DS7, I/On, S0, S1 to Clock	t <sub>H</sub>	2	0	-	-	0	-	-	0	-	-	ns
		4.5	0	-	-	0	-	-	0	-	-	ns
		6	0	-	-	0	-	-	0	-	-	ns
Recovery Time MR to Clock	t <sub>REC</sub>	2	5	-	-	5	-	-	5	-	-	ns
		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
Setup Time S1, S0 to Clock	t <sub>SU</sub>	2	120	-	-	150	-	-	180	-	-	ns
		4.5	24	-	-	30	-	-	36	-	-	ns
		6	20	-	-	26	-	-	31	-	-	ns
<b>HCT TYPES</b>												
Maximum Clock Frequency	f <sub>MAX</sub>	4.5	25	-	-	20	-	-	16	-	-	MHz
MR Pulse Width	t <sub>W</sub>	4.5	15	-	-	19	-	-	22	-	-	ns
Clock Pulse Width	t <sub>W</sub>	4.5	20	-	-	25	-	-	30	-	-	ns
Setup Time DS0, DS7, I/On, S0, S1 to Clock	t <sub>SU</sub>	4.5	20	-	-	25	-	-	30	-	-	ns
Hold Time DS0, DS7, I/On, S0, S1 to Clock	t <sub>H</sub>	4.5	0	-	-	0	-	-	0	-	-	ns
Recovery Time MR to Clock	t <sub>REC</sub>	4.5	5	-	-	5	-	-	5	-	-	ns
Setup Time S1, S0 to Clock	t <sub>SU</sub>	4.5	27	-	-	34	-	-	41	-	-	ns

**CD54HC299, CD74HC299, CD54HCT299, CD74HCT299**

**Switching Specifications**  $C_L = 50\text{pF}$ , Input  $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay Clock to I/O Output, Clock to Q0 and Q7, MR to Output	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	200	-	250	-	300	ns
			4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	34	-	43	-	51	ns
Output Enable and Disable Times	$t_{PZL}$	$C_L = 15\text{pF}$	5	-	10	-	-	-	-	-	ns
	$t_{PZH}, t_{PLZ}$		-	13	-	-	-	-	-	-	ns
	$t_{PHZ}$		-	15	-	-	-	-	-	-	ns
Output High-Z to High Level	$t_{PZH}$	$C_L = 50\text{pF}$	2	-	-	155	-	195	-	235	ns
			4.5	-	-	31	-	39	-	47	ns
			6	-	-	26	-	33	-	40	ns
Output High Level to High-Z	$t_{PHZ}$	$C_L = 50\text{pF}$	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
			6	-	-	31	-	39	-	48	ns
Output Low Level to High-Z	$t_{PLZ}$	$C_L = 50\text{pF}$	2	-	-	155	-	195	-	235	ns
			4.5	-	-	31	-	39	-	47	ns
			6	-	-	26	-	33	-	40	ns
Output High-Z to Low Level	$t_{PZL}$	$C_L = 50\text{pF}$	2	-	-	130	-	165	-	195	ns
			4.5	-	-	26	-	33	-	39	ns
			6	-	-	22	-	28	-	33	ns
Output Transition Time Q0, Q7	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
I/O <sub>0</sub> to I/O <sub>7</sub>	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	$C_I$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	$C_O$	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	$C_L = 15\text{pF}$	5	-	150	-	-	-	-	-	pF

**CD54HC299, CD74HC299, CD54HCT299, CD74HCT299**

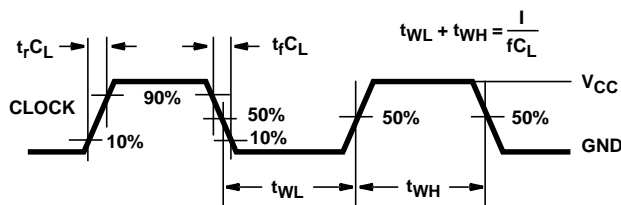
**Switching Specifications**  $C_L = 50\text{pF}$ , Input  $t_r$ ,  $t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>											
Propagation Delay Clock to I/O Output, Clock to Q0 and Q7	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	45	-	56	-	68	ns
		$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
$\overline{MR}$ to Output	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	46	-	58	-	69	ns
Output Enable and Disable Times	$t_{PZL}, t_{PZH}, t_{PLZ}, t_{PHZ}$	$C_L = 15\text{pF}$	5	-	10, 13, 15	-	-	-	-	-	ns
Output High-Z to High Level	$t_{PZH}$	$C_L = 50\text{pF}$	4.5	-	-	32	-	40	-	48	ns
Output High Level to High-Z	$t_{PHZ}$	$C_L = 50\text{pF}$	4.5	-	-	37	-	46	-	56	ns
Output Low Level to High-Z	$t_{PLZ}$	$C_L = 50\text{pF}$	4.5	-	-	32	-	40	-	48	ns
Output High-Z to Low Level	$t_{PZL}$	$C_L = 50\text{pF}$	4.5	-	-	30	-	38	-	45	ns
Output Transition Time Q0, Q7	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
I/O0 to I/O7		$C_L = 50\text{pF}$	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	$C_O$	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	$C_L = 15\text{pF}$	5	-	170	-	-	-	-	-	pF

**NOTES:**

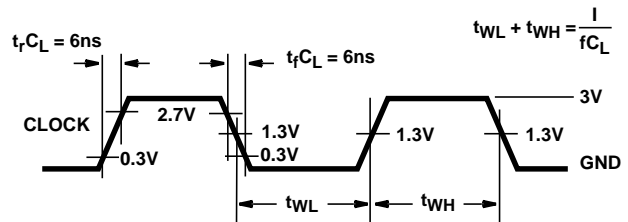
- $C_{PD}$  is used to determine the dynamic power consumption, per register.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

**Test Circuits and Waveforms**



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

Test Circuits and Waveforms (Continued)

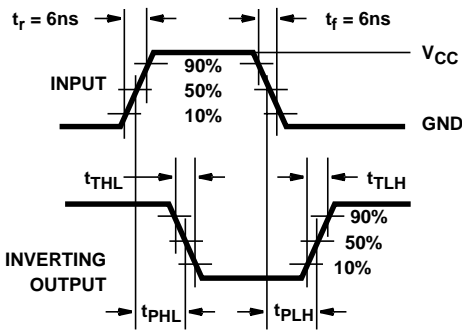


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

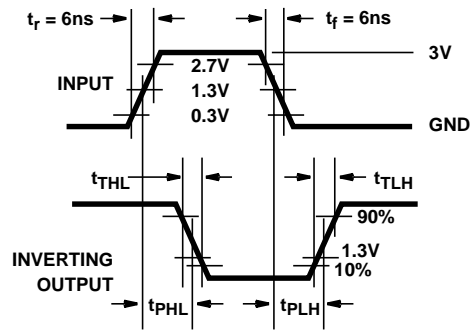


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

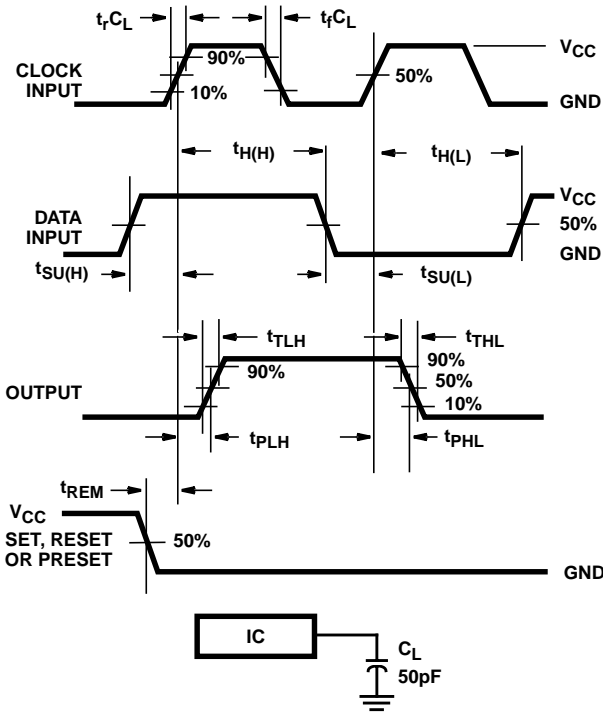


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

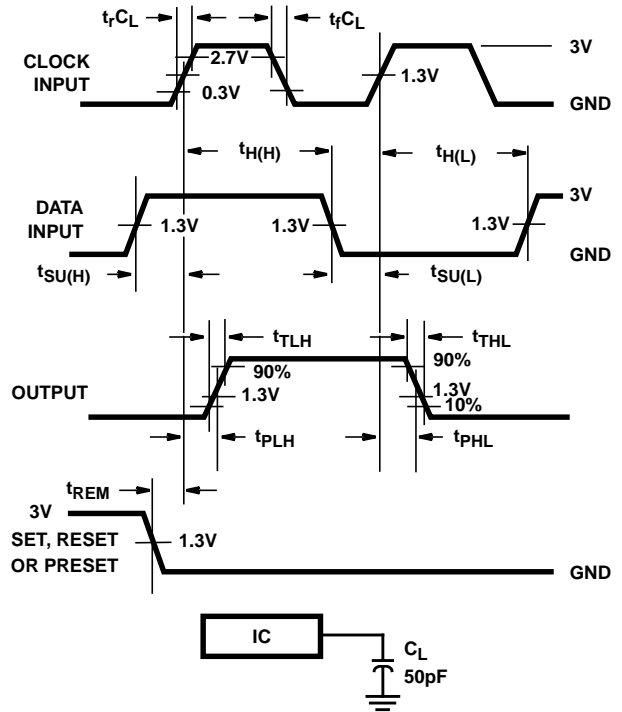


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS



**Test Circuits and Waveforms** (Continued)

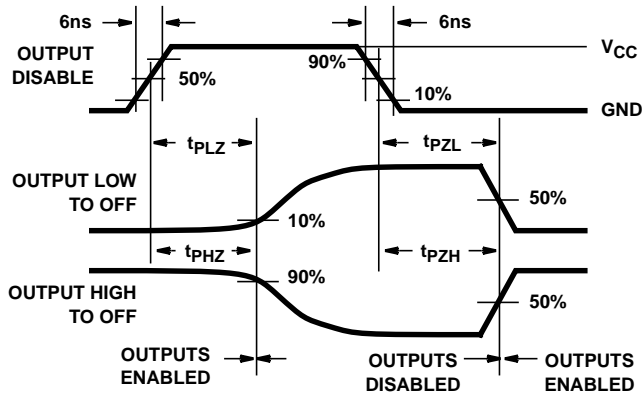


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

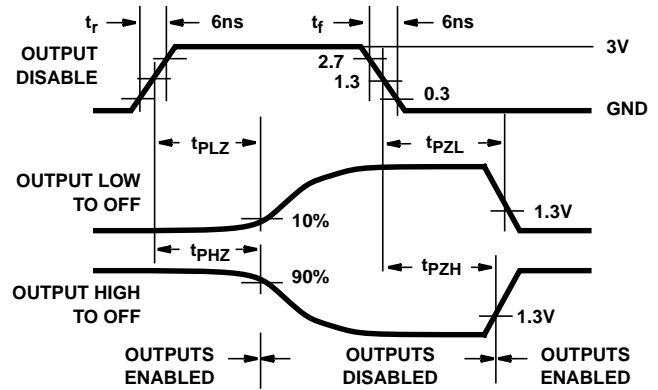


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8780601RA	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8780601RA CD54HC299F3A	<a href="#">Samples</a>
5962-8943601MRA	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8943601MR A CD54HCT299F3A	<a href="#">Samples</a>
CD54HC299F	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD54HC299F	<a href="#">Samples</a>
CD54HC299F3A	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8780601RA CD54HC299F3A	<a href="#">Samples</a>
CD54HCT299F3A	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8943601MR A CD54HCT299F3A	<a href="#">Samples</a>
CD74HC299E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC299E	<a href="#">Samples</a>
CD74HC299M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC299M	<a href="#">Samples</a>
CD74HC299M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC299M	<a href="#">Samples</a>
CD74HC299M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC299M	<a href="#">Samples</a>
CD74HCT299E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT299E	<a href="#">Samples</a>
CD74HCT299M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT299M	<a href="#">Samples</a>
CD74HCT299M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT299M	<a href="#">Samples</a>
CD74HCT299M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT299M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC299, CD54HCT299, CD74HC299, CD74HCT299 :**

● Catalog: [CD74HC299](#), [CD74HCT299](#)

● Military: [CD54HC299](#), [CD54HCT299](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HCT299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC299M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT299M96	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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