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January 2008

74AC240, 74ACT240 Octal Buffer/Line Driver with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inverting 3-STATE outputs drive bus lines or buffer memory address registers

Outputs source/sink 24mA

ACT240 has TTL-compatible inputs

General Description

The AC/ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

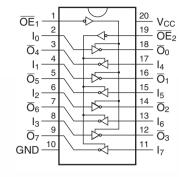
Ordering	Information
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Order Number	Package Number	Package Description
74AC240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

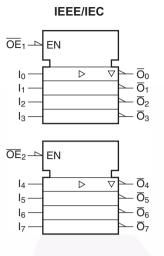
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I ₀ —I ₇	Inputs
$\overline{O}_0 - \overline{O}_7$	Outputs

Truth Tables

Inp	uts	Outputs
OE ₁	I _n	(Pins 12, 14, 16, 18)
L	L	Н
L	Н	L
Н	Х	Z

Inp	uts	Outputs
OE ₂	I _n	(Pins 3, 5, 7, 9)
L	L	Н
L	Н	L
Н	Х	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5V to +7.0V
I _{IK}	DC Input Diode Current	
	$V_{I} = -0.5V$	–20mA
	$V_{I} = V_{CC} + 0.5$	+20mA
VI	DC Input Voltage	-0.5V to V _{CC} + 0.5V
I _{OK}	DC Output Diode Current	
	$V_{O} = -0.5V$	-20mA
	$V_{O} = V_{CC} + 0.5V$	+20mA
Vo	DC Output Voltage	-0.5V to V _{CC} + 0.5V
Io	DC Output Source or Sink Current	±50mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current per Output Pin	±50mA
T _{STG}	Storage Temperature	-65°C to +150°C
TJ	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
VI	Input Voltage	0V to V _{CC}
Vo	Output Voltage	0V to V _{CC}
T _A	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices:	125mV/ns
	V _{IN} from 30% to 70% of V _{CC} , V _{CC} @ 3.3V, 4.5V, 5.5V	
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices:	125mV/ns
	V _{IN} from 0.8V to 2.0V, V _{CC} @ 4.5V, 5.5V	

				T _A = -	+ 25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol	Parameter	V _{CC} (V)	Conditions	Typ. G		uaranteed Limits	Unit
V _{IH}	Minimum HIGH Level	3.0	V _{OUT} = 0.1V or	1.5	2.1	2.1	V
	Input Voltage	4.5	V _{CC} – 0.1V	2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V _{IL}	Maximum LOW Level	3.0	V _{OUT} = 0.1V or	1.5	0.9	0.9	V
	Input Voltage	4.5	V _{CC} – 0.1V	2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V _{OH}	Minimum HIGH Level	3.0	Ι _{ΟUT} = –50μΑ	2.99	2.9	2.9	V
	Output Voltage	4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
	3.0	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -12 \text{mA}$		2.56	2.46		
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24 \text{mA}$		3.86	3.76	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24 \text{mA}^{(1)}$		4.86	4.76	
V _{OL} Maximum LOW Leve	Maximum LOW Level	3.0	Ι _{ΟUT} = 50μΑ	0.002	0.1	0.1	V
	Output Voltage	4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 12 \text{mA}$		0.36	0.44	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}^{(1)}$		0.36	0.44	
I _{IN} ⁽²⁾	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0	μA
I _{OZ}	Maximum 3-STATE Leakage Current	5.5	$\label{eq:VI} \begin{array}{l} V_{I}\left(OE\right)=V_{IL},V_{IH};\\ V_{I}=V_{CC},GND;\\ V_{O}=V_{CC},GND \end{array}$		±0.25	±2.5	μA
I _{OLD}	Minimum Dynamic	5.5	V _{OLD} = 1.65V Max.			75	mA
I _{OHD}	Output Current ⁽³⁾	5.5	V _{OHD} = 3.85V Min.			-75	mA
I _{CC} ⁽²⁾	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.

2. $I_{\rm IN}$ and $I_{\rm CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{\rm CC}.$

3. Maximum test duration 2.0ms, one output loaded at a time.

				$T_A = -$	+25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol	Parameter	V _{CC} (V)	Conditions	Тур.	G	uaranteed Limits	Units
V _{IH}	Minimum HIGH Level	4.5	$V_{OUT} = 0.1V \text{ or}$	1.5	2.0	2.0	V
	Input Voltage	5.5	V _{CC} – 0.1V	1.5	2.0	2.0	
V _{IL}	Maximum LOW	4.5	$V_{OUT} = 0.1V$ or	1.5	0.8	0.8	V
	Level Input Voltage	5.5	V _{CC} – 0.1V	1.5	0.8	0.8	
V _{OH}	Minimum HIGH Level	4.5	$I_{OUT} = -50 \mu A$	4.49	4.4	4.4	V
	Output Voltage	5.5		5.49	5.4	5.4	
	4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24 \text{mA}$		3.86	3.76		
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24 \text{mA}^{(4)}$		4.86	4.76	
V _{OL} Maximum LOW	4.5	Ι _{ΟUT} = 50μΑ	0.001	0.1	0.1	V	
	Level Output Voltage	5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}^{(4)}$		0.36	0.44	
I _{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}, \text{ GND}$		±0.1	±1.0	μA
I _{OZ}	Maximum 3-STATE Leakage Current	5.5	$V_{I} = V_{IL}, V_{IH};$ $V_{O} = V_{CC}, \text{ GND}$		±0.25	±2.5	μA
I _{CCT}	Maximum I _{CC} /Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I _{OLD}	Minimum Dynamic	5.5	V _{OLD} = 1.65V Max.			75	mA
I _{OHD}	Output Current ⁽⁵⁾	5.5	V _{OHD} = 3.85V Min.			-75	mA
I _{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

1.01

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

			T, C	_A = +25° C _L = 50p	C, F	$\begin{array}{c} T_{A} = -40^{\circ}C\\ C_{L} = \end{array}$	C to +85°C, 50pF	
Symbol	Parameter	V _{CC} (V) ⁽⁶⁾	Min.	Тур.	Max.	Min.	Max.	Units
t _{PLH}	Propagation Delay	3.3	1.5	6.0	8.0	1.0	9.0	ns
	Data to Output	5.0	1.5	4.5	6.5	1.0	7.0	1
t _{PHL}	Propagation Delay	3.3	1.5	5.5	8.0	1.0	8.5	ns
	Data to Output	5.0	1.5	4.5	6.0	1.0	6.5	1
t _{PZH}	Output Enable Time	3.3	1.5	6.0	10.5	1.0	11.0	ns
		5.0	1.5	5.0	7.0	1.0	8.0	1
t _{PZL}	Output Enable Time	3.3	1.5	7.0	10.0	1.0	11.0	ns
		5.0	1.5	5.5	8.0	1.0	8.5	1
t _{PHZ}	Output Disable Time	3.3	1.5	7.0	10.0	1.0	10.5	ns
		5.0	1.5	6.5	9.0	1.0	9.5	1
t _{PLZ}	Output Disable Time	3.3	1.5	7.5	10.5	1.0	11.5	ns
		5.0	1.5	6.5	9.0	1.0	9.5	1

Note:

6. Voltage range 3.3 is 3.3V \pm 0.3V. Voltage range 5.0 is 5.0V \pm 0.5V.

AC Electrical Characteristics for ACT

			T _A = +25°C, C _L = 50pF		$T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C,$ $C_{L} = 50\text{ pF}$			
Symbol	Parameter	V _{CC} (V) ⁽⁷⁾	Min.	Тур.	Max.	Min.	Max.	Units
t _{PLH}	Propagation Delay, Data to Output	5.0	1.5	6.0	8.5	1.5	9.5	ns
t _{PHL}	Propagation Delay, Data to Output	5.0	1.5	5.5	7.5	1.5	8.5	ns
t _{PZH}	Output Enable Time	5.0	1.5	7.0	8.5	1.0	9.5	ns
t _{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.5	10.5	ns
t _{PHZ}	Output Disable Time	5.0	2.0	8.0	9.5	2.0	10.5	ns
t _{PLZ}	Output Disable Time	5.0	2.5	6.5	10.0	2.0	10.5	ns

Note:

7. Voltage range 5.0 is 5.0V \pm 0.5V.

Capacitance

Symbol	Parameter	Conditions	Тур.	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN	4.5	pF
C _{PD}	Power Dissipation Capacitance	$V_{CC} = 5.0V$	45.0	pF

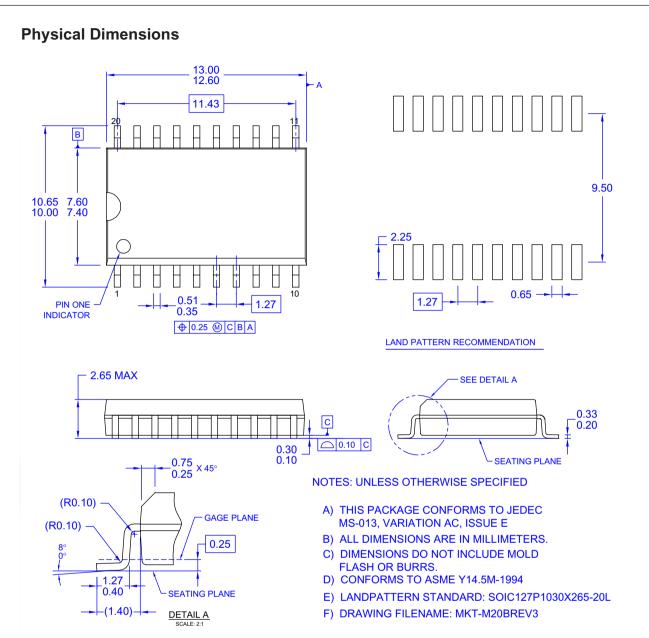
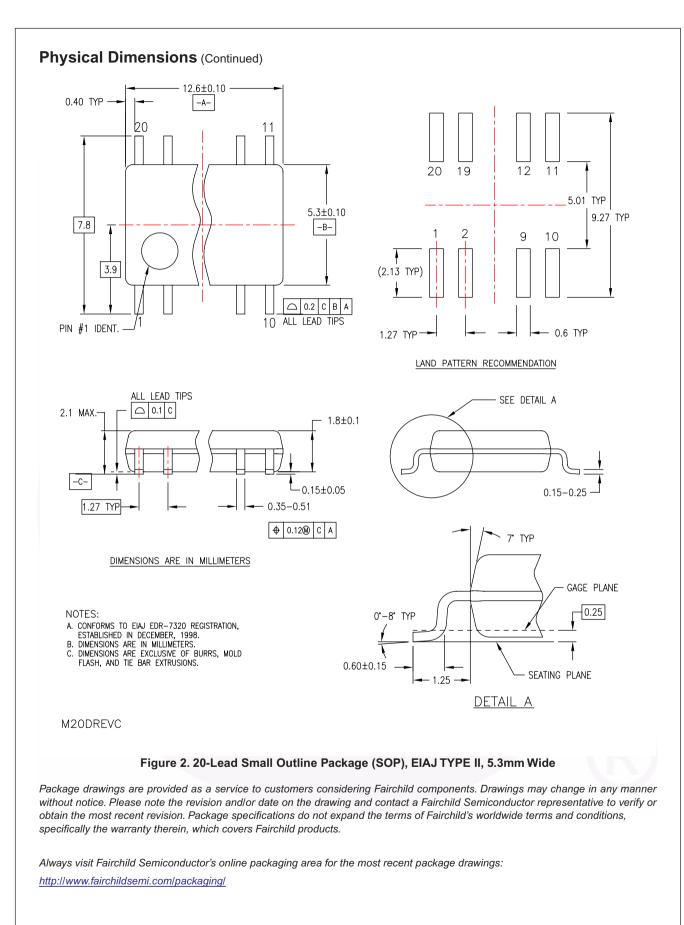


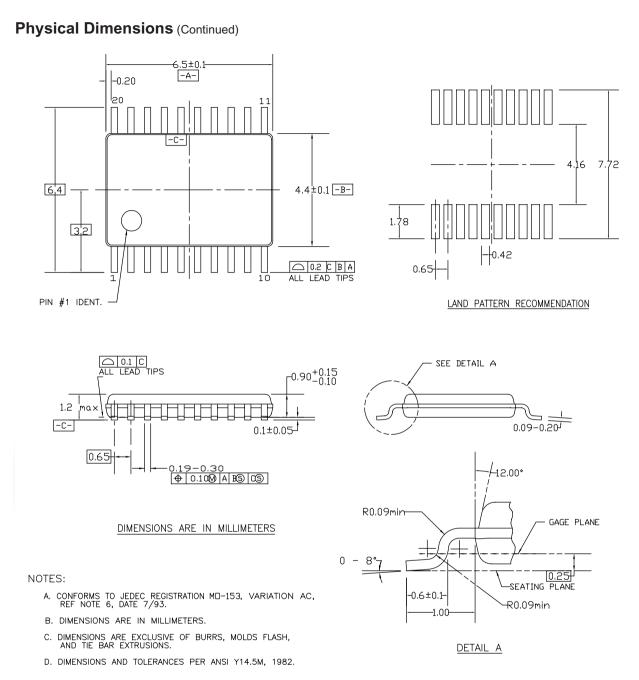
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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74AC240, 74ACT240 — Octal Buffer/Line Driver with 3-STATE Outputs

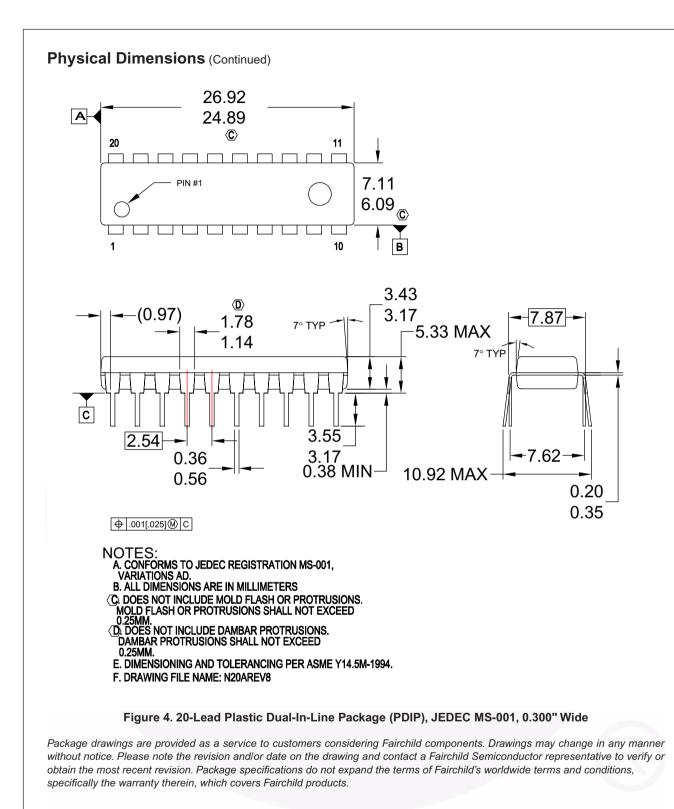
MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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