

TRS3232 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver

With ± 15 -kV ESD Protection

1 Features

- RS-232 Bus-Terminal ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU V.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 250 kbps
- Two Drivers and Two Receivers
- Low Supply Current: 300- μ A Typical
- External Capacitors: 4 \times 0.1 μ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Terminal-Compatible Devices (1 Mbps)
 - SN65C3232 (-40°C to 85°C)
 - SN75C3232 (0°C to 70°C)

2 Applications

- Battery-Powered Systems
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

3 Description

The TRS3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection terminal-to-terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. The devices operate at data-signaling rates up to 250 kbps and a maximum of 30-V/ μ s driver-output slew rate.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|----------------|---------------------------|
| TRS3232 | SOIC (16) | 9.90 mm \times 3.91 mm |
| | SSOP (16) | 6.20 mm \times 5.30 mm |
| | SOIC-Wide (16) | 10.30 mm \times 7.50 mm |
| | TSSOP (16) | 5.00 mm \times 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

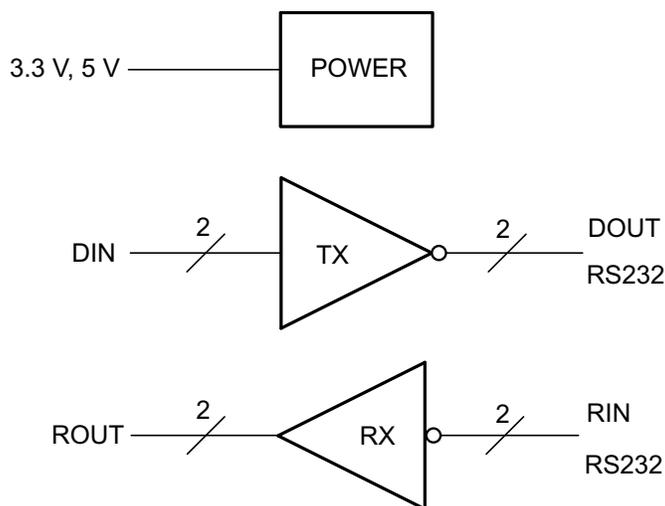


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4 Revision History

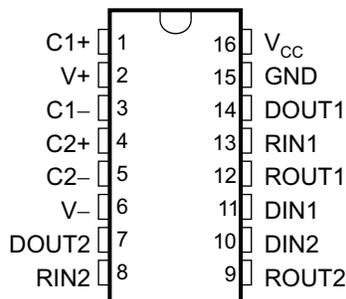
Changes from Original (July 2007) to Revision A

Page

- Changed *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Detailed Description* section, *Power Supply Recommendations* and *Layout* sections, *Device and Documentation Support* and *Mechanical, Packaging, and Orderable Information*
- Deleted *Ordering Information* table.

5 Pin Configuration and Functions

D, DB, DW, PW Packages
16-Pin SOIC, SSOP, SOIC (Wide), TSSOP
Top View



Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----------------|-----|------|---|
| NAME | NO. | | |
| C1+ | 1 | — | Positive lead of C1 capacitor |
| C1- | 3 | — | Negative lead of C1 capacitor |
| C2+ | 4 | — | Positive lead of C2 capacitor |
| C2- | 5 | — | Negative lead of C2 capacitor |
| DIN1 | 11 | I | Logic data input (from UART) |
| DIN2 | 10 | I | Logic data input (from UART) |
| DOUT1 | 14 | O | RS232 line data output (to remote RS232 system) |
| DOUT2 | 7 | O | RS232 line data output (to remote RS232 system) |
| GND | 15 | — | Ground |
| RIN1 | 13 | I | RS232 line data input (from remote RS232 system) |
| RIN2 | 8 | I | RS232 line data input (from remote RS232 system) |
| ROUT1 | 12 | O | Logic data output (to UART) |
| ROUT2 | 9 | O | Logic data output (to UART) |
| V+ | 2 | O | Positive charge pump output for storage capacitor only |
| V- | 6 | O | Negative charge pump output for storage capacitor only |
| V _{CC} | 16 | — | Supply Voltage, Connect to external 3-V to 5.5-V power supply |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|---------------------------------|---|-----------|-------|-----------------------|---|
| V _{CC} | Supply voltage ⁽²⁾ | -0.3 | 6 | V | |
| V ₊ | Positive output supply voltage ⁽²⁾ | -0.3 | 7 | V | |
| V ₋ | Negative output supply voltage ⁽²⁾ | -7 | 0.3 | V | |
| V ₊ – V ₋ | Supply voltage difference ⁽²⁾ | | 13 | V | |
| V _I | Input voltage | Drivers | -0.3 | 6 | V |
| | | Receivers | -25 | 25 | |
| V _O | Output voltage | Drivers | -13.2 | 13.2 | V |
| | | Receivers | -0.3 | V _{CC} + 0.3 | |
| T _J | Operating virtual junction temperature | | 150 | °C | |
| T _{stg} | Storage temperature | -65 | 150 | °C | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|--------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN, DOUT, and GND pins ⁽¹⁾ | ±15000 |
| | | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins ⁽¹⁾ | ±3000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see [Figure 6](#))⁽¹⁾

| | | MIN | NOM | MAX | UNIT | |
|-----------------|---------------------------------|-------------------------|-------------------------|-----|------|----|
| V _{CC} | Supply voltage | V _{CC} = 3.3 V | 3 | 3.3 | 3.6 | V |
| | | V _{CC} = 5 V | 4.5 | 5 | 5.5 | |
| V _{IH} | Driver high-level input voltage | DIN | V _{CC} = 3.3 V | 2 | | V |
| | | | V _{CC} = 5 V | 2.4 | | |
| V _{IL} | Driver low-level input voltage | DIN | | | 0.8 | V |
| V _I | Driver input voltage | DIN | | 0 | 5.5 | V |
| | Receiver input voltage | RIN | | -25 | 25 | |
| T _A | Operating free-air temperature | TRS3232C | | 0 | 70 | °C |
| | | TRS3232I | | -40 | 85 | |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | TRS3232 | | | | UNIT |
|---|-------------|--------------|-------------------|---------------|------|
| | D (SOIC) | DB (SSOP) | DW (SOIC-wide) | PW (TSSOP) | |
| | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 73 | 82 | 57 | 108 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics—Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see Figure 6)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--------------------------------|---|-----|--------------------|-----|------|
| I _{CC} Supply current | No load, V _{CC} = 3.3 V to 5 V | | 0.3 | 1 | mA |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.6 Electrical Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see Figure 6)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|---|--|-----|--------------------|-----|------|
| V _{OH} High-level output voltage | D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = GND | 5 | 5.4 | | V |
| V _{OL} Low-level output voltage | D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = V _{CC} | –5 | –5.4 | | V |
| I _{IH} High-level input current | V _I = V _{CC} | | ±0.01 | ±1 | μA |
| I _{IL} Low-level input current | V _I at GND | | ±0.01 | ±1 | μA |
| I _{OS} ⁽³⁾ Short-circuit output current | V _{CC} = 3.6 V V _O = 0 V V _{CC} = 5.5 V V _O = 0 V | | ±35 | ±60 | mA |
| r _O Output resistance | V _{CC} = 0 V, V ₊ = 0 V, and V _– = 0 V V _O = ±2 V | 300 | 10M | | Ω |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see Figure 6)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--|--|-----------------------|-----------------------|------------|------|
| V _{OH} High-level output voltage | I _{OH} = –1 mA | V _{CC} – 0.6 | V _{CC} – 0.1 | | V |
| V _{OL} Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{IT+} Positive-going input threshold voltage | V _{CC} = 3.3 V V _{CC} = 5 V | | 1.5 1.8 | 2.4 2.4 | V |
| V _{IT–} Negative-going input threshold voltage | V _{CC} = 3.3 V V _{CC} = 5 V | 0.6 0.8 | 1.2 1.5 | | V |
| V _{hys} Input hysteresis (V _{IT+} – V _{IT–}) | | | 0.3 | | V |
| r _I Input resistance | V _I = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Switching Characteristics

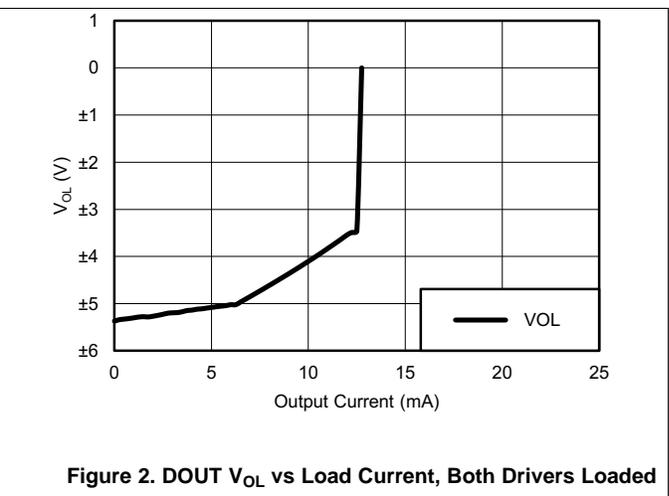
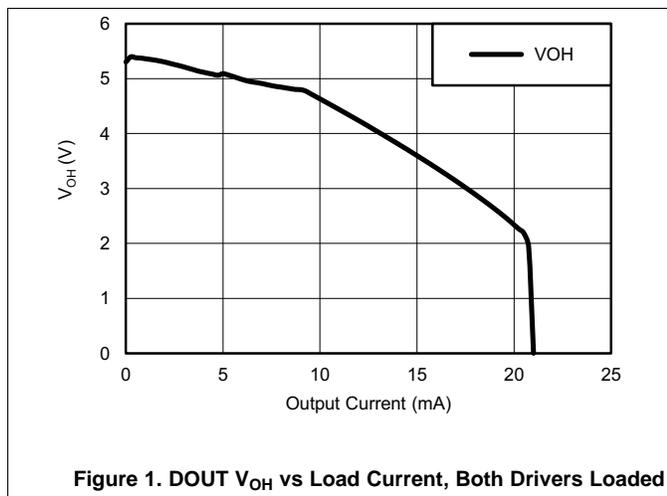
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see Figure 6)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-------------------|---|---|---|-----|--------------------|-----|------------|
| Maximum data rate | | $R_L = 3\text{ k}\Omega$, One D _{OUT} switching, | $C_L = 1000\text{ pF}$ See Figure 3 | 150 | 250 | | kbps |
| $t_{sk(p)}$ | Driver Pulse skew ⁽³⁾ | $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, | $C_L = 150$ to 2500 pF See Figure 4 | | 300 | | ns |
| SR(tr) | Driver Slew rate, transition region (see Figure 3) | $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $V_{CC} = 5\text{ V}$ | $C_L = 150$ to 1000 pF | 6 | | 30 | V/ μ s |
| | | | $C_L = 150$ to 2500 pF | 4 | | 30 | |
| t_{PLH} | Receiver Propagation delay time, low- to high-level output | $C_L = 150\text{ pF}$ | | | 300 | | ns |
| t_{PHL} | Receiver Propagation delay time, high- to low-level output | | | | 300 | | ns |
| $t_{sk(p)}$ | Receiver Pulse skew ⁽¹⁾ | | | | 300 | | ns |

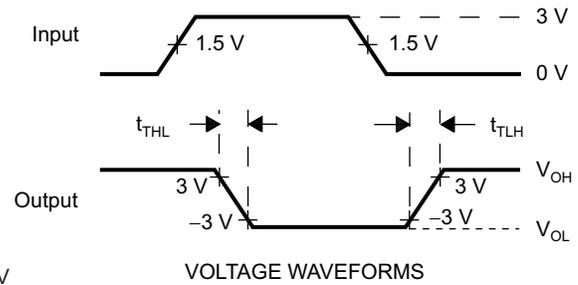
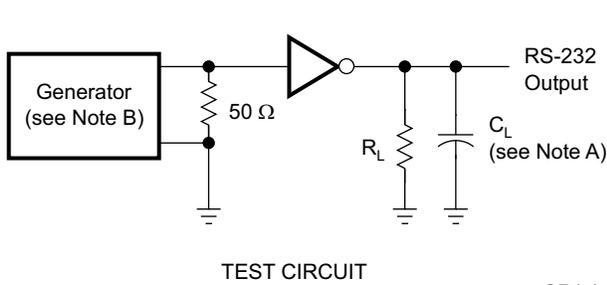
- (1) Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.
- (2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.
- (3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.9 Typical Characteristics

$V_{CC} = 3.3\text{ V}$



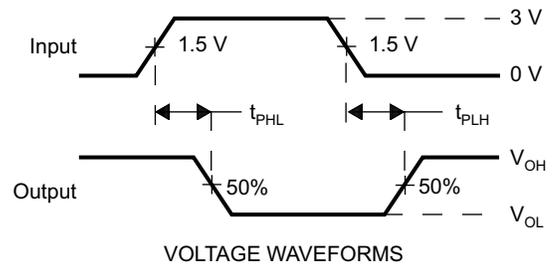
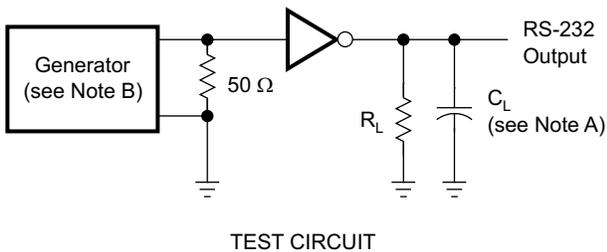
7 Parameter Measurement Information



$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

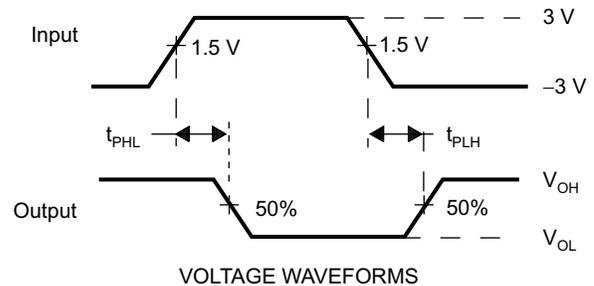
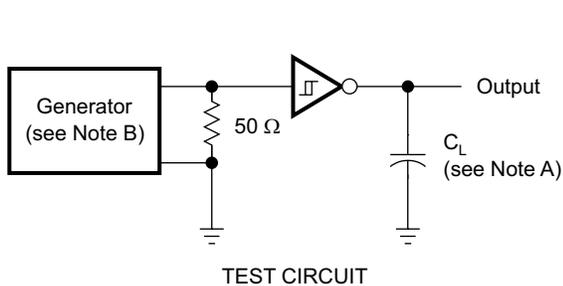
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 4. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

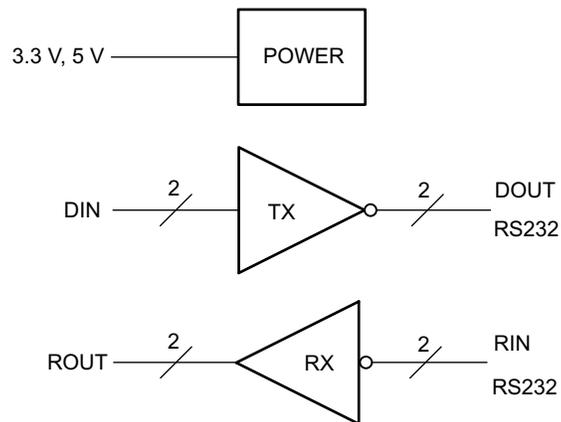
Figure 5. Receiver Propagation Delay Times

8 Detailed Description

8.1 Overview

The TRS3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbps and a maximum of 30-V/ μ s driver output slew rate. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V_+ and V_- pins using a charge pump that requires four external capacitors.

8.3.2 RS232 Driver

Two drivers interface the standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.4 Device Functional Modes

Table 1. Each Driver⁽¹⁾

| INPUT DIN | OUTPUT DOUT |
|--------------|----------------|
| L | H |
| H | L |

(1) H = high level, L = low level

Table 2. Each Receiver⁽¹⁾

| INPUT RIN | OUTPUT ROUT |
|--------------|----------------|
| L | H |
| H | L |
| Open | H |

(1) H = high level, L = low level,
Open = input disconnected or
connected driver off

8.4.1 V_{CC} Powered by 3 V to 5.5 V

The device is in normal operation.

8.4.2 V_{CC} Unpowered, $V_{CC} = 0$ V

When the TRS3232 device is unpowered, it can be safely connected to an active remote RS232 device.

9 Application and Implementation

NOTE

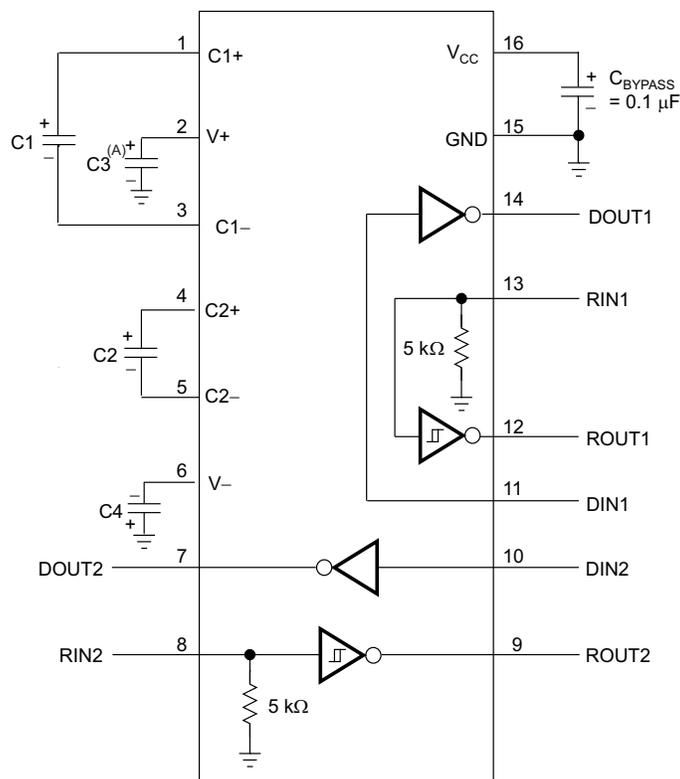
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TRS3232 device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa.

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector.

9.2 Typical Application



- C3 can be connected to V_{CC} or GND.
- Resistor values shown are nominal.
- Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.
- See [Table 3](#) for capacitor values.

Figure 6. Typical Operating Circuit

Typical Application (continued)

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V
 - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbps

Table 3. V_{CC} versus Capacitor Values

| V_{CC} | C1 | C2, C3, C4 |
|-------------------|---------------|--------------|
| 3.3 V \pm 0.3 V | 0.1 μ F | 0.1 μ F |
| 5 V \pm 0.5 V | 0.047 μ F | 0.33 μ F |
| 3 V to 5.5 V | 0.1 μ F | 0.47 μ F |

9.2.2 Detailed Design Procedure

For proper operation, add capacitors as shown in [Figure 6](#) and [Table 3](#).

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

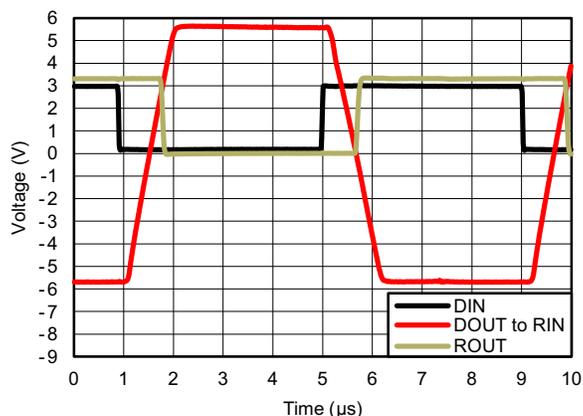


Figure 7. 250 kbps Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3 V

10 Power Supply Recommendations

V_{CC} must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using [Table 3](#).

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

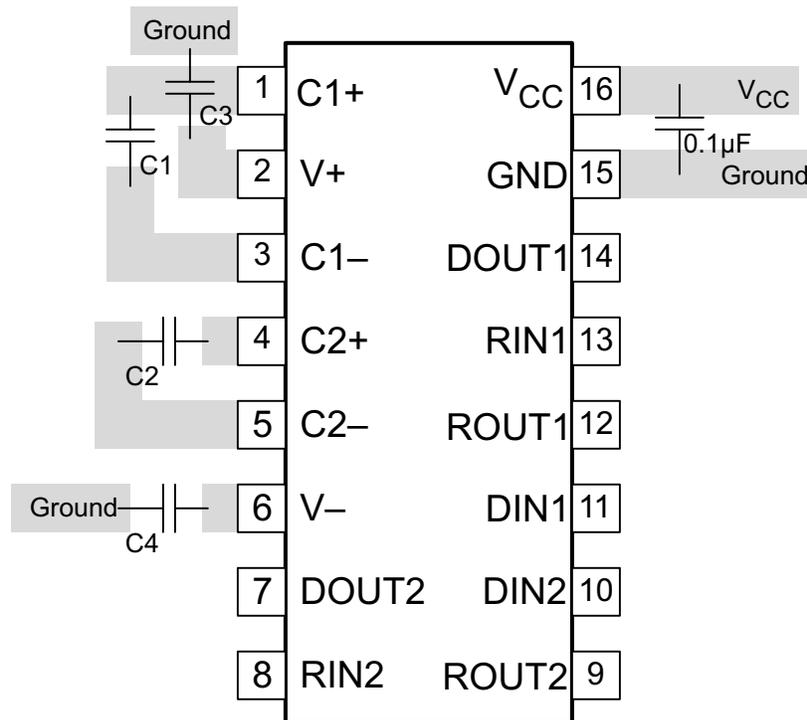


Figure 8. Layout Diagram

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TRS3232CDBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RS32C | Samples |
| TRS3232CDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TRS3232C | Samples |
| TRS3232CDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TRS3232C | Samples |
| TRS3232CPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RS32C | Samples |
| TRS3232IDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRS3232I | Samples |
| TRS3232IPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RS32I | Samples |
| TRS3232IPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RS32I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

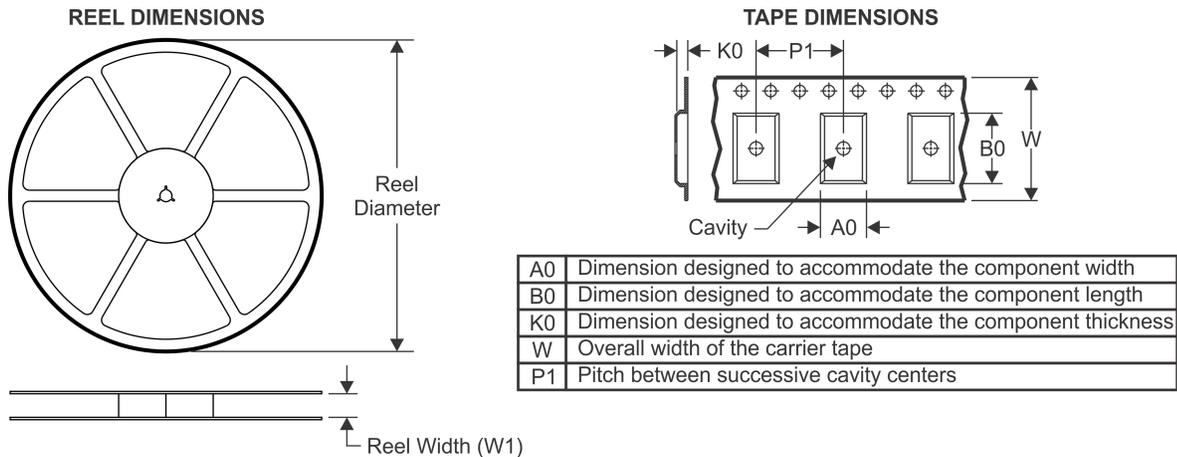
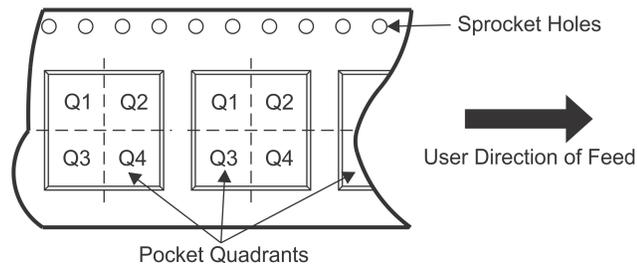
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

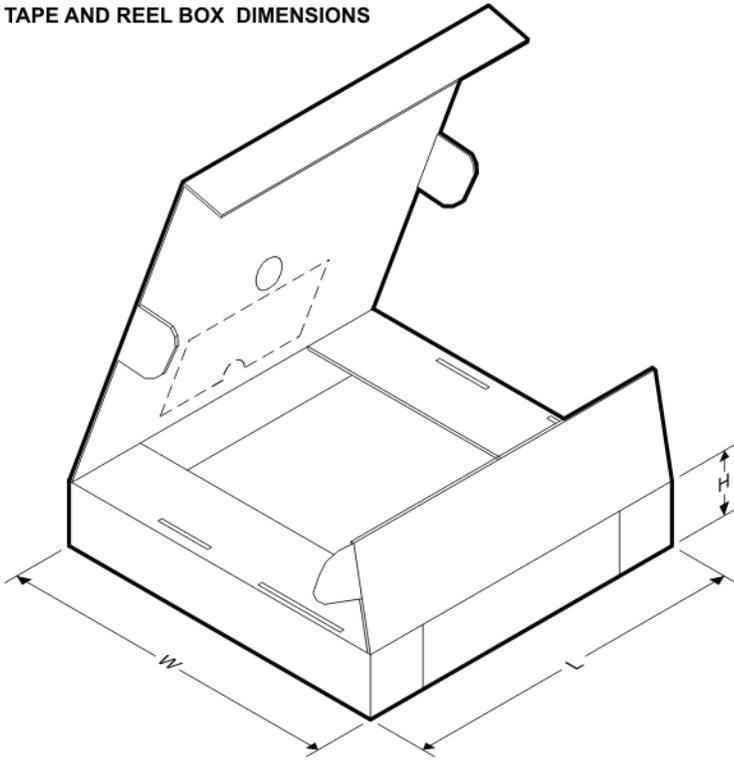
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRS3232CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TRS3232CDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| TRS3232IDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TRS3232IPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

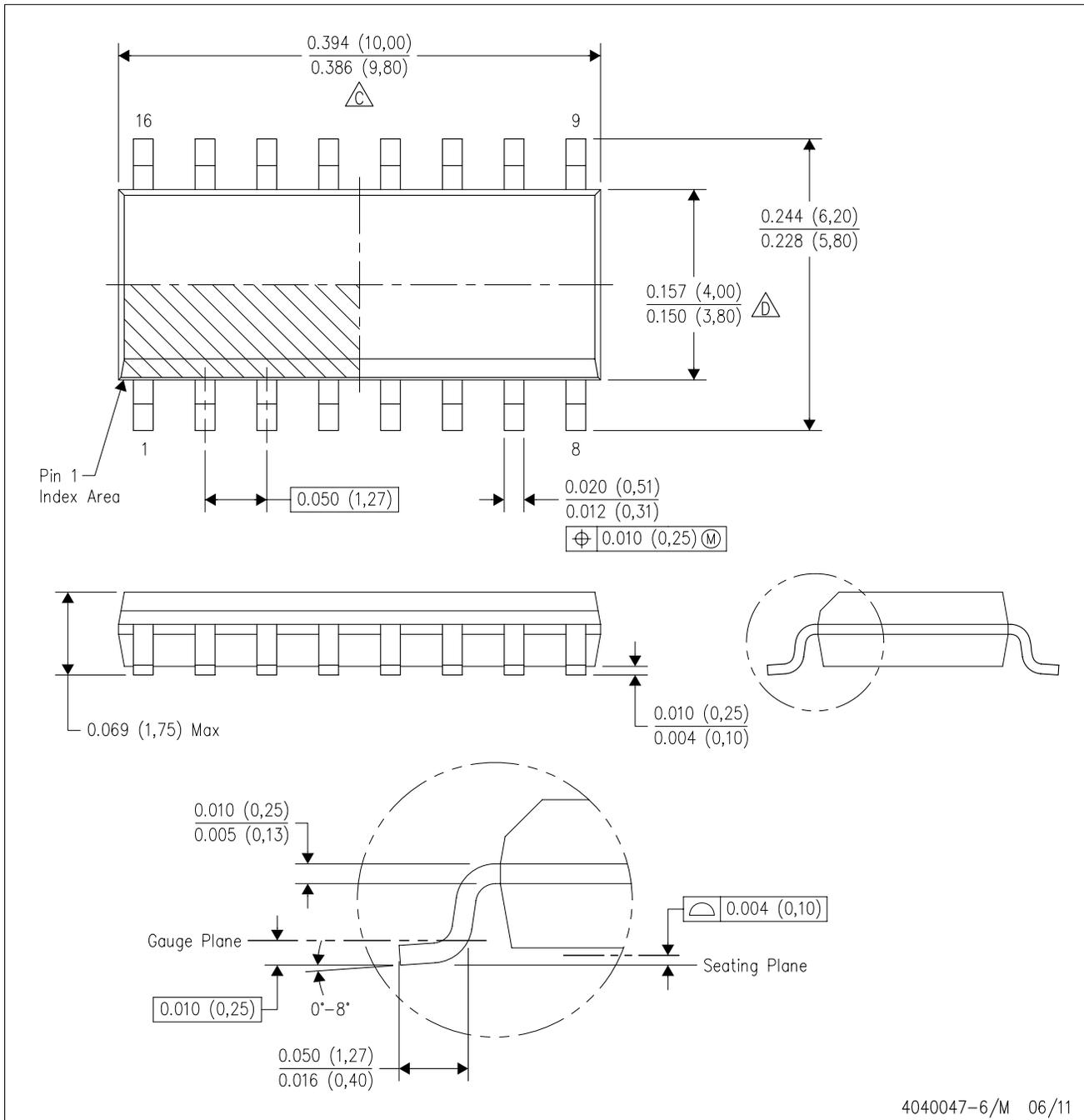
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRS3232CDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| TRS3232CDWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| TRS3232IDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| TRS3232IPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G16)

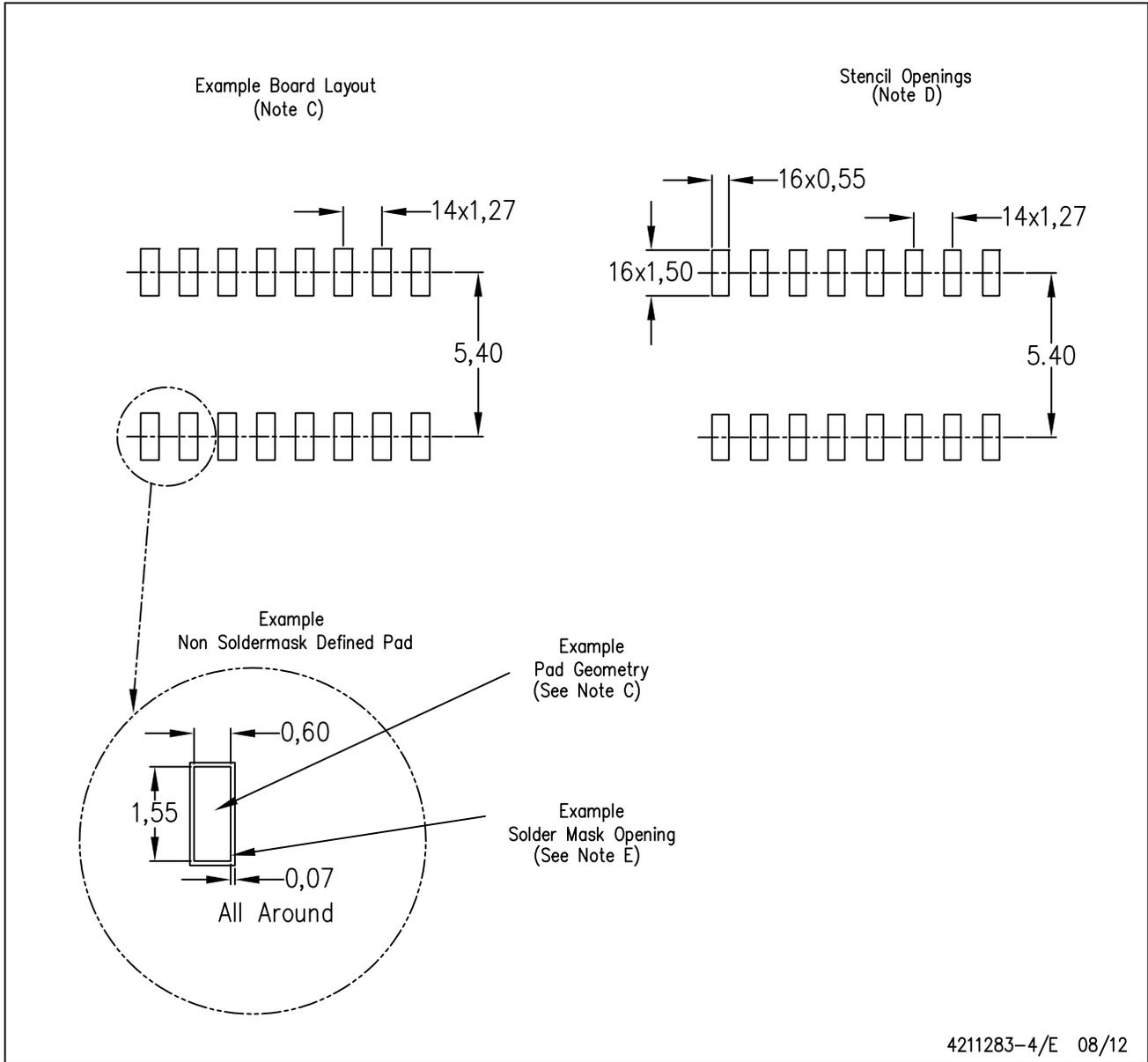
PLASTIC SMALL OUTLINE



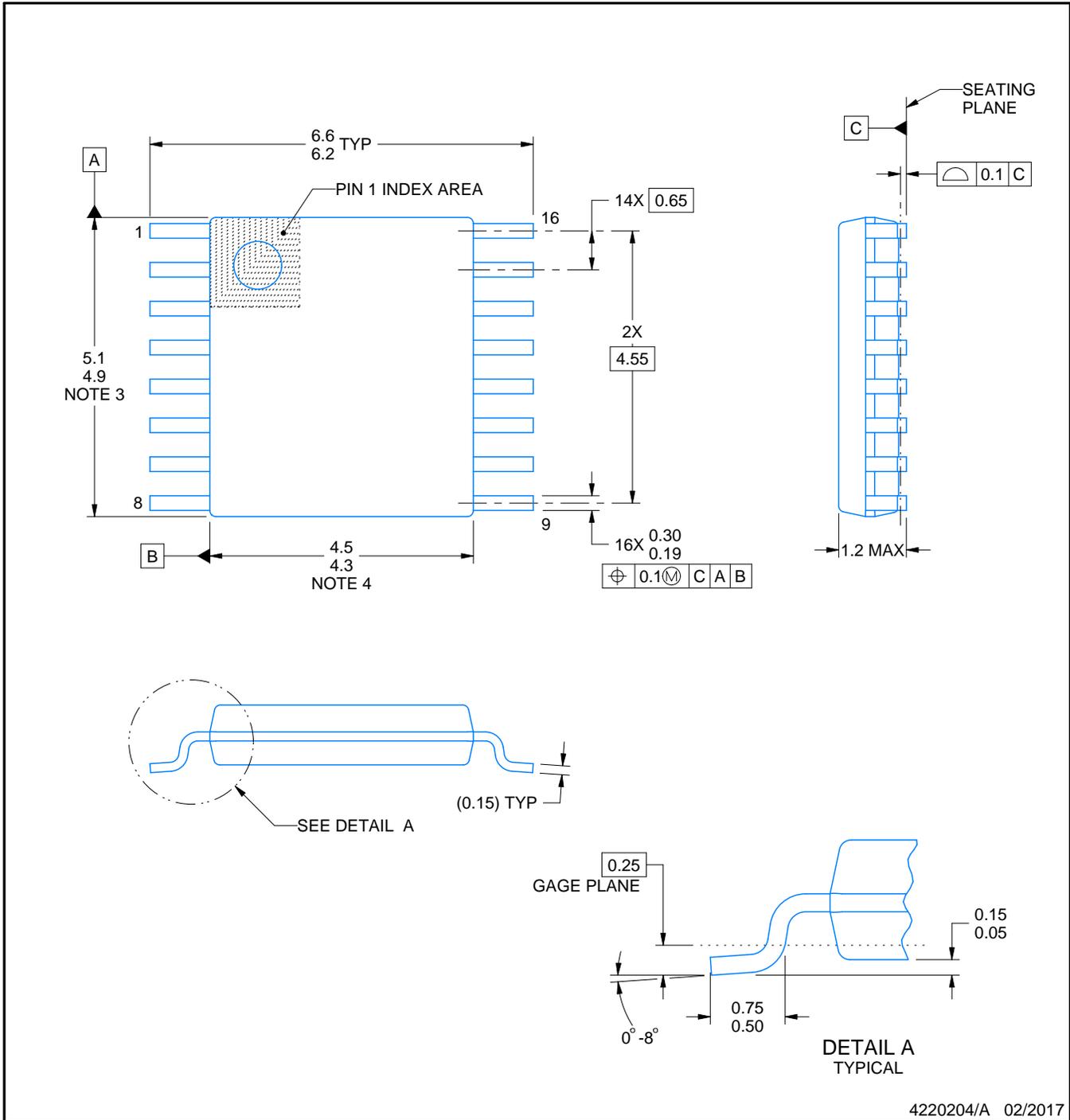
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

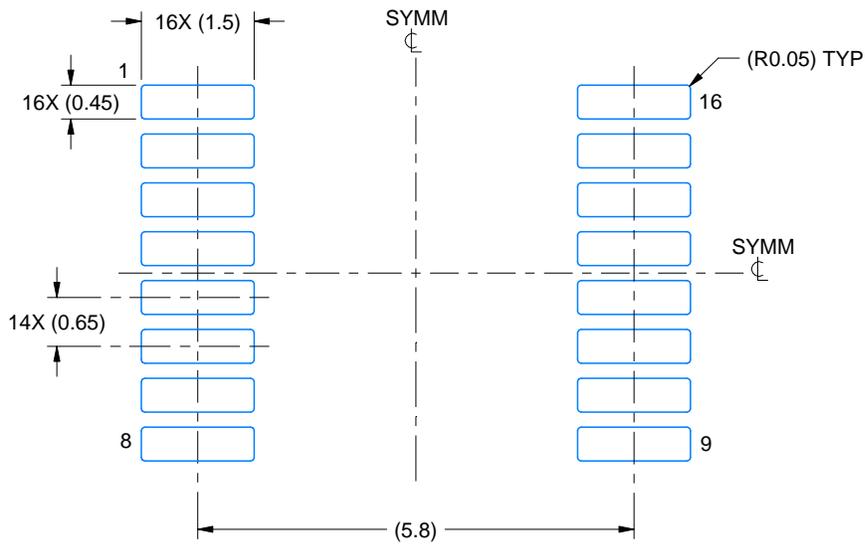
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

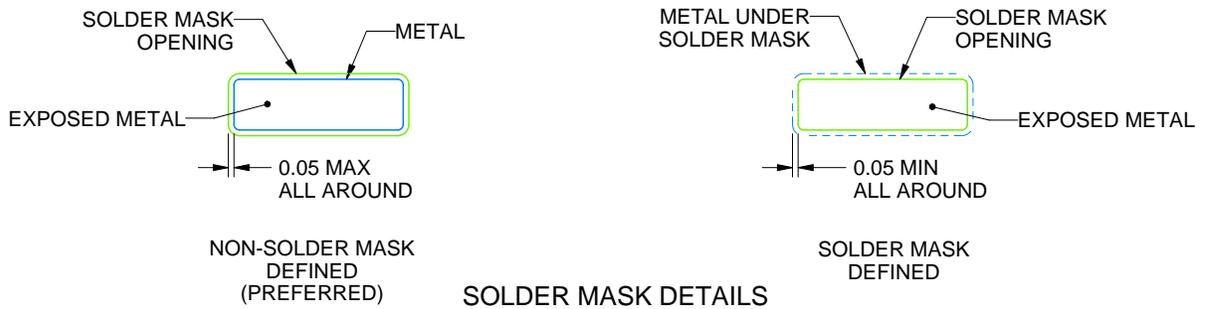
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

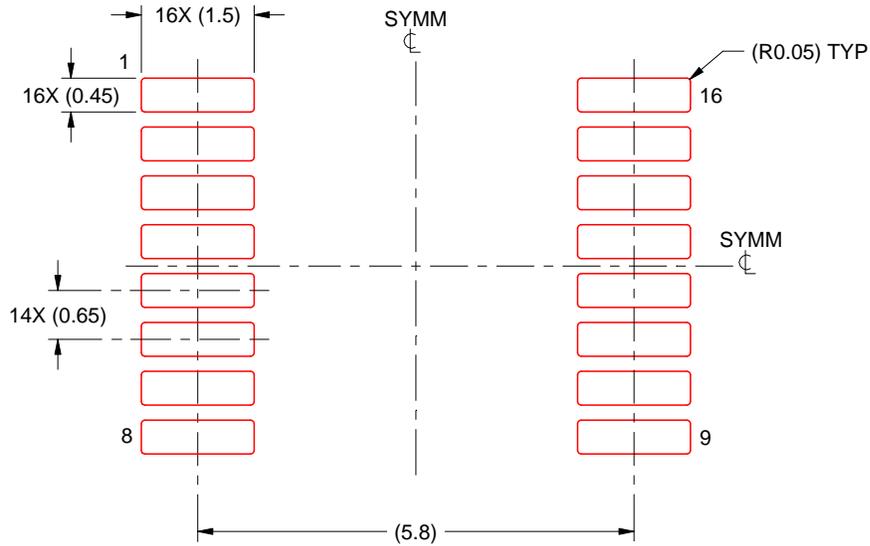
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

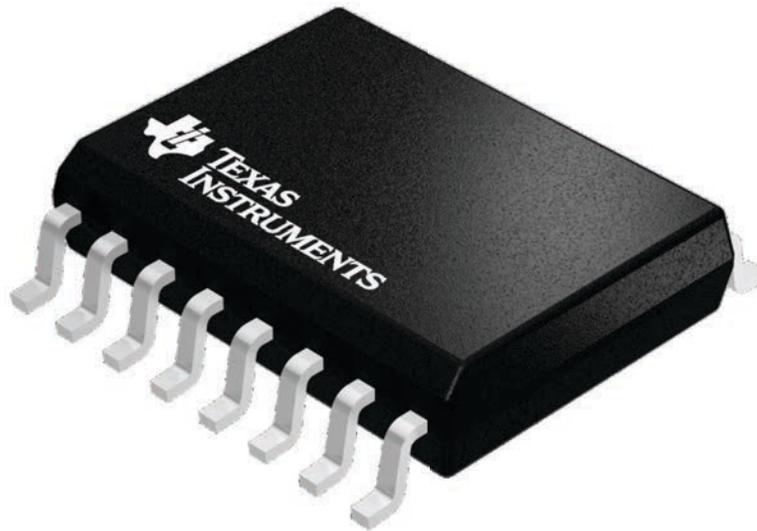
DW 16

SOIC - 2.65 mm max height

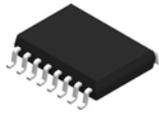
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



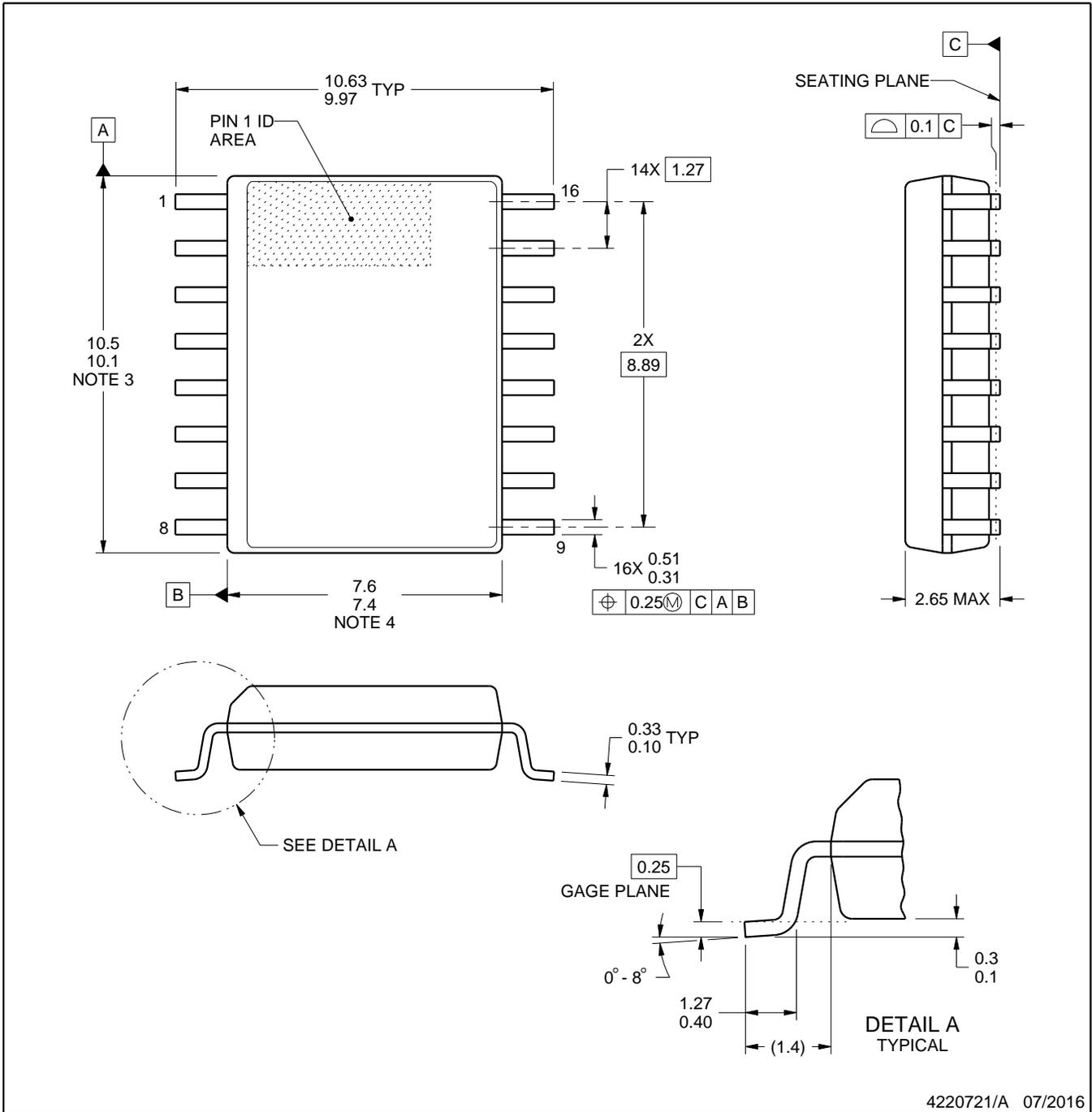
4224780/A



DW0016A

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



NOTES:

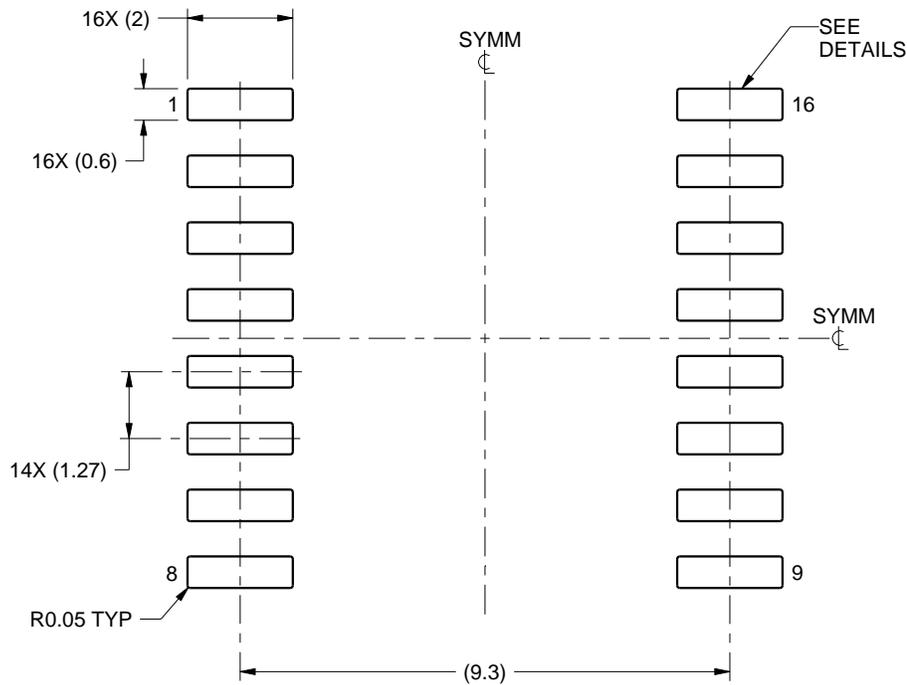
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

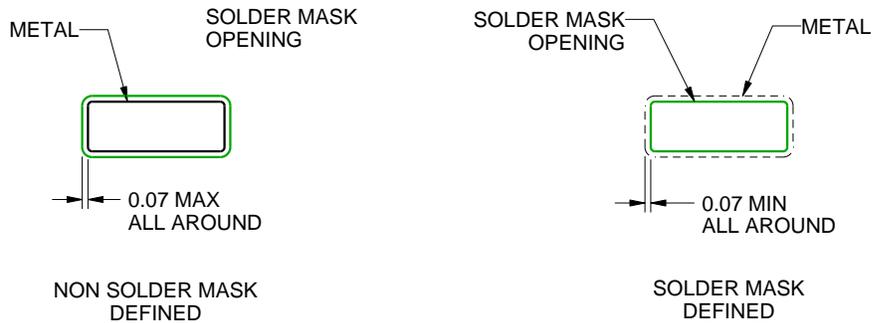
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

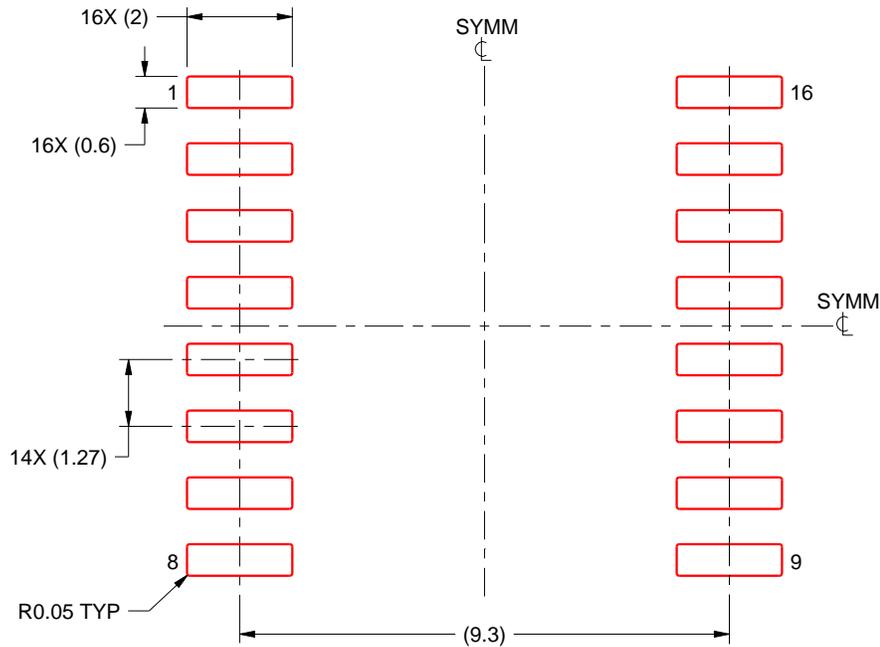
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

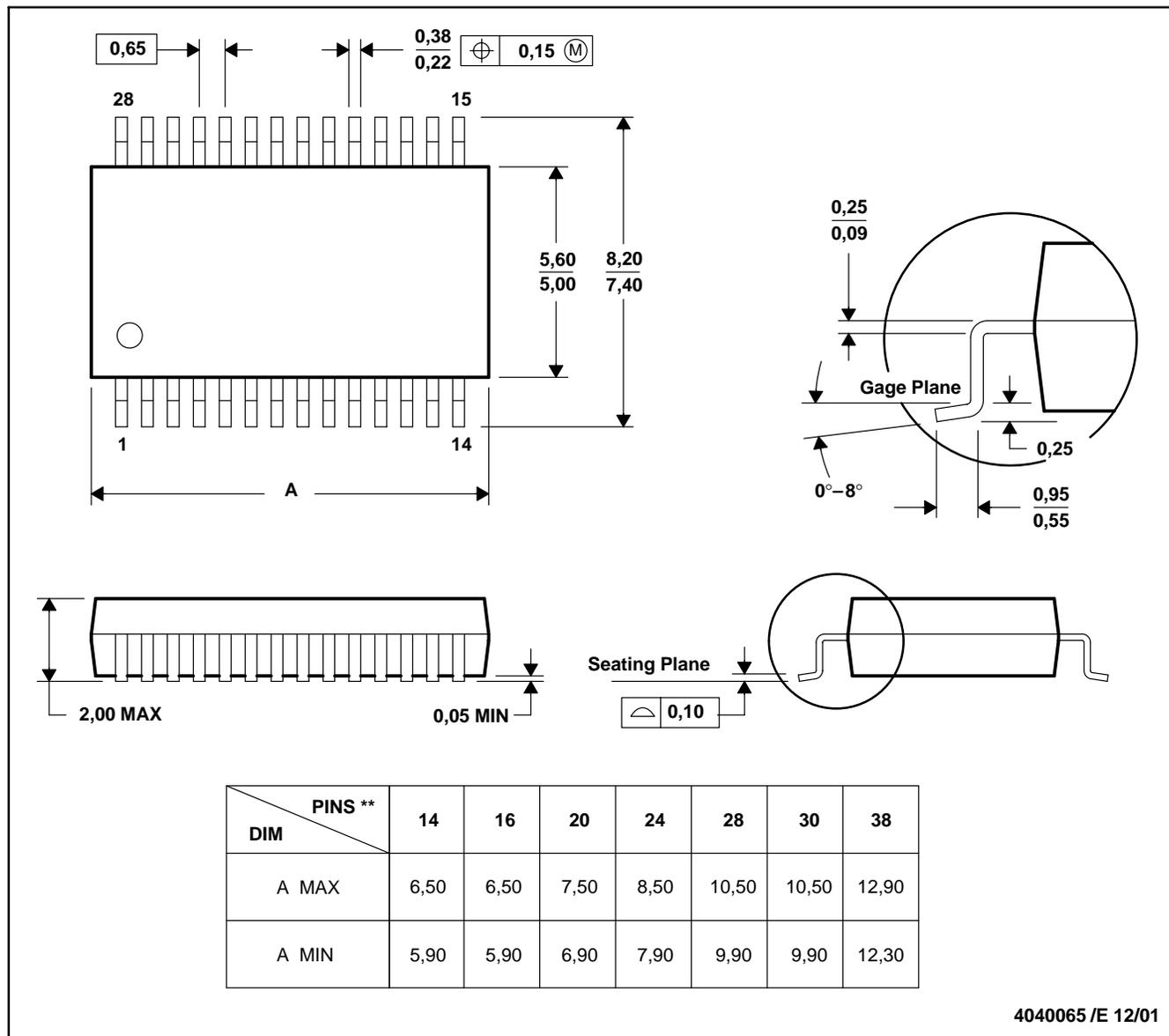
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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