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December 2014

FDZ197PZ

P-Channel 1.5 V Specified PowerTrench $^{(\!R\!)}$ Thin WL-CSP MOSFET -20 V, -3.8 A, 64 m Ω

Features

- Max $r_{DS(on)} = 64 \text{ m}\Omega$ at $V_{GS} = -4.5 \text{ V}$, $I_D = -2.0 \text{ A}$
- Max $r_{DS(on)} = 71 \text{ m}\Omega$ at $V_{GS} = -2.5 \text{ V}$, $I_D = -2.0 \text{ A}$
- Max $r_{DS(on)}$ = 79 m Ω at V_{GS} = -1.8 V, I_D = -1.0 A
- Max $r_{DS(on)}$ = 95 m Ω at V_{GS} = -1.5 V, I_D = -1.0 A
- Occupies only 1.5 mm² of PCB area.Less than 50% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.65 mm height when mounted to PCR
- HBM ESD protection level > 4400V (Note3)
- RoHS Compliant

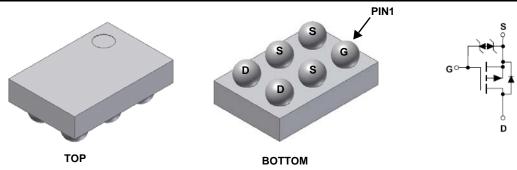


General Description

Designed on Fairchild's advanced 1.5 V PowerTrench® process with state of the art "fine pitch" WLCSP packaging process, the FDZ197PZ minimizes both PCB space and $r_{\text{DS(on)}}.$ This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{\text{DS(on)}}.$

Applications

- Battery management
- Load switch
- Battery protection



WL-CSP 1x1.5 Thin

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Param	neter		Ratings	Units
V_{DS}	Drain to Source Voltage			-20	V
V_{GS}	Gate to Source Voltage			±8	V
1	-Continuous	T _A = 25°C	(Note 1a)	-3.8	^
I _D	-Pulsed			-15	— A
D	Power Dissipation	T _A = 25°C	(Note 1a)	1.9	10/
P_{D}	Power Dissipation	$T_A = 25$ °C	(Note 1b)	0.9	W
T _J , T _{STG}	Operating and Storage Junction Temper	ature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	133	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
7	FDZ197PZ	WL-CSP 1x1.5 Thin	7 "	8 mm	5000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-10		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V			-1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.4	-0.5	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		2.7		mV/°C
		$V_{GS} = -4.5 \text{ V}, I_D = -2.0 \text{ A}$		46	64	
		$V_{GS} = -2.5 \text{ V}, I_D = -2.0 \text{ A}$		53	71	
roo()	Static Drain to Source On Resistance	$V_{GS} = -1.8 \text{ V}, I_D = -1.0 \text{ A}$	59	79	mΩ	
r _{DS(on)}	Static Brain to Godice On Resistance	$V_{GS} = -1.5 \text{ V}, I_D = -1.0 \text{ A}$		68	95	11152
		$V_{GS} = -4.5 \text{ V}, I_D = -2.0 \text{ A},$ $T_J = 125 ^{\circ}\text{C}$		54	84	
9 _{FS}	Forward Transconductance	V _{DD} = -5 V, I _D = -3.8 A		21		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 40 V V 0 V	1180	1570	pF
C _{oss}	Output Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	190	255	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	160	225	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			5.8	12	ns
t _r	Rise Time	$V_{DD} = -10 \text{ V}, I_{D} = -3.8 \text{ A},$		5.9	12	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		311	498	ns
t _f	Fall Time			280	448	ns
Q_{g}	Total Gate Charge	$V_{GS} = 0V \text{ to } -4.5V$ $V_{DD} = -10 \text{ V}$		18	25	nC
Q_{gs}	Gate to Source Charge	V _{DD} = -10 V I _D = -3.8 A	1	1.5		nC
Q_{gd}	Gate to Drain "Miller" Charge	ID = -3.0 A		4.7		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -1.1 \text{ A}$ (Note 2)		-0.6	-1.2	V
t _{rr}	Reverse Recovery Time	F = -3.8 A, di/dt = 100 A/μs		194	310	ns
Q_{rr}	Reverse Recovery Charge			344	550	nC

^{1.} $R_{\theta,IA}$ is determined with the device mounted on a 1 in 2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta,IC}$ is guaranteed by design while $R_{\theta,CA}$ is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 133 °C/W when mounted on a minimum pad of 2 oz copper.

^{2.} Pulse Test: Pulse Width < $300\mu\text{s},$ Duty cycle < 2.0%.

^{3.} The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

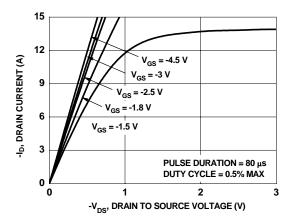


Figure 1. On-Region Characteristics

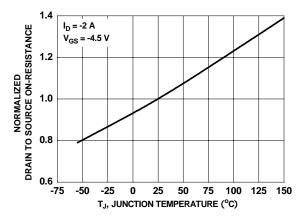


Figure 3. Normalized On-Resistance vs Junction Temperature

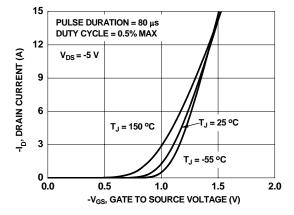


Figure 5. Transfer Characteristics

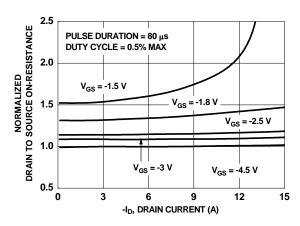


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

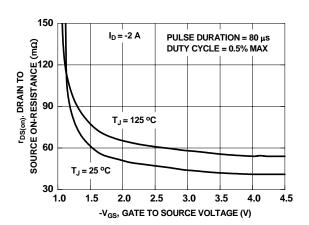


Figure 4. On-Resistance vs Gate to Source Voltage

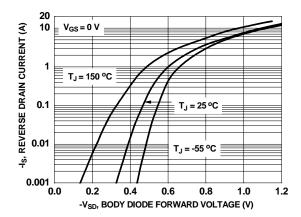


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

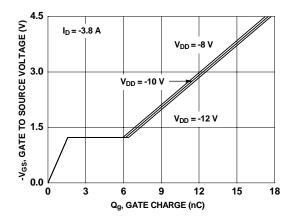


Figure 7. Gate Charge Characteristics

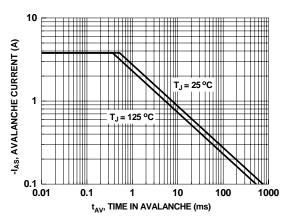


Figure 9. Unclamped Inductive Switching Capability

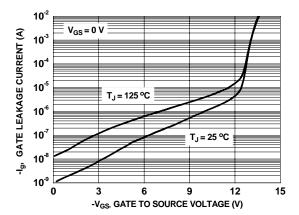


Figure 11. Gate Leakage Current vs Gate to Source Voltage

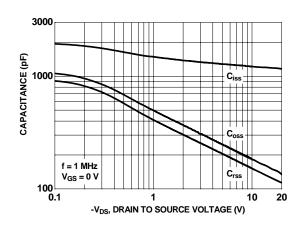


Figure 8. Capacitance vs Drain to Source Voltage

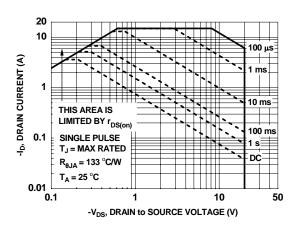


Figure 10. Forward Bias Safe Operating Area

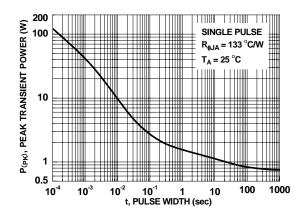


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

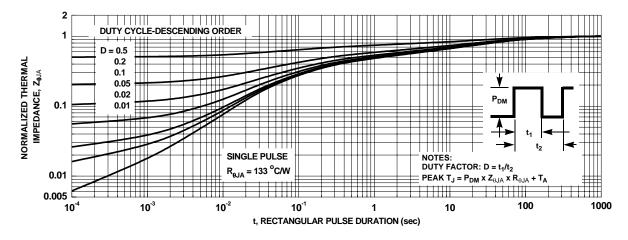
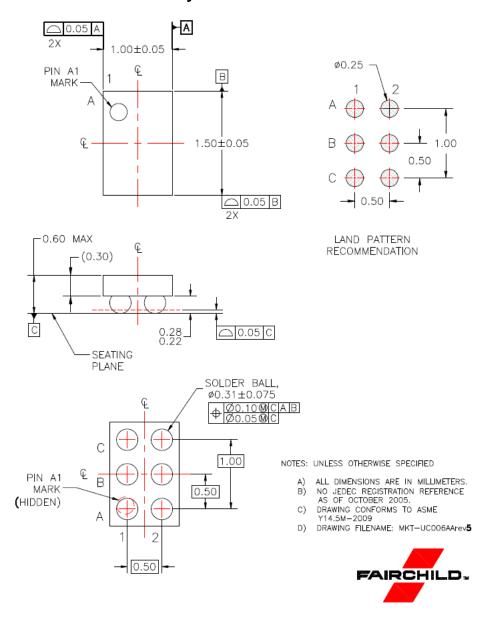


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



Pin Definations:

Gate	Drain	Source
A1	C1, C2	A2, B1, B2

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