Si5327

Any-Frequency Precision Clock Multiplier/Jitter Attenuator

Features

- Generates any frequency from 2 kHz to 808 MHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 0.5 ps rms (12 kHz–20 MHz)
- Integrated loop filter with selectable loop bandwidth (4 to 525 Hz)
- Meets OC-192 GR-253-CORE jitter specifications
- Dual clock inputs with manually controlled hitless switching
- Free run and VCO freeze modes
- Support for ITU G.709 and custom FEC ratios (255/238, 255/237, 255/236)
- LOL and LOS alarm outputs
- I^2C or SPI programmable
- Single 1.8, 2.5, 3.3 V supply
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

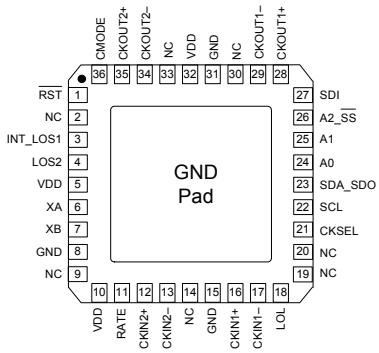
Ordering Information:

See page 54.

Applications

- Dual clock outputs with programmable signal format (LVPECL, LVDS, CML, CMOS)
- SONET/SDH OC-48/OC-192/STM-16/STM-64 line cards
- ITU G.709 and custom FEC line cards
- GbE/10GbE, 1/2/4/8/10G Fibre Channel line cards
- Synchronous Ethernet
- Optical modules
- Wireless repeaters/ wireless backhaul
- Data converter clocking
- xDSL
- PDH clock synthesis
- Test and measurement
- Broadcast video

Pin Assignments



Description

The Si5327 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5327 accepts two input clocks ranging from 2 kHz to 710 MHz and generates two output clocks ranging from 2 kHz to 808 MHz. The two outputs are divided down separately from a common source. The Si5327 can also use its crystal oscillator as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. The Si5327 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. The Si5327 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5327 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

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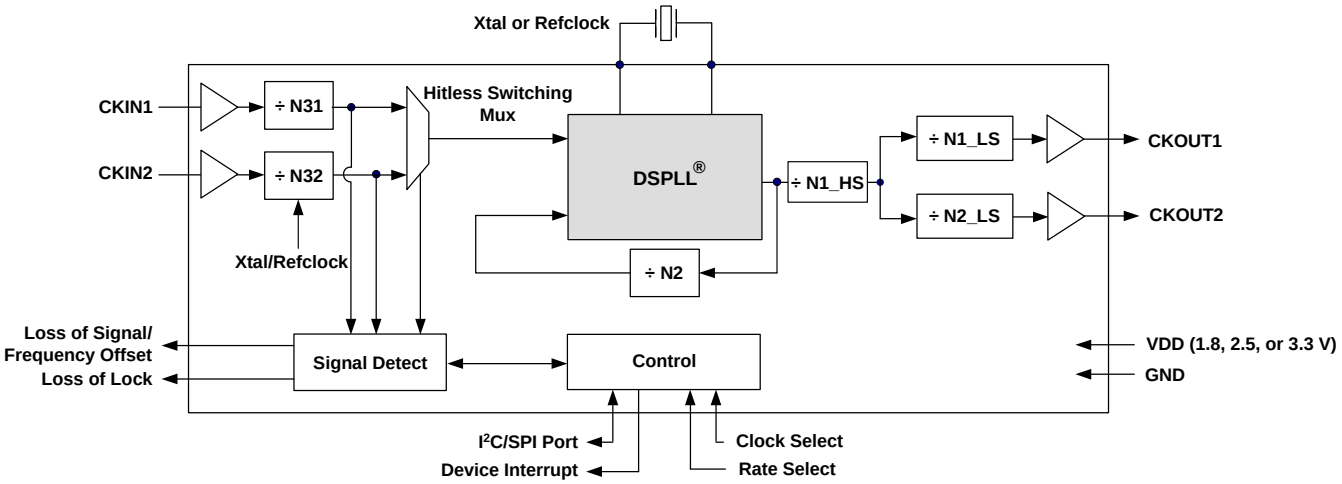
Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	C
Supply Voltage during Normal Operation	V_{DD}	3.3 V Nominal	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 ºC unless otherwise stated.						

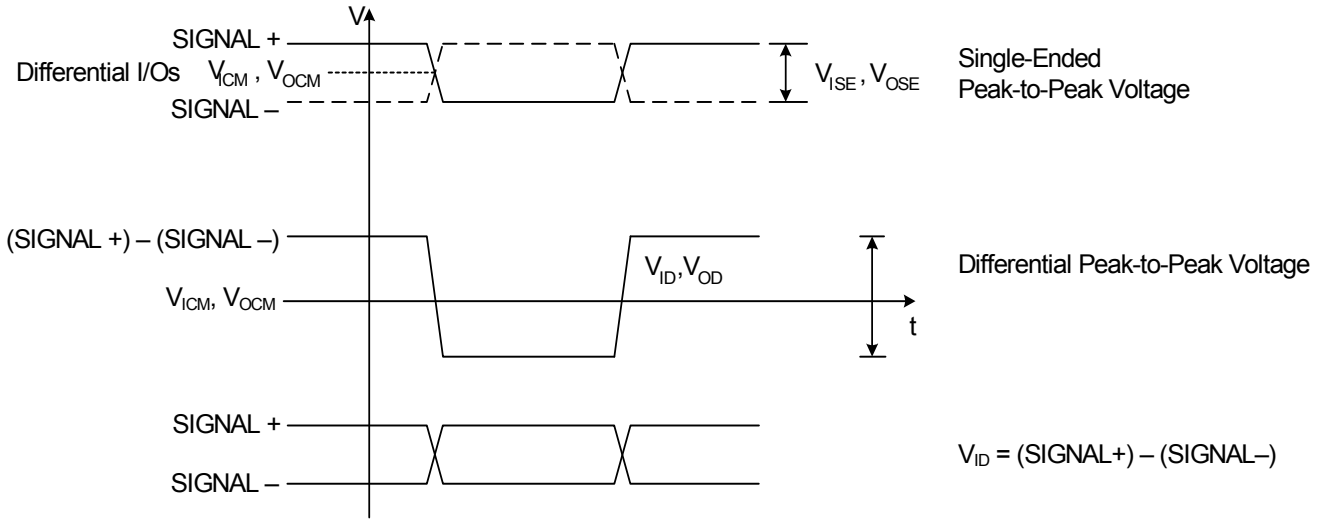


Figure 1. Differential Voltage Characteristics

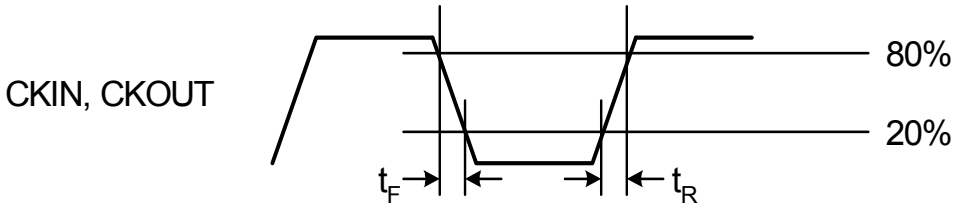


Figure 2. Rise/Fall Time Characteristics

Table 2. DC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1]	I_{DD}	LVPECL Format 622.08 MHz Out Both CKOUTs Enabled	—	251	279	mA
		LVPECL Format 622.08 MHz Out 1 CKOUT Enabled	—	217	243	mA
		CMOS Format 19.44 MHz Out Both CKOUTs Enabled	—	204	234	mA
		CMOS Format 19.44 MHz Out 1 CKOUT Enabled	—	194	220	mA
		Disable Mode	—	165	—	mA
CKINn Input Pins[2]						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ± 5%	0.9	—	1.4	V
		2.5 V ± 10%	1	—	1.7	V
		3.3 V ± 10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		fCKIN > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}

Notes:

1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clocks (CKOUTn)[3,5]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} –1.42	—	V_{DD} –1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD}-0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Drive Current (CMOS driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO_{IO}	ICMOS[1:0] = 11 V_{DD} = 1.8 V	—	7.5	—	mA
		ICMOS[1:0] = 10 V_{DD} = 1.8 V	—	5.5	—	mA
		ICMOS[1:0] = 01 V_{DD} = 1.8 V	—	3.5	—	mA
		ICMOS[1:0] = 00 V_{DD} = 1.8 V	—	1.75	—	mA
		ICMOS[1:0] = 11 V_{DD} = 3.3 V	—	32	—	mA
		ICMOS[1:0] = 10 V_{DD} = 3.3 V	—	24	—	mA
		ICMOS[1:0] = 01 V_{DD} = 3.3 V	—	16	—	mA
		ICMOS[1:0] = 00 V_{DD} = 3.3 V	—	8	—	mA
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3-Level Input Pins[4]						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}	See Note 4	–20	—	—	µA
Input Mid Current	I_{IMM}	See Note 4	–2	—	+2	µA
Input High Current	I_{IHH}	See Note 4	—	—	20	µA
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	IO = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
Output Voltage Low		IO = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	IO = –2 mA V_{DD} = 1.71 V	V_{DD} –0.4	—	—	V
Output Voltage High		IO = –2 mA V_{DD} = 2.97 V	V_{DD} –0.4	—	—	V

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 3. AC Specifications

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Reference Clock Input Pin XA (XB with cap to GND)						
Input Resistance	XA_{RIN}	RATE = M, ac coupled	—	12	—	kΩ
Input Voltage Swing	XA_{VPP}	RATE = M, ac coupled	0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Voltage Swing	XA/XB_{VPP}	RATE = M	0.5	—	2.4	V_{PP}
CKINn Input Pins						
Input Frequency	CKN_F		0.002	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F	N1_HS ≥ 6	0.002	—	808	MHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 1.71 C_{LOAD} = 5 pF	—	—	8	ns

Notes:

1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan. Please visit the Silicon Labs Technical Support web page at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.

Table 3. AC Specifications (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 2.97 C_{LOAD} = 5 pF	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO_{DC}	100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	+/-40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMN}		1	—	—	µs
Reset to Microprocessor Access Ready	t_{READY}		—	—	10	ms
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKINn ↑ to ↓ Internal detection of LOSn N3 ≠ 1	—	—	4.5 x N3	T_{CKIN}
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	↓LOS to ↓LOL Fold = Fnew Stable Xa/XB reference	—	10	—	ms
Device Skew						
Output Clock Skew	t_{SKEW}	↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency and signal format CKOUT_ALWAYS_ON = 1 SQ_ICAL = 1	—	—	100	ps
Phase Change due to Temperature Variation[1]	t_{TEMP}	Max phase changes from –40 to +85 °C	—	300	500	ps

Notes:
1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan. Please visit the Silicon Labs Technical Support web page at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.

Table 3. AC Specifications (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Performance (fin = fout = 622.08 MHz; BW = 7 Hz; LVPECL, XAXB = 40 MHz)						
Lock Time[2]	t_{LOCKMP}	Start of ICAL to ↓ of LOL	—	1.9	3	s
Settle Time[2]	t_{SETTLE}	Start of ICAL to F_{OUT} within 5 ppm of final value	—	5.5	6.5	s
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise fout = 622.08 MHz	CKO_{PN}	100 Hz Offset	—	–80	—	dBc/Hz
		1 kHz Offset	—	–110	—	dBc/Hz
		10 kHz Offset	—	–113	—	dBc/Hz
		100 kHz Offset	—	–117	—	dBc/Hz
		1 MHz Offset	—	–125	—	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	–80	—	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	–65	—	dBc

Notes:
1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan. Please visit the Silicon Labs Technical Support web page at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.

Table 4. Microprocessor Control

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I^2C Bus Lines (SDA, SCL)						
Input Voltage Low	VIL_{I2C}		—	—	0.25 x V_{DD}	V
Input Voltage High	VIH_{I2C}		0.7 x V_{DD}	—	V_{DD}	V
Hysteresis of Schmitt trigger inputs	$VHYS_{I2C}$	V_{DD} = 1.8V	0.1 x V_{DD}	—	—	V
		V_{DD} = 2.5 or 3.3 V	0.05 x V_{DD}	—	—	V
Output Voltage Low	VOL_{I2C}	V_{DD} = 1.8 V IO = 3 mA	—	—	0.2 x V_{DD}	V
		V_{DD} = 2.5 or 3.3 V IO = 3 mA	—	—	0.4	V

Table 4. Microprocessor Control (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SPI Specifications						
Duty Cycle, SCLK	t_{DC}	SCLK = 10 MHz	40	—	60	%
Cycle Time, SCLK	t_c		100	—	—	ns
Rise Time, SCLK	t_r	20–80%	—	—	25	ns
Fall Time, SCLK	t_f	20–80%	—	—	25	ns
Low Time, SCLK	t_{lsc}	20–20%	30	—	—	ns
High Time, SCLK	t_{hsc}	80–80%	30	—	—	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	25	ns
Delay Time, SS Rise to SDO Tri-state	t_{d3}		—	—	25	ns
Setup Time, SS to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, SS to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Slave Selects	t_{cs}		25	—	—	ns

Table 5. Jitter Generation

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition[1,2,3,4]		Min	Typ	Max	GR-253-CORE	Unit
		Measurement Filter (MHz)	DSPLL BW[1]					
Jitter Gen OC-48	J_{GEN}	0.012–20	111 Hz	—	0.5	0.6	4.02 ps_{rms} (0.01 UI_{rms})	ps_{rms}

Notes:
1. 40 MHz fundamental mode crystal used as XA/XB input.
2. V_{DD} = 2.5 V
3. T_A = 85 °C
4. Test condition: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz, LVPECL clock input: 1.19 Vppd with 0.5 ns rise/fall time (20–80%), LVPECL clock output.

Table 6. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	32	C°/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	14	C°/W

Table 7. Absolute Maximum Ratings*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		–0.5	—	3.8	V
LVCMOS Input Voltage	V_{DIG}		–0.3	—	V_{DD}+0.3	V
CKINn Voltage Level Limits	CKN_{VIN}		0	—	V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Operating Junction Temperature	T_{JCT}		–55	—	150	ºC
Storage Temperature Range	T_{STG}		–55	—	150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–			2	—	—	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–			150	—	—	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–			750	—	—	V
ESD MM Tolerance; CKIN+/CKIN–			100	—	—	V
Latch-up Tolerance			JESD78 Compliant			

***Note:** Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

2. Typical Phase Noise Performance

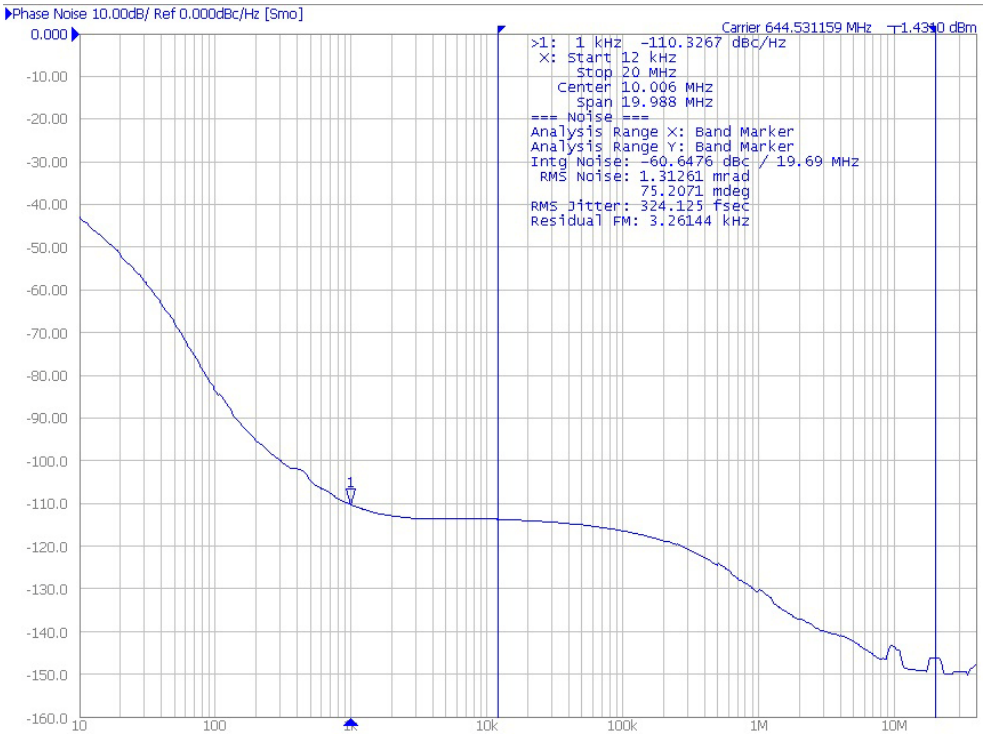


Figure 3. Typical Phase Noise (669.326 MHz)

Jitter Bandwidth	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	322 fs
SONET_OC192_A, 20 kHz to 80 MHz	322 fs
SONET_OC192_B, 4 MHz to 80 MHz	105 fs
SONET_OC192_C, 50 kHz to 80 MHz	308 fs
Brick Wall_800 Hz to 80 MHz	332 fs
Note: Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE.	

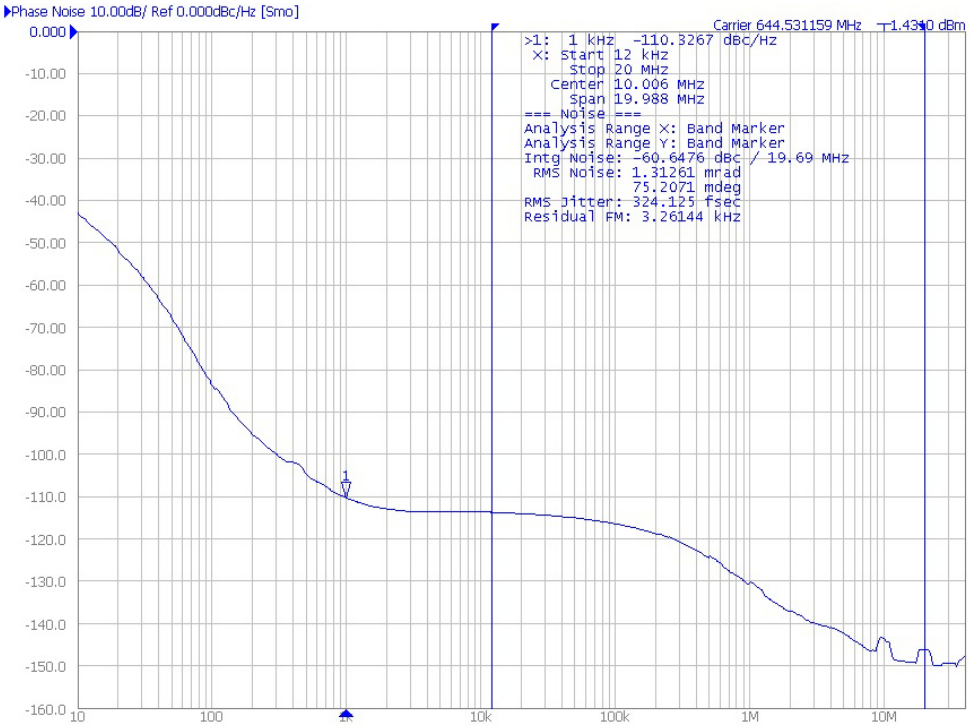
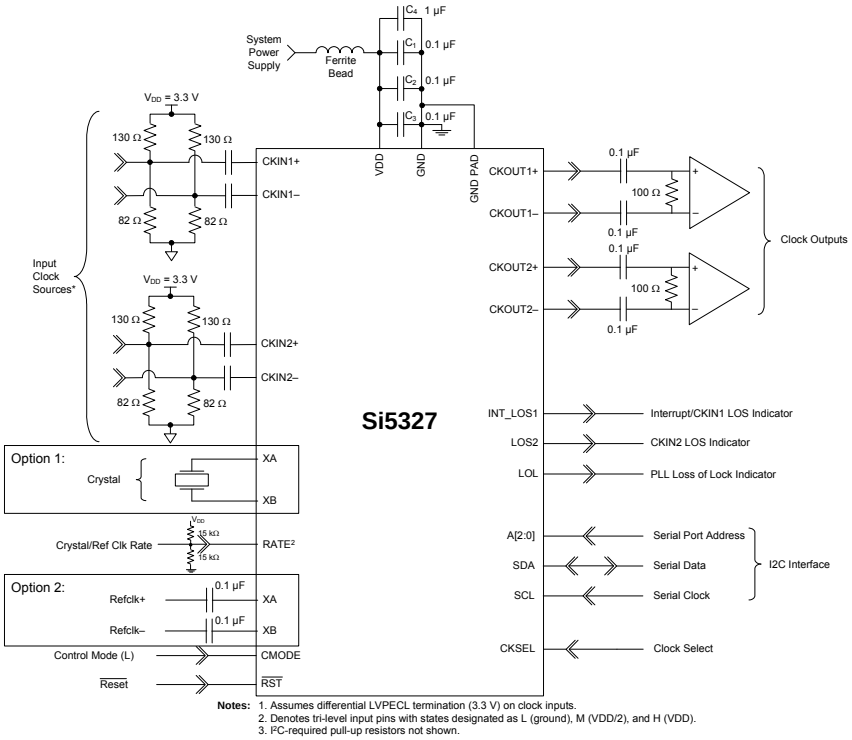


Figure 4. Typical Phase Noise (644.531 MHz)

Jitter Bandwidth	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	329 fs
SONET_OC192_A, 20 kHz to 80 MHz	328 fs
SONET_OC192_B, 4 MHz to 80 MHz	105 fs
SONET_OC192_C, 50 kHz to 80 MHz	314 fs
Brick Wall_800 Hz to 80 MHz	339 fs
Note: Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE.	

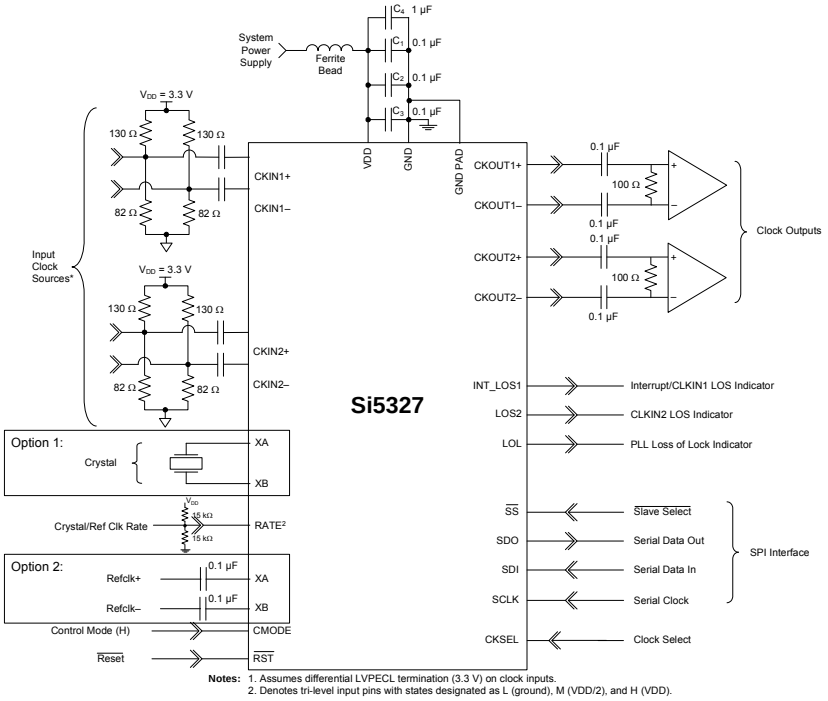
3. Typical Application Circuit



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).
3. I²C-required pull-up resistors not shown.

Figure 5. Si5327 Typical Application Circuit (I²C Control Mode)

Note: For an example schematic and layout, refer to the Si5327-EVB User's Guide.



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).

Figure 6. Si5327 Typical Application Circuit (SPI Control Mode)

Note: For an example schematic and layout, refer to the Si5327-EVB User's Guide.

4. Functional Description

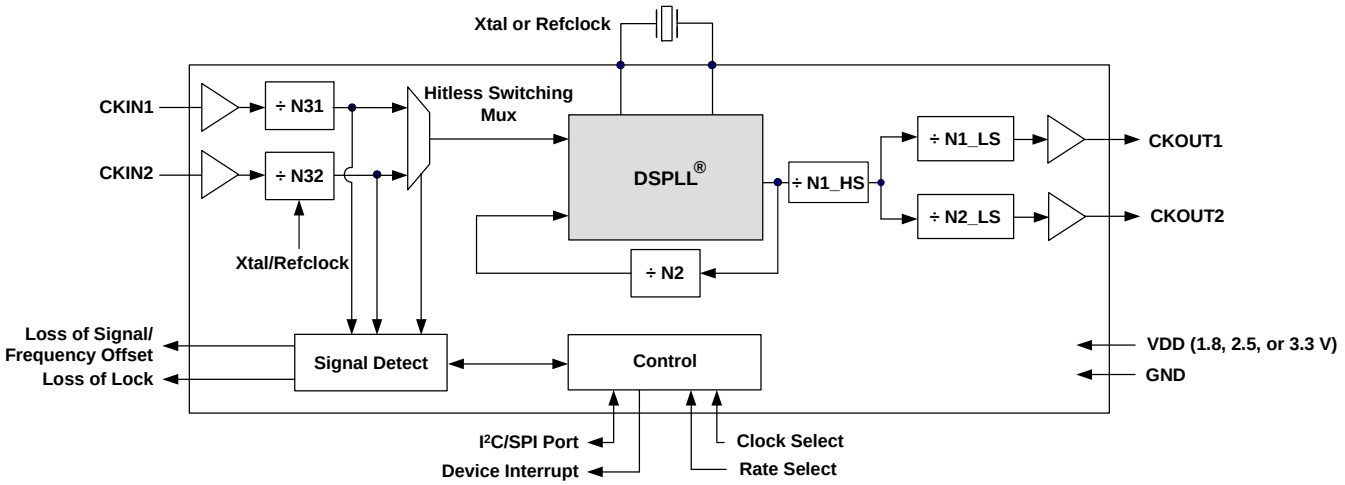


Figure 7. Functional Block Diagram

The Si5327 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5327 accepts two input clocks ranging from 2 kHz to 710 MHz and generates two output clocks ranging from 2 kHz to 808 MHz. The Si5327 can also use its crystal oscillator as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for each input clock and output clock, so the Si5327 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5327 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing.

The Si5327 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5327 PLL loop bandwidth is digitally programmable and supports a range from 4 to 525 Hz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5327 supports hitless switching between the two manually controlled synchronous input clocks in compliance with GR-253-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (maximum 200 ps phase change). The Si5327 monitors both input clocks for loss-of-signal (LOS) and provides a LOS alarm (INT_LOS1 and LOS2) when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. The Si5327 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average frequency that existed for a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5327 has two differential clock outputs. The electrical format of each clock output is independently programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. The device input to output skew is not specified. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

4.1. External Reference

An external, high quality clock or a low-cost 40 MHz crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high quality crystal. Specific recommendations may be found in the Family Reference Manual.

In digital hold, the DSPLL remains locked and tracks the external reference. Note that crystals can have temperature sensitivities.

If there is a need to use a reference oscillator instead of a crystal, Silicon Labs does not recommend using MEMS based oscillators. The very low loop BW of the Si5327 means that it can be susceptible to XAXB reference sources that have high wander. Experience has shown that in spite of having low jitter, some MEMs oscillators have high wander, and these devices should be avoided. Contact Silicon Labs for details.

4.2. Further Documentation

Consult the Silicon Laboratories Si53xx Any Frequency Precision Clock Family Reference Manual (Si53xx FRM) for detailed information about the Si5327 functions. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing.

Table 8. CKOUT_ALWAYS_ON and SQ_ICAL Truth Table

CKOUT_ALWAYS_ON	SQ_ICAL	Results
0	0	CKOUT OFF until after the first ICAL
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)
1	0	CKOUT always ON, including during an ICAL
1	1	CKOUT always ON, including during an ICAL. Use these settings to preserve output-to-output skew

5. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

Register	D7	D6	D5	D4	D3	D2	D1	D0
0		FREE_RUN	CKOUT_ ALWAYS_ ON				BYPASS_ REG	
2	BWSEL_REG[3:0]							
3			VCO_ FREEZE	SQ_ICAL				
4				HIST_DEL[4:0]				
5	ICMOS[1:0]							
6			SFOUT2_REG[2:0]			SFOUT1_REG[2:0]		
8	HLOG_2[1:0]		HLOG_1[1:0]					
9	HIST_AVG[4:0]							
10					DSBL2_ REG	DSBL1_ REG		
11							PD_CK2	PD_CK1
19				VALTIME[1:0]		LOCK[T2:0]		
20					CK2_ BAD_ PIN	CK1_ BAD_ PIN	LOL_PIN	INT_PIN
22						CK_BAD_ POL	LOL_POL	INT_POL
23						LOS2_MSK	LOS1_MSK	LOSX_MSK
24								LOL_MSK
25		N1_HS[2:0]						
31					NC1_LS[19:16]			
32	NC1_LS[15:8]							
33	NC1_LS[7:0]							
34					NC2_LS[19:16]			
35	NC2_LS[15:8]							
36	NC2_LS[7:0]							
40	N2_HS[2:0]				N2_LS[19:16]			
41	N2_LS[15:8]							

Register	D7	D6	D5	D4	D3	D2	D1	D0
42	N2_LS[7:0]							
43						N31[18:16]		
44	N31[15:8]							
45	N31[7:0]							
46						N32[18:16]		
47	N32[15:8]							
48	N32[7:0]							
128							CK2_ACT-V_REG	CK1_ACT-V_REG
129						LOS2_INT	LOS1_INT	LOSX_INT
130								LOL_INT
131						LOS2_FLG	LOS1_FLG	LOSX_FLG
132							LOL_FLG	
134	PARTNUM_RO[11:4]							
135	PARTNUM_RO[3:0]				REVID_RO[3:0]			
136	RST_REG	ICAL						
137								FASTLOCK
138							LOS2_EN [1:1]	LOS1_EN [1:1]
139			LOS2_EN [0:0]	LOS1_EN [0:0]				

6. Register Descriptions

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FREE_ RUN	CKOUT_ ALWAYS_ ON				BYPASS_ REG	
Type	R	R/W	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7	Reserved	
6	FREE_RUN	**Free Run.** Internal to the device, route XA/XB to CKIN2. This allows the device to lock to its XA-XB reference. 0: Disable 1: Enable
5	CKOUT_ ALWAYS_ON	**CKOUT Always On.** This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 8 on page 20. 0: Squelch output until part is calibrated (ICAL). 1: Provide an output. Note: The frequency may be significantly off and variable until the part is calibrated.
4:2	Reserved	
1	BYPASS_ REG	**Bypass Register.** This bit enables or disables the PLL bypass mode. Use only when the device is in digital hold or before the first ICAL. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing the PLL. Bypass mode does not support CMOS clock outputs.
0	Reserved	

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]							
Type	R/W				R	R	R	R

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	**BWSEL_REG.** Selects nominal f3dB bandwidth for PLL. See DSPLL*sim* for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	Reserved	

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VCO_FREEZE	SQ_ICAL				
Type	R		R/W	R/W	R	R	R	R

Reset value = 0000 0101

Bit	Name	Function
7:6	Reserved	
5	VCO_FREEZE	**VCO_FREEZE.** Forces the part into VCO freeze. This bit overrides all other manual and automatic clock selection controls. 0: Normal operation. 1: Force VCO freeze mode. Overrides all other settings and ignores the quality of all of the input clocks.
4	SQ_ICAL	**SQ_ICAL.** This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 8 on page 20. 0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.
3:0	Reserved	

Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				HIST_DEL [4:0]				
Type	R	R	R	R/W				

Reset value = 0001 0010

Bit	Name	Function
7:5	Reserved	
4:0	HIST_DEL [4:0]	**HIST_DEL [4:0].** Selects amount of delay to be used in generating the history information used for Digital Hold. See the Si53xx Family Reference Manual for a detailed description.

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ICMOS [1:0]							
Type	R/W		R	R	R	R	R	R

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	**ICMOS [1:0].** When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-. 00: 8mA/2mA 01: 16mA/4mA 10: 24mA/6mA 11: 32mA/8mA
5:0	Reserved	

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			SFOUT2_REG [2:0]			SFOUT1_REG [2:0]		
Type	R	R	R/W			R/W		

Reset value = 0010 1101

Bit	Name	Function
7:6	Reserved	
5:3	SFOUT2_REG [2:0]	**SFOUT2_REG [2:0].** Controls output signal format and disable for CKOUT2 output buffer. 000: Reserved 001: Disable 010: CMOS (Bypass mode not supported) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS **Note:** LVPECL requires a nominal $V_{DD} \geq 2.5$ V.
2:0	SFOUT1_REG [2:0]	**SFOUT1_REG [2:0].** Controls output signal format and disable for CKOUT1 output buffer. 000: Reserved 001: Disable 010: CMOS (Bypass mode not supported) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS **Note:** LVPECL requires a nominal $V_{DD} \geq 2.5$ V.

Register 8.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HLOG_2[1:0]		HLOG_1[1:0]					
Type	R/W		R/W		R			

Reset value = 0000 0000

Bit	Name	Function
7:6	HLOG_2 [1:0]	**HLOG_2 [1:0].** 00: Normal operation 01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
5:4		**HLOG_1 [1:0].** 00: Normal operation 01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
3:0	Reserved	

Register 9.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HIST_AVG [4:0]							
Type	R/W					R	R	R

Reset value = 1100 0000

Bit	Name	Function
7:3	HIST_AVG [4:0]	**HIST_AVG [4:0].** Selects amount of averaging time to be used in generating the history information for Digital Hold. See the Si53xx Family Reference Manual for a detailed description
2:0	Reserved	

Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					DSBL2_REG	DSBL1_REG		
Type	R	R	R	R	R/W	R/W	R	R

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3	DSBL2_REG	**DSBL2_REG.** This bit controls the powerdown of the CKOUT2 output buffer. If disable mode is selected, the NC2_LS output divider is also powered down. 0: CKOUT2 enabled 1: CKOUT2 disabled
2	DSBL1_REG	**DSBL1_REG.** This bit controls the powerdown of the CKOUT1 output buffer. If disable mode is selected, the NC1_LS output divider is also powered down. 0: CKOUT1 enabled 1: CKOUT1 disabled
1:0	Reserved	

Register 11.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							PD_CK2	PD_CK1
Type	R	R	R	R	R	R	R/W	R/W

Reset value = 0100 0000

Bit	Name	Function
7:2	Reserved	
1	PD_CK2	**PD_CK2.** This bit controls the powerdown of the CKIN2 input buffer. 0: CKIN2 enabled 1: CKIN2 disabled
0	PD_CK1	**PD_CK1.** This bit controls the powerdown of the CKIN1 input buffer. 0: CKIN1 enabled 1: CKIN1 disabled

Register 19.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				VALTIME [1:0]		LOCKT [2:0]		
Type	R	R	R	R/W		R/W		

Reset value = 0010 1100

Bit	Name	Function
7:5	Reserved	
4:3	VALTIME [1:0]	**VALTIME [1:0].** Sets amount of time for input clock to be valid before the associated alarm is removed. 00: 2 ms 01: 100 ms 10: 200 ms 11: 13 seconds
2:0	LOCKT [2:0]	**LOCKT [2:0].** Sets retrigger interval for one shot monitoring phase detector output. One shot is triggered by phase slip in DSPLL. Refer to the Si53xx Family Reference Manual for more details. To minimize lock time, the value 001 for LOCKT is recommended. 000: 106 ms 001: 53 ms 010: 26.5 ms 011: 13.3 ms 100: 6.6 ms 101: 3.3 ms 110: 1.66 ms 111: .833 ms

Register 20.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CK2_BAD_PIN	CK1_BAD_PIN	LOL_PIN	INT_PIN
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 0011 1110

Bit	Name	Function
7:4	Reserved	
3	CK2_BAD_PIN	**CK2_BAD_PIN.** The CK2_BAD status can be reflected on the LOS2 output pin. 0: LOS2 output pin tristated 1: CK2_BAD status reflected to output pin
2	CK1_BAD_PIN	**CK1_BAD_PIN.** Either LOS1 or INT (see INT_PIN) status can be reflected on the INT_LOS1 output pin. 0: INT_LOS1 output pin tristated 1: LOS1 or INT (see INT_PIN) status reflected to output pin
1	LOL_PIN	**LOL_PIN.** The LOL_INT status bit can be reflected on the LOL output pin. 0: LOL output pin tristated 1: LOL_INT status reflected to output pin
0	INT_PIN	**INT_PIN.** Reflects the interrupt status on the INT_LOS1 output pin. 0: Interrupt status not displayed on INT_LOS1 output pin. Instead, the INT_LOS1 pin indicates when CKIN1 is bad. If CK1_BAD_PIN = 0, INT_LOS1 output pin is tristated. 1: Interrupt status reflected to output pin.

Register 22.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						CK_BAD_ POL	LOL_POL	INT_POL
Type	R	R	R	R	R	R	R/W	R/W

Reset value = 1101 1111

Bit	Name	Function
7:3	Reserved	
2	CK_BAD_ POL	**CK_BAD_POL.** Sets the active polarity for the INT_C1B and C2B signals when reflected on output pins. 0: Active low 1: Active high
1	LOL_POL	**LOL_POL.** Sets the active polarity for the LOL status when reflected on an output pin. 0: Active low 1: Active high
0	INT_POL	**INT_POL.** Sets the active polarity for the interrupt status when reflected on the INT_LOS1 output pin. 0: Active low 1: Active high

Register 23.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						LOS2_ MSK	LOS1_ MSK	LOSX_ MSK
Type	R	R	R	R	R	R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	
2	LOS2_MSK	**LOS2_MSK.** Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register. 0: LOS2 alarm triggers active interrupt on INT_LOS1 output (if INT_PIN=1). 1: LOS2_FLG ignored in generating interrupt output.
1	LOS1_MSK	**LOS1_MSK.** Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register. 0: LOS1 alarm triggers active interrupt on INT_LOS1 output (if INT_PIN=1). 1: LOS1_FLG ignored in generating interrupt output.
0	LOSX_MSK	**LOSX_MSK.** Determines if a LOS on XA/XB(LOSX_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOSX_FLG register. 0: LOSX alarm triggers active interrupt on INT_LOS1 output (if INT_PIN=1). 1: LOSX_FLG ignored in generating interrupt output.

Register 24.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								LOL_MSK
Type	R	R	R	R	R	R	R	R

Reset value = 0011 1111

Bit	Name	Function
7:1	Reserved	
0	LOL_MSK	**LOL_MSK.** Determines if the LOL_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the LOL_FLG register. 0: LOL alarm triggers active interrupt on INT_LOS1 output (if INT_PIN=1). 1: LOL_FLG ignored in generating interrupt output.

Register 25.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1_HS [2:0]							
Type	R/W			R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	**N1_HS [2:0].** Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 2) low-speed divider. 000: N1= 4 001: N1= 5 010: N1= 6 011: N1= 7 100: N1= 8 101: N1= 9 110: N1= 10 111: N1= 11
4:0	Reserved	

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC1_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC1_LS [19:16]	**NC1_LS [19:16].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	**NC1_LS [15:8].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [19:0]	**NC1_LS [7:0].** Sets value for N1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC2_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC2_LS [19:16]	**NC2_LS [19:16].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 0000000000000000000=1 0000000000000000001=2 0000000000000000011=4 0000000000000000101=6 ... 1111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC2_LS [15:8]	**NC2_LS [15:8].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 36.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC2_LS [7:0]	**NC2_LS [7:0].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_HS [2:0]				N2_LS [19:16]			
Type	R/W			R	R/W			

Reset value = 1100 0000

Bit	Name	Function
7:5	N2_HS [2:0]	**N2_HS [2:0].** Sets value for N2 high speed divider, which drives N2_LS low-speed divider. 000: 4 001: 5 010: 6 011: 7 100: 8 101: 9 110: 10 111: 11
4	Reserved	
3:0	N2_LS [19:16]	**N2_LS [19:16].** Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^20 Valid divider values = [2, 4, 6, ..., 2^20]

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	**N2_LS [15:8].** Sets value for N2 low-speed divider, which drives phase detector. 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111 = 2^20 Valid divider values = [2, 4, 6, ..., 2^20]

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [7:0]							
Type	R/W							

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	**N2_LS [7:0].** Sets value for N2 low-speed divider, which drives phase detector. 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111 = 2^20 Valid divider values = [2, 4, 6, ..., 2^20]

Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N31 [18:16]		
Type	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N31 [18:16]	**N31 [18:16].** Sets value for input divider for CKIN1. 000000000000000000 = 1 000000000000000001 = 2 000000000000000010 = 3 ... 111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N31_[15:8]	**N31_[15:8].** Sets value for input divider for CKIN1. 000000000000000000 = 1 000000000000000001 = 2 000000000000000010 = 3 ... 111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N31_[7:0	**N31_[7:0].** Sets value for input divider for CKIN1. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N32_[18:16]		
Type	R					R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N32_[18:16]	**N32_[18:16].** Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N32_[15:8]	N32[15:8]. Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N32_[7:0]	**N32[7:0].** Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							CK2_ACTV_REG	CK1_ACTV_REG
Type	R	R	R	R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:2	Reserved	
1	CK2_ACTV_REG	**CK2_ACTV_REG.** Indicates if CKIN2 is currently the active clock for the PLL input. 0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1. 1: CKIN2 is the active input clock.
0	CK1_ACTV_REG	**CK1_ACTV_REG.** Indicates if CKIN1 is currently the active clock for the PLL input. 0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1. 1: CKIN1 is the active input clock.

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						LOS2_INT	LOS1_INT	LOSX_INT
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0110

Bit	Name	Function
7:3	Reserved	
2	LOS2_INT	**LOS2_INT.** Indicates the LOS status on CKIN2. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN2 input.
1	LOS1_INT	**LOS1_INT.** Indicates the LOS status on CKIN1. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN1 input.
0	LOSX_INT	**LOSX_INT.** Indicates the LOS status of the external reference on the XA/XB pins. 0: Normal operation. 1: Internal loss-of-signal alarm on XA/XB reference clock input.

Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								LOL_INT
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0001

Bit	Name	Function
7:1	Reserved	
0	LOL_INT	**PLL Loss of Lock Status.** 0: PLL locked. 1: PLL unlocked.

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						LOS2_FLG	LOS1_FLG	LOSX_FLG
Type	R	R	R	R	R	R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	
2	LOS2_FLG	**CKIN2 Loss-of-Signal Flag.** 0: Normal operation. 1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS2_MSK bit. Flag cleared by writing 0 to this bit.
1	LOS1_FLG	**CKIN1 Loss-of-Signal Flag.** 0: Normal operation 1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS1_MSK bit. Flag cleared by writing 0 to this bit.
0	LOSX_FLG	**External Reference (signal on pins XA/XB) Loss-of-Signal Flag.** 0: Normal operation 1: Held version of LOSX_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOSX_MSK bit. Flag cleared by writing 0 to this bit.

Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOL_FLG	
Type	R	R	R	R	R	R	R/W	R

Reset value = 0000 0010

Bit	Name	Function
7:2	Reserved	
1	LOL_FLG	**PLL Loss of Lock Flag.** 0: PLL locked 1: Held version of LOL_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOL_MSK bit. Flag cleared by writing 0 to this bit.
0	Reserved	

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [11:4]							
Type	R							

Reset value = 0000 0001

Bit	Name	Function
7:0	PARTNUM_ RO [11:0]	**Device ID (1 of 2).** 0000 0001 1011: Si5327

Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [3:0]				REVID_RO [3:0]			
Type	R				R			

Reset value = 1011 0010

Bit	Name	Function
7:4	PARTNUM_RO [11:0]	**Device ID (2 of 2).** 0000 0001 1011: Si5327
3:0	REVID_RO [3:0]	**Device Revision.** 0000: Revision A 0001: Revision B 0010: Revision C Others: Reserved

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	ICAL						
Type	R/W	R/W	R	R	R	R	R	R

Reset value = 0000 0000

Bit	Name	Function
7	RST_REG	**Internal Reset (Same as Pin Reset).** **Note:** The I^2C (or SPI) port may not be accessed until 10 ms after RST_REG is asserted. 0: Normal operation. 1: Reset of all internal logic. Outputs disabled or tristated during reset.
6	ICAL	**Start an Internal Calibration Sequence.** For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a “1” to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. 0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, LOL will go low. **Notes:** **1.** A valid stable clock (within 100 ppm) must be present to begin ICAL. **2.** If the input changes by more than 500 ppm, the part may do an autonomous ICAL. **3.** See Table 9, “Register Locations Requiring ICAL,” on page 53 for register changes that require an ICAL.
5:0	Reserved	

Register 137.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								FASTLOCK
Type	R	R	R	R	R	R	R	R/W

Reset value = 0000 0000

Bit	Name	Function
7:1	Reserved	Do not modify.
0	FASTLOCK	This bit must be set to 1 to enable FASTLOCK. This improves initial lock time by dynamically changing the loop bandwidth.

Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOS2_EN	LOS1_EN
Type	R	R	R	R	R	R	R/W	R/W

Reset value = 0000 1111

Bit	Name	Function
7:2	Reserved	
1	LOS2_EN	**Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).** **Note:** LOS2_EN is split between two registers. 00: Disable LOS monitoring 01: Reserved 10: Enable LOSA monitoring 11: Enable LOS monitoring LOSA is a slower and less sensitive version of LOS. SEe the Si53xx Family Reference Manual for details.
0	LOS1_EN	**Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring 01: Reserved 10: Enable LOSA monitoring 11: Enable LOS monitoring LOSA is a slower and less sensitive version of LOS. See the Si53xx Family Reference Manual for details.

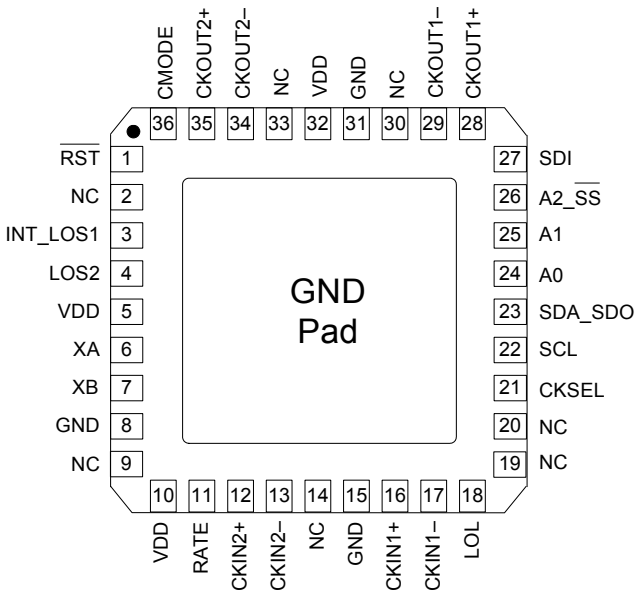
Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			LOS2_EN	LOS1_EN				
Type	R	R	R/W	R/W	R	R	R	R

Reset value = 1111 1111

Bit	Name	Function
7:6	Reserved	
5	LOS2_EN	**Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).** **Note:** LOS2_EN is split between two registers. 00: Disable LOS monitoring 01: Reserved 10: Enable LOSA monitoring 11: Enable LOS monitoring LOSA is a slower and less sensitive version of LOS. See the Si53xx Family Reference Manual for details
4	LOS1_EN	**Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring 01: Reserved 10: Enable LOSA monitoring 11: Enable LOS monitoring LOSA is a slower and less sensitive version of LOS. See the Si53xx Family Reference Manual for details.
3:0	Reserved	

7. Pin Descriptions: Si5327



Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. The part must be programmed after a reset or power on to get a clock output. See the Si53xx Family Reference Manual for details. This pin has a weak pull-up.
2, 9, 14, 19, 20, 30, 33	NC			**No Connection.** Leave floating. Make no external connections to this pin for normal operation.
3	INT_LOS1	O	LVCMOS	**Interrupt/CKIN1 LOS Indicator.** This pin functions as a device interrupt output or an alarm output for CKIN1. If used as an interrupt output, *INT_PIN* must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the *INT_POL* register bit. If used as an alarm output, the pin functions as a LOS alarm indicator for CKIN1. Set *CK1_BAD_PIN* = 1 and *INT_PIN* = 0. 0 = CKIN1 present 1 = LOS on CKIN1 The active polarity is controlled by *CK_BAD_POL*. If no function is selected, the pin tristates.
Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Section “5.Register Map”.				

Pin #	Pin Name	I/O	Signal Level	Description
4	LOS2	O	LVCMOS	**CKIN2 Invalid Indicator.** This pin functions as a LOS alarm indicator for CKIN2 if *CK2_BAD_PIN* = 1. 0 = CKIN2 present 1 = LOS on CKIN2 The active polarity can be changed by *CK_BAD_POL*. If *CK2_BAD_PIN* = 0, the pin tristates.
5, 10, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should also be placed as close to the device as is practical.
7 6	XB XA	I	Analog	**External Crystal or Reference Clock.** External crystal should be connected to these pins to use internal oscillator based reference. Refer to the Si53xx Family Reference Manual for interfacing to an external reference. External reference must be from a high-quality clock source (TCXO, OCXO). Accepts 37–41 MHz crystal or reference clock, as determine by the RATE pin setting.
8, 15, 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device. Grounding these pins does not eliminate the requirement to ground the GND PAD on the bottom of the package.
11	RATE	I	3-Level	**External Crystal or Reference Clock Rate.** Three level input that selects an external crystal or reference clock to be applied to the XA/XB interface. L setting (GND) = crystal on XA/XB M setting (VDD/2) = clock or XO on XA/XB H setting (VDD) = reserved Some designs may require an external resistor voltage divider when driven by an active device that will tristate.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 2 kHz to 710 MHz.
12 13	CKIN2+ CKIN2–	I	Multi	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 2 kHz to 710 MHz.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Section “5.Register Map”.

Pin #	Pin Name	I/O	Signal Level	Description
18	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator if the LOL_PIN register bit is set to 1. 0 = PLL locked 1 = PLL unlocked If *LOL_PIN* = 0, this pin will tristate. Active polarity is controlled by the *LOL_POL* bit. The PLL lock status will always be reflected in the *LOL_INT* read only register bit.
21	CKSEL	I	LVCMOS	**Input Clock Select.** This pin functions as the manual input clock selector. 0 = Select CKIN1 1 = Select CKIN2 CKSEL should not be left open and should be driven to either logic high or logic low.
22	SCL	I	LVCMOS	**Serial Clock.** This pin functions as the serial clock input for both SPI and I^2C modes. This pin has a weak pull-down.
23	SDA_SDO	I/O	LVCMOS	**Serial Data.** In I^2C control mode (CMODE = 0), this pin functions as the bidirectional serial data port. In SPI control mode (CMODE = 1), this pin functions as the serial data output.
25 24	A1 A0	I	LVCMOS	**Serial Port Address.** In I^2C control mode (CMODE = 0), these pins function as hardware controlled address bits. The I^2C address is 1101 [A2] [A1] [A0]. In SPI control mode (CMODE = 1), these pins are ignored. These pins have a weak pull-down.
26	A2_$\overline{SS}$	I	LVCMOS	**Serial Port Address/Slave Select.** In I^2C control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2]. In SPI control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pull-down.
27	SDI	I	LVCMOS	**Serial Data In.** In I^2C control mode (CMODE = 0), this pin is ignored. In SPI control mode (CMODE = 1), this pin functions as the serial data input. This pin has a weak pull-down.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Section “5.Register Map”.

Pin #	Pin Name	I/O	Signal Level	Description
29 28	CKOUT1– CKOUT1+	O	Multi	**Output Clock 1.** Differential output clock with a frequency range of 2 kHz to 808 MHz. Output signal format is selected by *SFOUT1_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
34 35	CKOUT2– CKOUT2+	O	Multi	**Output Clock 2.** Differential output clock with a frequency range of 2 kHz to 808 MHz. Output signal format is selected by *SFOUT2_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
36	CMODE	I	LVCMOS	**Control Mode.** Selects I^2C or SPI control mode for the Si5327. 0 = I^2C Control Mode 1 = SPI Control Mode This pin must not be NC. Tie either high or low. See the Si53xx Family Reference Manual for details on I^2C or SPI operation.
GND PAD	GND	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Section “5.Register Map”.

Table 9 lists all of the register locations that should be followed by an ICAL after their contents are changed.

Table 9. Register Locations Requiring ICAL

Addr	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
2	BWSEL_REG
4	HIST_DEL
5	ICMOS
9	HIST_AVG
10	DSBL2_REG
10	DSBL1_REG
11	PD_CK2
11	PD_CK1
19	VALTIME
19	LOCKT
25	N1_HS
31	NC1_LS
34	NC2_LS
40	N2_HS
40	N2_LS
43	N31
46	N32

Table 10. Si5327 Internal Pull up/Pull down

Pin #	Si5327	Pull up/ Pull down
1	$\overline{\text{RST}}$	U
11	RATE	U, D
21	CKSEL	U, D
22	SCL	D
24	A0	D
25	A1	D
26	A2_SS	D
27	SDI	D
36	CMODE	U, D

8. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	ROHS6, Pb-Free	Temperature
Si5327B-C-GM	2 kHz–808 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5327C-C-GM	2 kHz–346 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5327D-C-GM	2 kHz–243 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5327-EVB		Evaluation Board		
Note: Add an R at the end of the device to denote tape and reel options.				

9. Package Outline: 36-Pin QFN

Figure 8 illustrates the package details for the Si5327. Table 11 lists the values for the dimensions shown in the illustration.

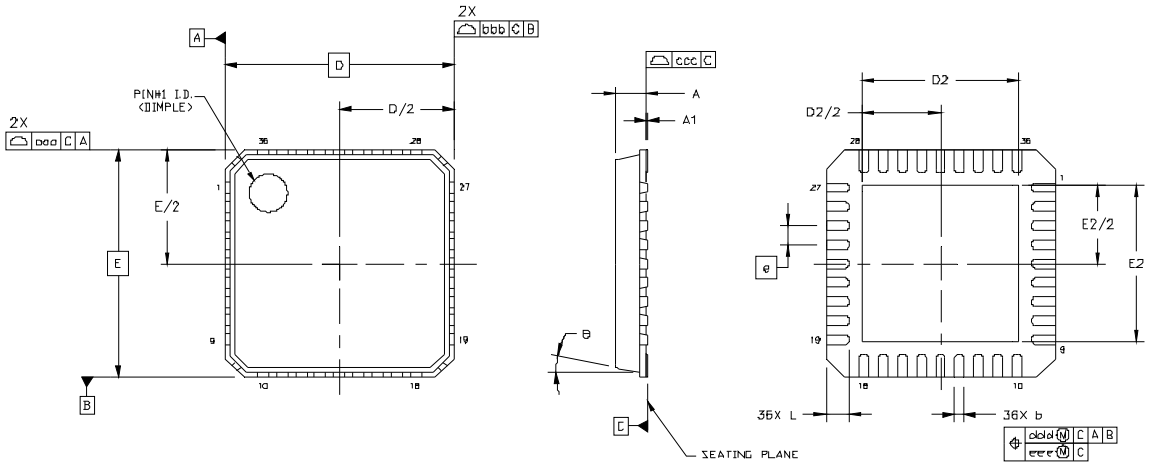


Figure 8. 36-Pin Quad Flat No-lead (QFN)

Table 11. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		6.00 BSC	
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.70
θ	—	—	12º
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Recommended PCB Layout

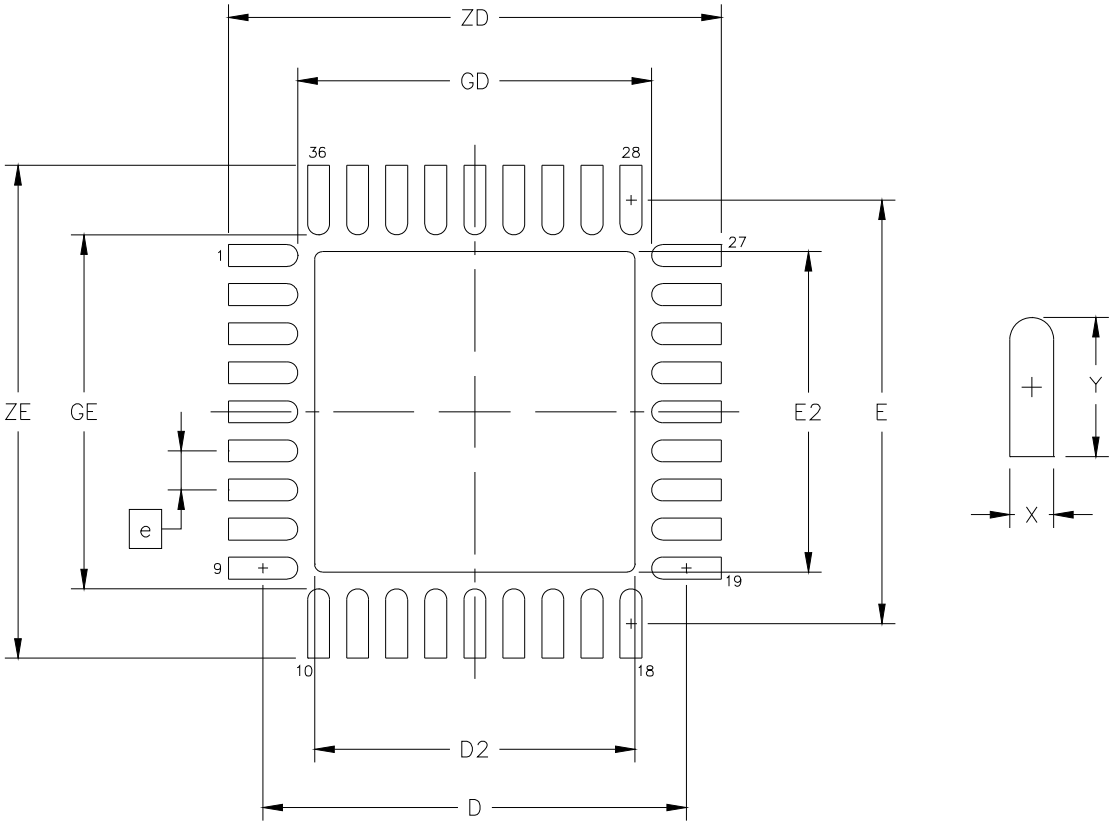


Figure 9. PCB Land Pattern Diagram

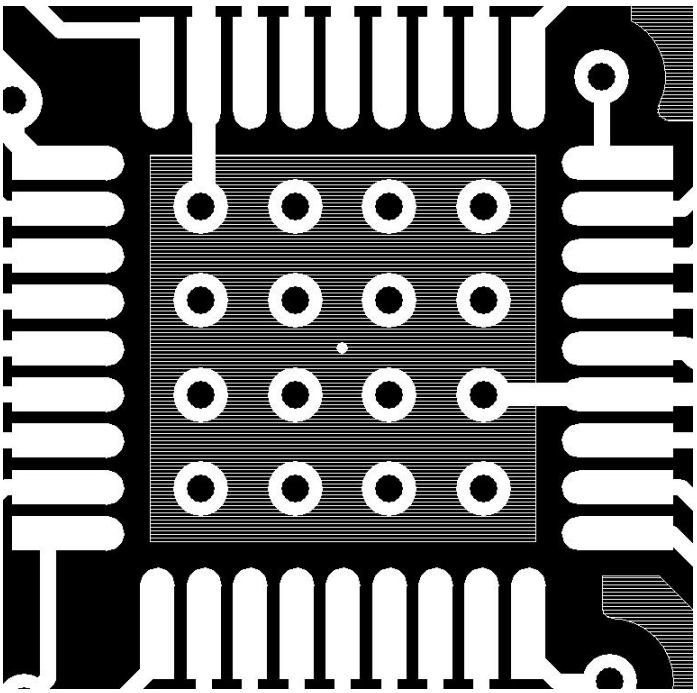


Figure 10. Ground Pad Recommended Layout

Table 12. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

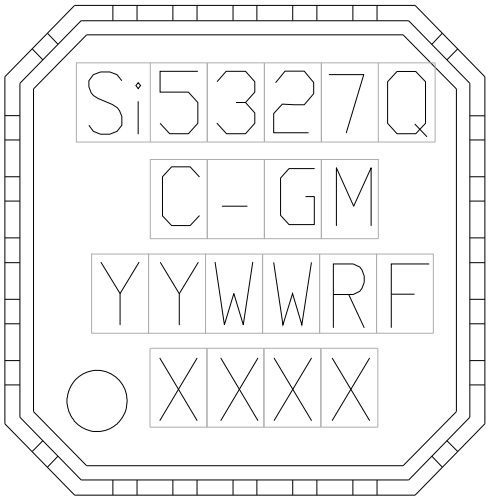
Stencil Design

6. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Si5327 Device Top Mark



Mark Method:	Laser	
Font Size:	0.80 mm Right-Justified	
Line 1 Marking:	Si5327Q	Customer Part Number Q = Speed Code: B, C, D See Ordering Guide for options
Line 2 Marking:	C-GM	C = Product Revision G = Temperature Range –40 to 85 °C (RoHS6) M = QFN Package
Line 3 Marking:	YYWWRF	YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 4 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	XXXX	Internal Code

Document Change List

Revision 0.1 to Revision 0.4

- Updated Table 3, “AC Specifications,” on page 9.
  - Added table note.
- Updated Table 5, “Jitter Generation,” on page 14.
  - Updated maximum jitter generation specifications.

Revision 0.4 to Revision 1.0

- Minor changes to Table 2 on page 5
- Minor changes to Table 4 on page 12
- Added maximum lock and settle time specs to Table 3.
- Fixed typos in description of Register 10 on page 28.
- Fixed typos in description of Register 48 on page 41.
- Added warning about MEMS oscillators to "4.1." on page 20.

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