ISL98012

1.8V Input PWM Step-Up Regulator

FN6654
Rev 1.00
December 8, 2010

The ISL98012 is a high frequency, high efficiency step-up DC/DC regulator operated in fixed frequency PWM mode. With an integrated 1.4A MOSFET, it can deliver up to 600mA output current at up to 92% efficiency. The adjustable switching frequency is up to 750kHz, making it ideal for common boost applications.

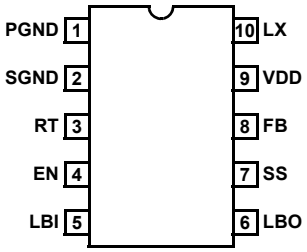
When shut down, it draws <1µA of current. This feature, along with the minimum starting voltage of 1.8V, makes it suitable for portable equipment powered by 1 Lithium Ion, 3 to 4 NiMH cells, or 2 cells of alkaline battery.

The ISL98012 is available in a 10 Ld MSOP package, with a maximum height of 1.1mm. With proper external components, the whole converter takes less than 0.25in^2 PCB space.

This device is specified for operation over the full -40°C to +85°C temperature range.

Pinout

ISL98012
(10 LD MSOP)
TOP VIEW



Features

- Up to 92% Efficiency
- Up to 600mA I_{OUT}
- 4.5V < V_{OUT} < 17V
- 1.8V < V_{IN} < 13.2V
- Up to 750kHz Adjustable Frequency
- <1µA Shutdown Current
- Adjustable Soft-Start
- Low Battery Detection
- Internal Thermal Protection
- 1.1mm Max Height 10 Ld MSOP Package
- Pb-Free (RoHS compliant)

Applications

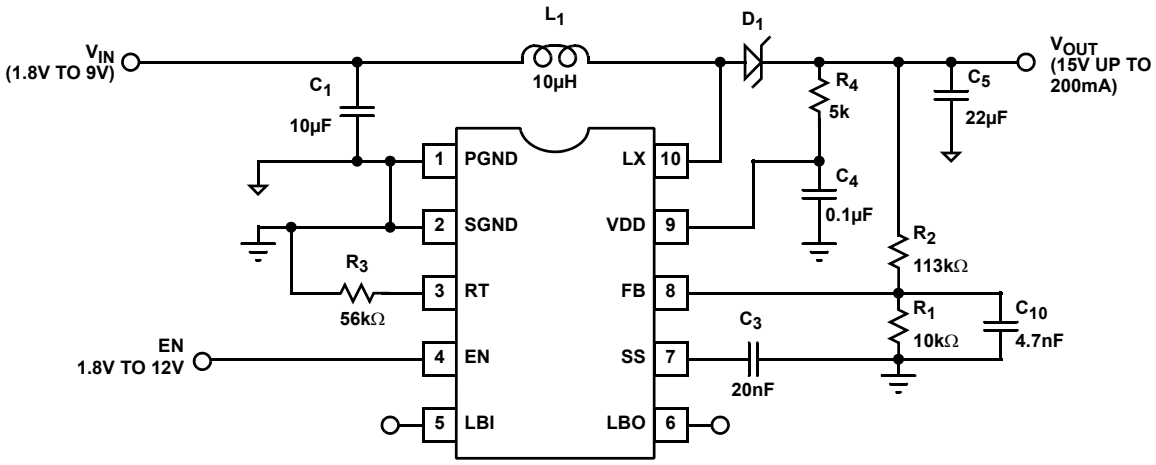
- 1.8V to 15V Converters - OLED
- 5V to 12V Converters
- 3V to 5V and 3V to 12V Converters
- TFT-LCD
- Portable Equipment

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL98012IUZ	98012	10 Ld MSOP	M10.118A
ISL98012IUZ-T*	98012	10 Ld MSOP	M10.118A
ISL98012IUZ-TK*	98012	10 Ld MSOP	M10.118A

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application



Absolute Maximum Ratings (T_A = +25°C)

FB, SS, RT, ... -0.3V, 6.5V
LX. . . . . -0.3V, +18V
VDD, EN, LBI, LBO . . . . . -0.3V, +12V

Maximum Operating Conditions

Maximum Operating Frequency. 750kHz
Minimum Operating Frequency 380kHz

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
10 Lead MSOP. 152
Storage Temperature . . . . . .-65°C to +150°C
Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature: . . . . . .+135°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{IN} = 5V, V_{OUT} = 12V, L = 10µH, I_{OUT} = 0mA, R_T = 56kΩ, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	R_4 must ensure $V_{DD} \leq 12V$	1.8		13.2	V
V_{OUT}	Output Voltage Range	Note 2	4.5		17	V
IQ1	Quiescent Current - Shut-down	V_{EN} = 0, feedback resistors disconnected			1	µA
IQ2	Quiescent Current	V_{EN} = 2V, Continuous operation		1.4	2	mA
V_{FB}	Feedback Voltage		1.29	1.33	1.37	V
I_{FB}	Feedback Input Bias Current	$0 < V_{FB} < 1.5V$			0.10	µA
D_{MAX}	Maximum Duty Cycle		89.5	92		%
I_{LIM}	Current Limit - Max Peak Input Current		1	1.4		A
I_{EN}	Enable Input Bias Current				1	µA
V_{LBI}	LBI Threshold Voltage		180	220	250	mV
V_{OL-LBO}	LBO Output Low	I_{LBO} = 1mA		0.1	0.2	V
$I_{LEAK-LBO}$	LBO Output Leakage Current	V_{LBI} = 250mV, V_{LBO} = 5V		0.02	2	µA
$R_{DS(ON)}$	Switch On Resistance	At 12V output		220		mΩ
$I_{LEAK-SWITCH}$	Switch Leakage Current	LX = 18V			1	µA
$\Delta V_{OUT}/\Delta V_{IN}/V_{OUT}$	Line Regulation	$3V < V_{IN} < 6V$, V_{OUT} = 12V, no load		0.4		%/V
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	I_{OUT} = 50mA to 150mA		1		%
I_{SS}	Soft Start Current	$0 < V_{SS} < 0.1V$		12		µA
V_{RT}	Voltage at R_T for Bias Current	R_T = 56kΩ		1.34		V
f_{OSC1}	Switching Frequency	R_T = 56kΩ	600	670	750	kHz
VHI_EN	EN Input High Threshold		1.6			V
VLO_EN	EN Input Low Threshold				0.5	V

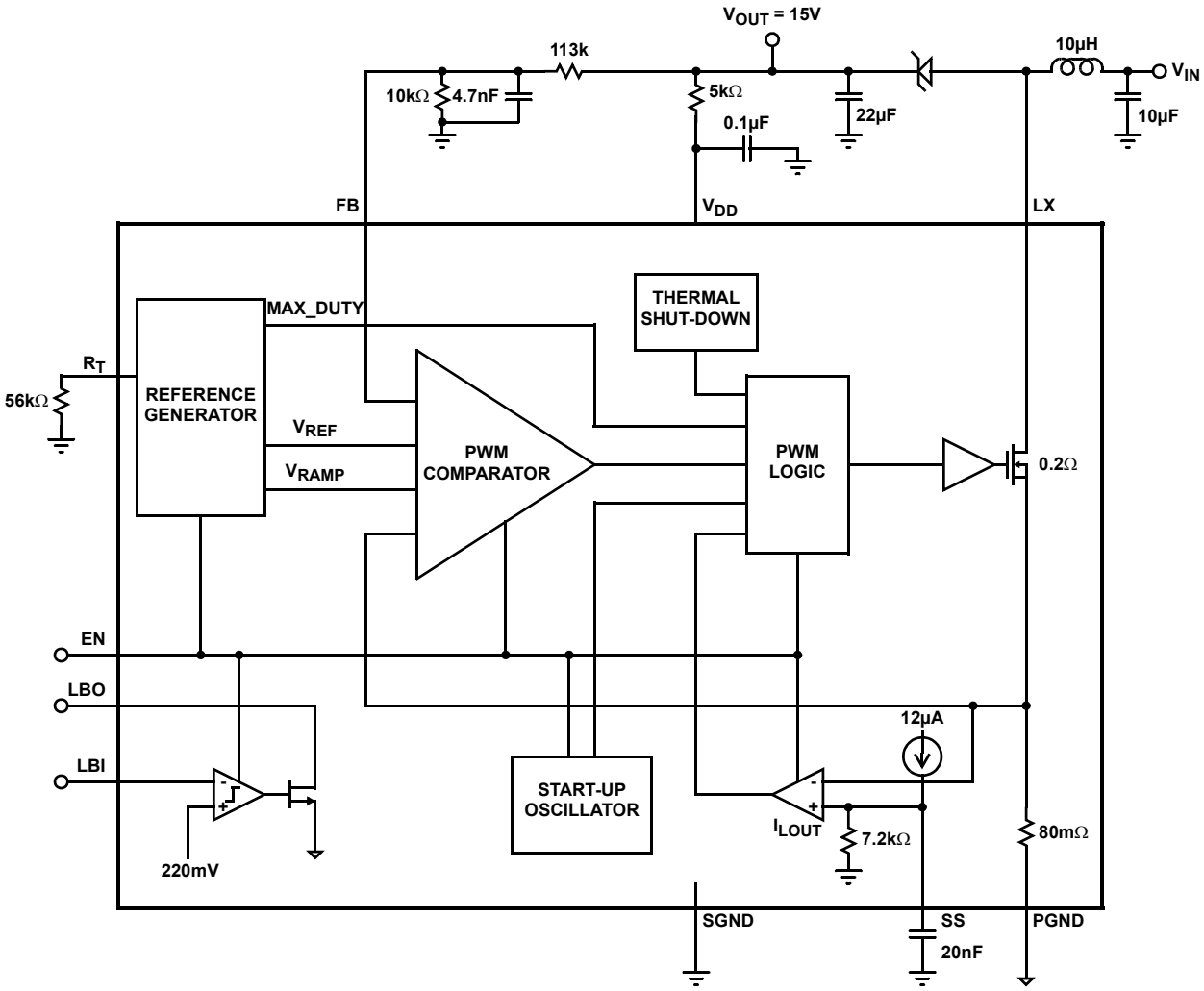
NOTE:

2. Minimum V_{OUT} of 4.5V is tested with V_{IN} = 1.8V.

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	PGND	Power ground; connected to the source of internal N-Channel power MOSFET
2	SGND	Signal ground; ground reference for all the control circuitry; needs to have only a single connection to PGND
3	RT	Timing resistor to adjust the oscillation frequency of the converter. Resistor value on RT pin determines frequency. Range varies from R_T = 49.9kΩ for 750kHz and R_T = 100kΩ for 380kHz
4	EN	Chip enable; connects to logic HI (>1.6V) for chip to function
5	LBI	Low battery input; connects to a sensing voltage, or connect to GND if function is not used
6	LBO	Low battery detection output; connected to the open drain of a MOSFET; able to sink 1mA current
7	SS	Soft-start; connects to a capacitor to control the start-up of the converter. During start-up, V_{SS} controls the current limit and hence the in-rush current.
8	FB	Voltage feedback input; needs to connect to resistor divider to decide V_O
9	VDD	Control circuit positive supply
10	LX	Inductor drive pin; connected to the drain of internal N-Channel power MOSFET

Block Diagram



Typical Performance Curves

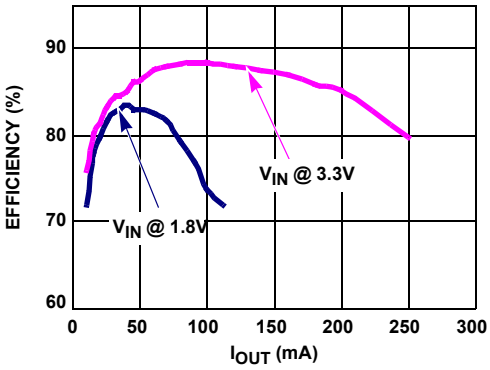


FIGURE 1. EFFICIENCY vs I_{OUT}, V_O = 15V

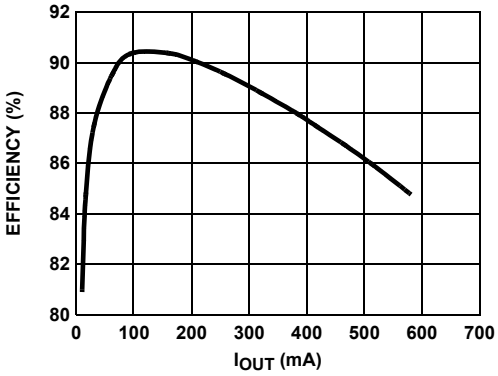


FIGURE 2. EFFICIENCY vs I_{OUT}, V_{IN} = 3.3V, V_O = 5V

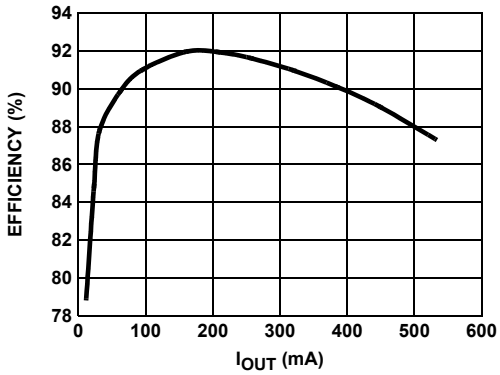


FIGURE 3. EFFICIENCY vs I_{OUT}, V_{IN} = 5V, V_O = 12V

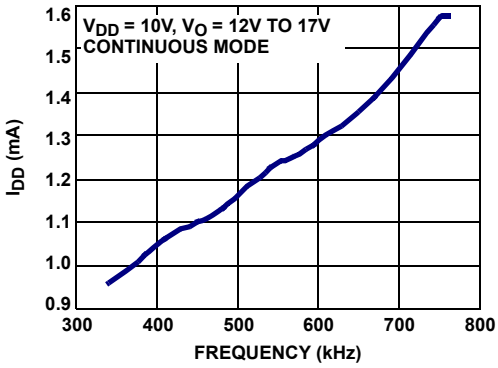


FIGURE 4. I_{DD} vs F_S

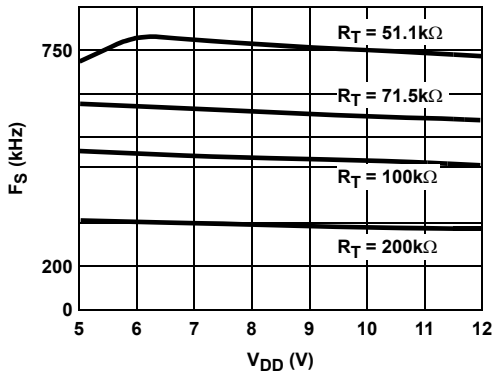


FIGURE 5. F_S vs V_{DD}

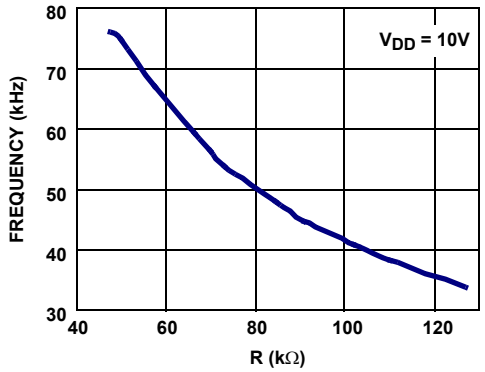


FIGURE 6. F_S vs R_T

Typical Performance Curves (Continued)

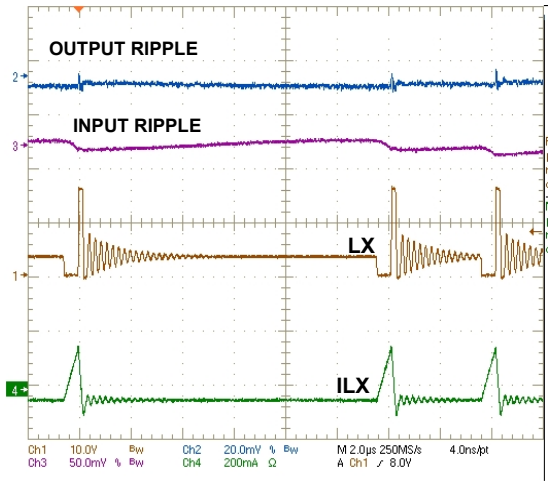


FIGURE 7. STEADY STATE OPERATION (INDUCTOR DISCONTINUOUS CONDUCTION), V_{IN} = 3.3V, V_O = 15V, I_O < 1mA

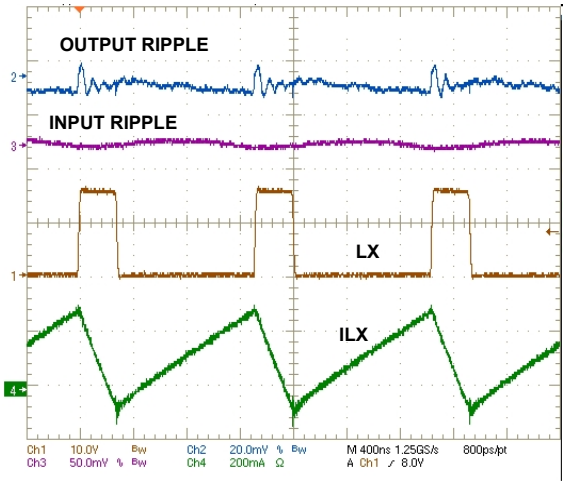


FIGURE 8. STEADY STATE OPERATION (INDUCTOR CONTINUOUS CONDUCTION), V_{IN} = 3.3V, V_O = 15V, I_O = 30mA

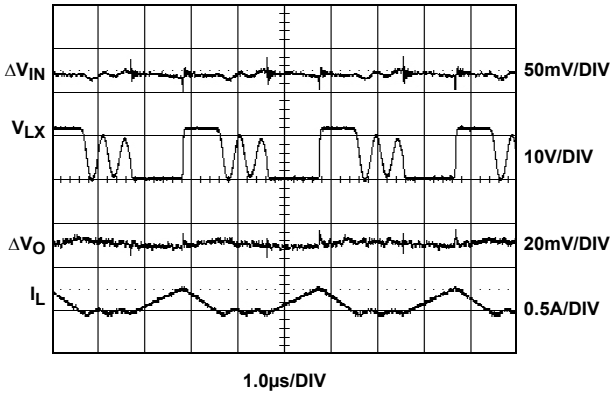


FIGURE 9. STEADY STATE OPERATION (INDUCTOR DISCONTINUOUS CONDUCTION), V_{IN} = 5V, V_O = 12V, I_O = 30mA

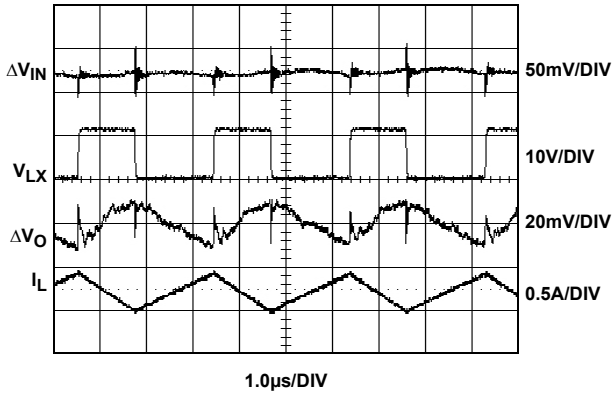


FIGURE 10. STEADY STATE OPERATION (INDUCTOR CONTINUOUS CONDUCTION), V_{IN} = 5V, V_O = 12V, I_O = 300mA

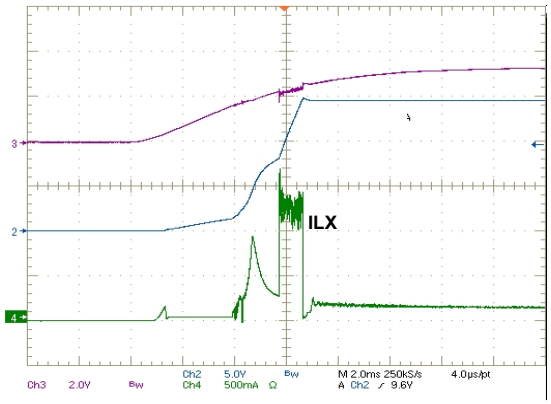


FIGURE 11. POWER-UP, V_{IN} = 3.3V, V_O = 15V, I_O = 30mA

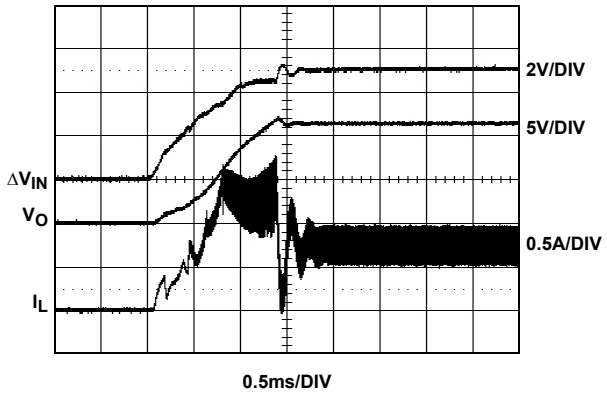


FIGURE 12. POWER-UP, V_{IN} = 5V, V_O = 12V, I_O = 300mA

Typical Performance Curves (Continued)

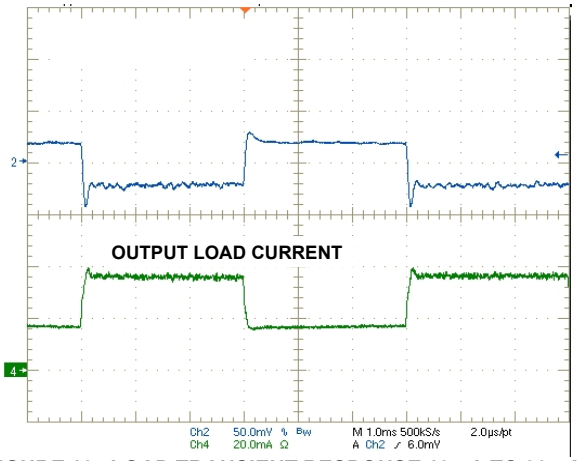


FIGURE 13. LOAD TRANSIENT RESPONSE 10mA TO 30mA, V_{IN} = 1.8V, FREQ = 56.2k, V_O = 15V, I_O = 10mA TO 30mA

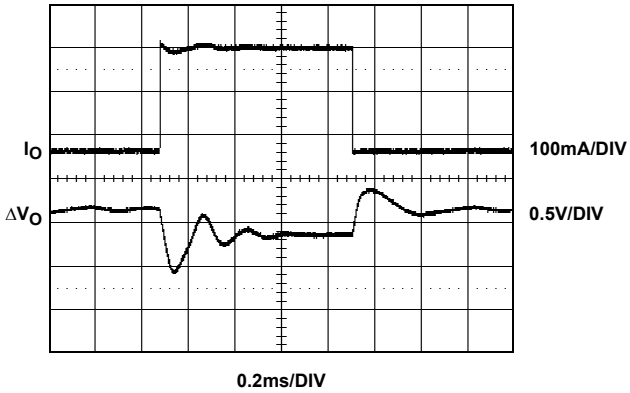


FIGURE 14. LOAD TRANSIENT RESPONSE, V_{IN} = 5V, V_O = 12V, I_O = 50mA TO 300mA

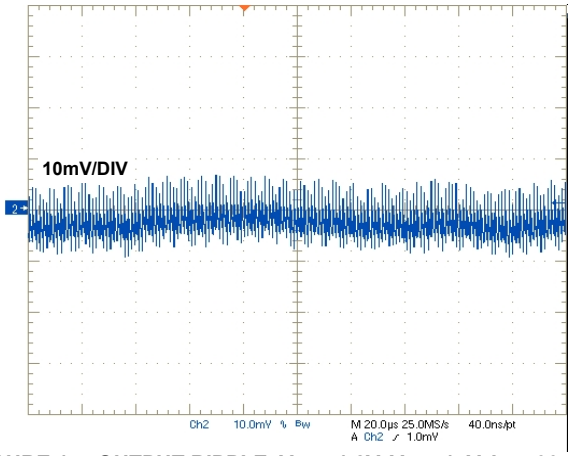


FIGURE 15. OUTPUT RIPPLE, V_{IN} = 1.8V, V_O = 15V, I_O = 30mA

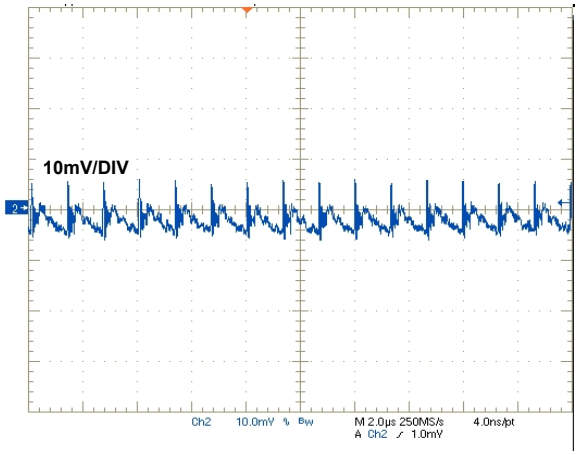


FIGURE 16. OUTPUT RIPPLE, V_{IN} = 3.3V, V_O = 15V, I_O = 30mA

Applications Information

The ISL98012 is a fixed frequency step-up pulse-width modulation (PWM) regulator. The input voltage range is 1.8V to 13.2V and output voltage range is 4.5V to 17V. The switching frequency (up to 750kHz) is decided by the resistor connected to RT pin.

Start-Up

During start-up, as V_{DD} reaches a threshold of about 1.6V, a start-up oscillator generates a fixed duty-ratio of 0.5 to 0.7 at a frequency of several hundred kHz. This will boost the output voltage.

When V_{DD} reaches about 3.7V, the PWM comparator takes over control. The duty ratio will be decided by the least of the multiple-input direct summing comparator, the Max_Duty signal (about 92% duty-ratio), or the Current Limit Comparator.

Soft-start is provided by ramping up the current limit comparator. An internal 12µA current source charges the external CSS capacitor. The peak MOSFET current is limited by the voltage on this capacitor. This in turn controls the rising rate of the output voltage.

The regulator goes through the same start-up sequence as well after the EN signal is pulled to HI.

Steady-State Operation

When the output reaches the preset voltage, the regulator operates in steady state. Depending on the input/output conditions and component values, the inductor operates in either continuous-conduction mode or discontinuous-conduction mode.

In continuous-conduction mode, inductor current is a triangular waveform and LX voltage a pulse waveform. In discontinuous-conduction mode, inductor current has

completely dried out before the MOSFET is turned on again. The input voltage source, the inductor, and the MOSFET and output diode parasitic capacitors form a resonant circuit. Oscillation will occur in this period. This oscillation is normal and will not affect regulation.

At very low load, the MOSFET will skip pulses sometimes; this is normal.

Current Limit

The MOSFET current limit is nominally 1.4A and guaranteed 1A. This restricts the maximum output current I_{OMAX} based on Equation 1:

$$I_{OMAX} = \left(1 - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 1)}$$

where:

- ΔI_L is the inductor peak-to-peak current ripple and is decided by Equation 2:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 2)}$$

- D is the MOSFET turn-on ratio and is decided by Equation 3:

$$D = \frac{V_O - V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

- f_S is the switching frequency

Table1 gives typical values:

TABLE 1. MAX CONTINUOUS OUTPUT CURRENTS

V_{IN} (V)	V_O (V)	L (µH)	f_S (kHz)	I_{OMAX} (mA)
2	5	10	750	360
2	9	10	750	190
2	12	10	750	140
3.3	5	10	750	600
3.3	9	10	750	310
3.3	12	10	750	230
5	9	10	750	470
5	12	10	750	340
9	12	10	750	630
12	15	10	750	670

Component Considerations

It is recommended that C_{IN} is larger than 10µF. Theoretically, the input capacitor has a ripple current of ΔI_L. Due to high-frequency noise in the circuit, the input current ripple may exceed the theoretical value. A larger capacitor will reduce the ripple further.

The inductor has peak and average current decided by Equations 4 and 5:

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 4)}$$

$$I_{LAVG} = \frac{I_O}{1 - D} \quad \text{(EQ. 5)}$$

The inductor should be chosen to handle this current. Furthermore, due to fixed internal compensation, it is recommended that maximum inductance of 10µH and 15µH be used in the 5V and 12V or higher output voltage, respectively.

The output diode has an average current of I_O and peak current is the same as the inductor's peak current. A Schottky diode is recommended and it should be able to handle those currents.

The output voltage ripple can be calculated as Equation 6:

$$\Delta V_O = \frac{I_O \times D}{F_S \times C_O} + I_{LPK} \times ESR \quad \text{(EQ. 6)}$$

Where:

- C_O is the output capacitance.
- The ESR is the output capacitor ESR value.

Low ESR capacitors should be used to minimize output voltage ripple. Multilayer ceramic capacitors (X5R and X7R) are preferred for output capacitors since they have a low ESR and small packages. Tantalum capacitors also can be used, but they take more board space and have higher ESR. A minimum of 22µF output capacitor is sufficient for high output current application. For lower output current, the output capacitor can be smaller, like 4.7µF. The capacitor should always have enough voltage rating. In addition to the voltage rating, the output capacitor should also be able to handle the RMS current, which is given by Equation 7:

$$I_{CORMS} = \sqrt{(1 - D) \times \left(D + \frac{\Delta I_L^2}{I_{LAVG}^2} \times \frac{1}{12}\right)} \times I_{LAVG} \quad \text{(EQ. 7)}$$

Output Voltage

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. The current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network less than 300kΩ is recommended.

The boost converter output voltage is determined by the relationship in Equation 8:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_2}{R_1}\right) \quad \text{(EQ. 8)}$$

where V_{FB} slightly changes with V_{DD}.

RC Filter

The maximum voltage rating for the VDD pin is 12V. An RC filter is recommended to clean the output ripple before bootstrapping the part. For bootstrapped applications with V_{OUT} greater than 10V, R_4 can drop V_{OUT} for coupling into the VDD pin and is given by Equation 9:

$$R_4 = \frac{V_O - 10}{I_{DD}} \quad \text{(EQ. 9)}$$

where I_{DD} is shown in the I_{DD} vs f_S curve. Otherwise, R_4 can be 10Ω to 51Ω with C_4 = 0.1µF.

Thermal Performance

The ISL98012 uses a fused-lead package, which has a reduced θ_{JA} of +100°C/W on a four-layer board and +115°C/W on a two-layer board. Maximizing copper around the ground pins will improve the thermal performance.

This chip also has internal thermal shut-down set at around +135°C to protect the component.

Layout Considerations

The layout is very important for the converter to function properly. power ground (⏚) and signal ground (⏚) should be separated to ensure that the high pulse current in the power ground never interferes with the sensitive signals connected to signal ground. They should only be connected at one point.

The trace connected to pin 8 (FB) is the most sensitive trace. It needs to be as short as possible and in a “quiet” place, preferably between PGND or SGND traces.

In addition, the bypass capacitor connected to the VDD pin needs to be as close to the pin as possible.

The heat of the chip is mainly dissipated through the SGND pin. Maximizing the copper area around it is preferable. In addition, a solid ground plane is always helpful for the EMI performance.

The demo board is a good example of layout based on these principles. Please refer to the ISL98012 Technical Brief for the layout.

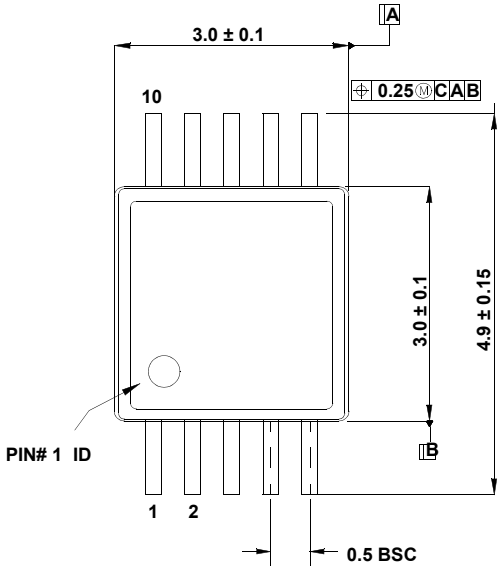
http://www.intersil.com/data/tb/tb429.pdf

Package Outline Drawing

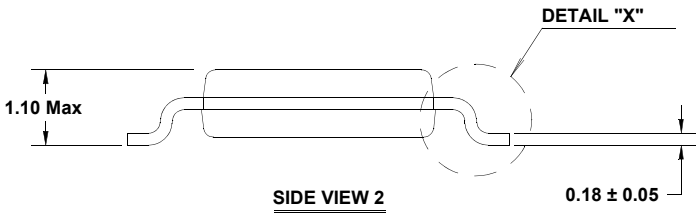
M10.118A (JEDEC MO-187-BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

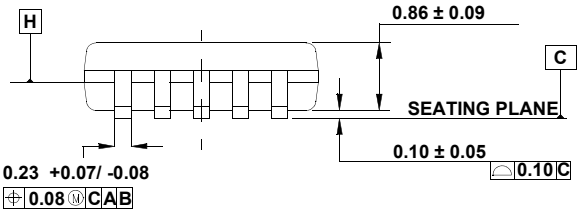
Rev 0, 9/09



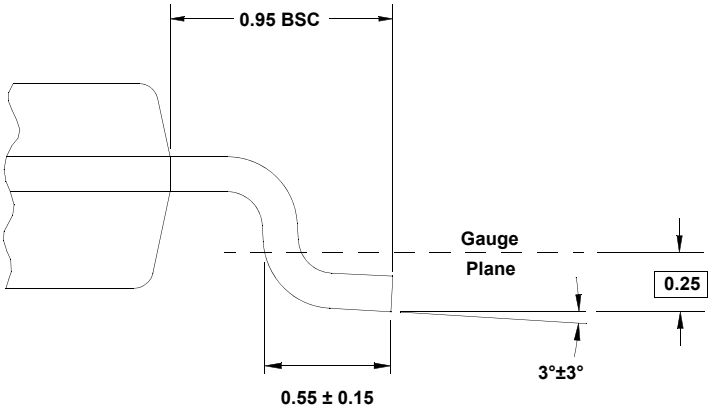
TOP VIEW



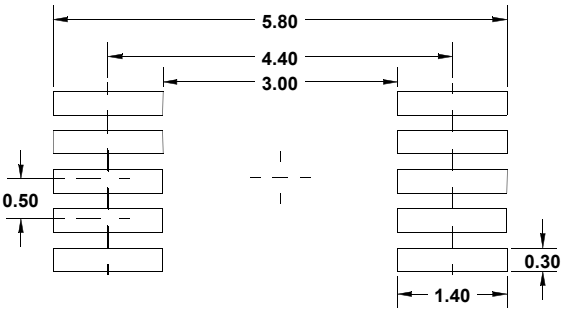
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.